Io=3.0A Low output voltage Adjustable LDO with dual input voltages

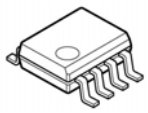
■ GENERAL DESCRIPTION

The NJW4111 is a low output voltage, low drop out adjustable regulators that delivers low output voltage from 0.8 to 1.8V with high precision and high line/load regulations.

It has also built-in current limit, under voltage lock-out, soft start function and short circuit protection (Timer latch type).

It is suitable for a low noise constant voltage source such as the chip-set that demand a large output current up to 3.0A.

■ OUTLINE

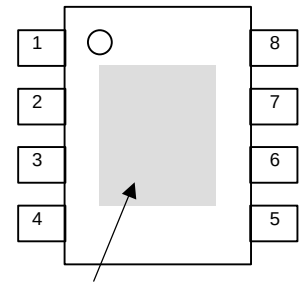


NJW4111GM1

■ FEATURES

- Dual input voltage V_{IN} : 0.8 to 3.3V
  V_{BIAS}: 4.3 to 5.5V
- Output current I_{OUT}(min.) = 3.0A
- High precision reference V_{FB} = 0.65V±1%
- Adjustable output voltage 0.8V to 1.8V
- ON/OFF function
- Discharge function
- Soft start function to reduces in-rush current $T_{CS(ON)}$ = 3msec typ.
- Undervoltage lockout (UVLO) circuit
- Thermal shutdown circuit (Timer latch type)
- Over current protection
- Short circuit protection (Timer latch type)
- Package HSOP8

■ PIN CONFIGURATION



NJW4111GM1

1. V_{OUT} :Output Voltage Pin
2. V_{OUT} :Output Voltage Pin
3. FB :Reference Voltage Feedback Pin
4. GND :Ground Pin
5. V_{BIAS} :Bias Voltage Pin
6. CONTROL :Control Pin
7. V_{IN} :Input Voltage Pin
8. V_{IN} :Input Voltage Pin

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYNBOL	RATINGS	UNIT
Input Voltage	V_{IN}	+4	V
Bias Voltage	V_{BIAS}	+6	V
Control Voltage	V_{CONT}	+6	V
Output Current	I_{OUT}	3	A
Power Dissipation	P_D	790(*1) 2500(*2)	mW
Junction Temperature	Tj	-40 to +150	°C
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tstg	-40 to +150	°C

(*1)：Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 2Layers)
(*2)：Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 4Layers)
(For 4Layers : Applying 74.2 x 74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYNBOL	MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{IN}	0.8	-	3.3	V
Bias Voltage	V_{BIAS}	4.3	-	5.5	V
Control Voltage	V_{CONT}	-0.3	-	5.5	V
Output voltage Range	V_{OUT}	0.8	-	1.8	V

■ BUILT-IN PROTECTION CIRCUIT

PARAMETER	NOTE
Over current protection	-
Short circuit protection	Timer latch type
Thermal shutdown circuit	Timer latch type

■ BUILT-IN FUNCTION

PARAMETER	NOTE
Soft start Function	3msec typ.
V_{IN}-UVLO	0.73V typ.
V_{BIAS}-UVLO	3.8V typ.
Power supply injection sequence-free	-

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{BIAS}=5V, V_{CONT}=3V, V_{IN}=V_{OUT}+0.5V, C_{BIAS}=1µF, C_{IN}=22µF, C_O=10µF, C_{FB}=1000pF, Ta=25°C)

General Characteristic

PARAMETER	SYNBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Bias Current	$I_{Q(BIAS)}$	I_{OUT}=0mA, except I_{CONT}	-	1.4	2.2	mA
Bias Current at OFF	$I_{Q(BIAS/OFF)}$	V_{CONT}=0V	-	-	100	nA
Input Current at OFF	$I_{Q(VIN/OFF)}$	V_{CONT}=0V	-	-	100	nA
Feedback Voltage	V_{FB}		-1.0%	0.65	+1.0%	V
Output Current	I_{OUT}	$V_{OUT} \times 0.9$	3.0	-	-	A
Line Regulation (V_{BIAS})	$\Delta V_O/\Delta V_{BIAS}$	V_{BIAS} =4.2V to 5.5V, I_{OUT}=30mA	-	-	0.5	%/V
Line Regulation (V_{IN})	$\Delta V_O/\Delta V_{IN}$	V_{IN}=V_{OUT}+0.5V to 3.3V, I_{OUT}=30mA	-	-	0.5	%/V
Load Regulation	$\Delta V_O/\Delta I_O$	I_{OUT}=0mA to 3A	-	-	10	mV
Output ON Resistance	R_{ON}	I_{OUT}=3A, V_{IN}=1.2V	-	28	50	mΩ
Discharge Current at OFF	$I_{O(OFF)}$	V_{CONT}=0V, V_O=1V	1	-	-	mA
Feedback Current	I_{FB}		-100	0	+100	nA
V_{IN} Pin Leak Current	$I_{LEAK(IN)}$	V_{BIAS} = V_{CONT} =5V, V_{IN}=0V	-	0.25	0.60	µA

ON/OFF Control Block

PARAMETER	SYNBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Control Voltage for ON-state	$V_{CONT(ON)}$	V_{CONT}: Sweep up	1.6	-	-	V
Control Voltage for OFF-state	$V_{CONT(OFF)}$	V_{CONT}: Sweep down	-	-	0.6	V
Control Current	I_{CONT}	V_{CONT}=1.6V	1	3	12	µA
Soft Start Time	$T_{CS(ON)}$	V_{CONT}=L→H	-	3	-	msec

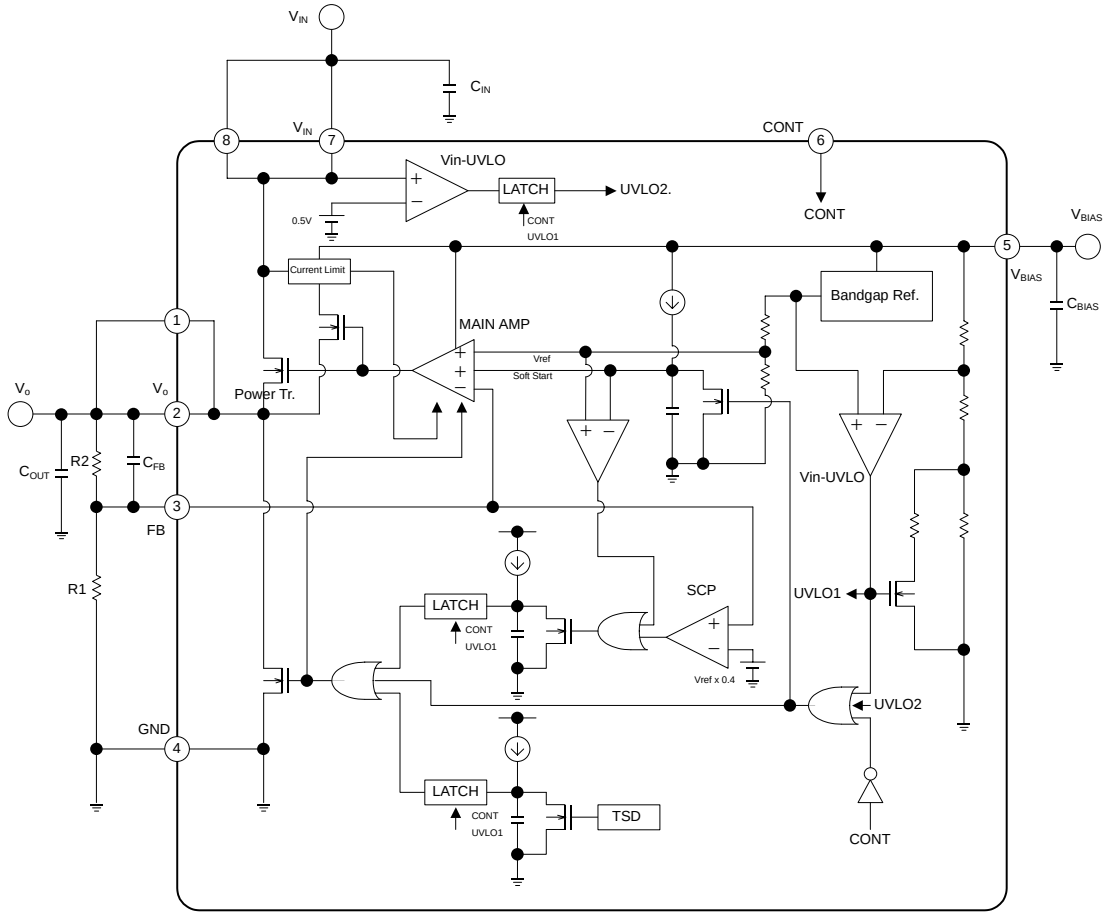
UVLO Block

PARAMETER	SYNBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{BIAS} Undervoltage Lockout Threshold Voltage	V_{BIAS}UVLO	V_{BIAS}: Sweep up	3.5	3.8	4.1	V
V_{BIAS} Undervoltage Lockout Hysteresis Voltage	V_{BIAS}HYS	V_{BIAS}: Sweep down	100	160	220	mV
V_{IN} Undervoltage Lockout Threshold Voltage	V_{IN}UVLO	V_{IN}: Sweep up	0.71	0.73	0.75	V

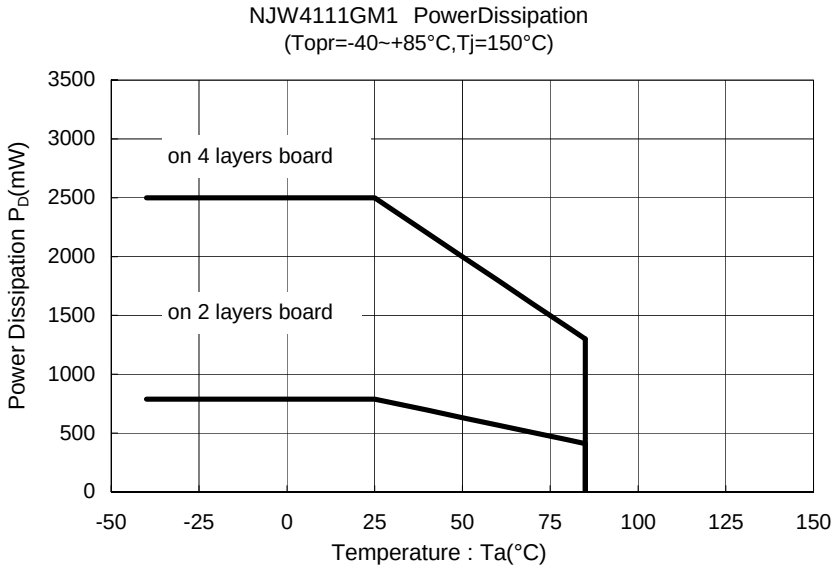
SCP Block

PARAMETER	SYNBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SCP Start up Voltage	V_{OCSP}		Vo×0.32	Vo×0.33	Vo×0.34	V
SCP Timer Latch Time	T_{SCP}		-	200	-	µsec

■ BLOCK DIAGRAM



■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



■ PIN DESCRIPTIONS

PIN NUMBER	PIN NAME	FUNCTION
1	V_{OUT}	Output Voltage pin. It can be adjusted from 0.8V to 1.8V.
2	V_{OUT}	Output Voltage pin. It can be adjusted from 0.8V to 1.8V.
3	FB	Output Voltage Detecting pin. Connected output voltage through the resistor divider tap to this pin in order to voltage of the FB pin become 0.65V typ.
4	GND	GND pin.
5	V_{BIAS}	Power supply for IC Control bias. Insert the capacitor between V_{BIAS} pin and GND pin for reduce the power supply impedance.
6	CONTROL	ON/OFF control pin for NJW4111. Normal Operation at the time of High level. Standby Mode at the time of Low level or Open.
7	V_{IN}	Power supply for power line. Insert the capacitor between V_{IN} pin and GND pin for reduce the power supply impedance.
8	V_{IN}	Power supply for power line. Insert the capacitor between V_{IN} pin and GND pin for reduce the power supply impedance.
-	Exposed PAD	Connected to GND pin.

■ DESCRIPSION OF EACH BLOCK

• MAIN AMP

This is an error amp compares the reference voltage (0.65V) with V_{OUT} to drive the output Nch-MOSFET. This amp's phase compensation is designed to be able to use a very low ESR capacitor from 0.02Ω.

• CONTROL

Control block switches the regulator's ON/OFF state. In the OFF state, circuit current is maintained at 0μA, and minimize current consumption at standby. Discharge circuit, connected to the V_{OUT} pin, pulls up an unnecessary electric charge and prevents the malfunction of the load side in the OFF state.

• V_{BIAS} - UVLO

ULVO block for bias voltage turns the output voltage off to prevent malfunction when V_{BIAS} is the threshold voltage or less. At the time of the lockout, discharges output voltage in the same way as OFF state.

• V_{IN} - UVLO

When the V_{IN} voltage is beyond 0.5V(typ.), UVLO block for input voltage turns the output on. The output does not turn off when once a lockout is released even if the V_{IN} voltage falls. But, when the V_{IN} voltage falls and the V_{OUT} voltage falls below the SCP threshold voltage, turn the output off due to SCP. The V_{IN}-UVLO is available only at the time of startup. If the V_{CONT} or the V_{BIAS} is re-injected, V_{IN}-UVLO will be available again.

• Over Current Protection

This circuit protect an IC of the load side to damp the output voltage when output current exceed the constant value.
When the overcurrent state eliminated, output voltage restored to the parameter value. However when output voltage is less than SCP startup voltage, the SCP function becomes active and output switches OFF

• Thermal Shutdown (TSD)

Thermal Shutdown circuit is latched OFF the output when the chip temperature exceeds the threshold temperature after the programmed time period elapses. Because equipped with a latch function, maintain an Off state till apply CONTROL or V_{BIAS} again. Because TSD circuit is builted-in for the purpose of protecting IC itself, please do the thermal design within Tj(max).

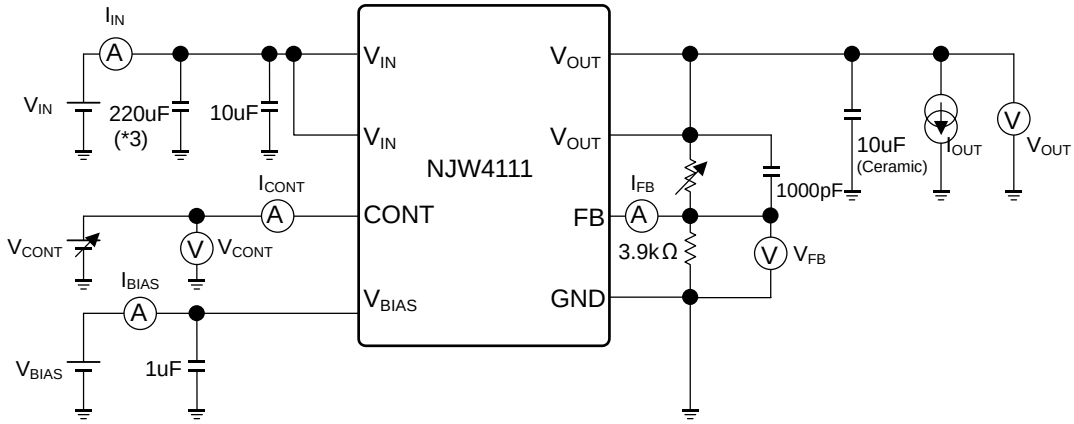
• Short Circuit Protection(SCP)

When output voltage drops, NJW4111 assumes that V_{OUT} pin is shorted to GND and switched output OFF after a certain period of time. Because equipped with a latch function, maintain an Off state till apply CONTROL or V_{BIAS} again.

When SCP becomes effective, and an output current is intercepted, please be careful the voltage more than the maximum rating be never impressed on a V_{IN} pin.(refer to *4)

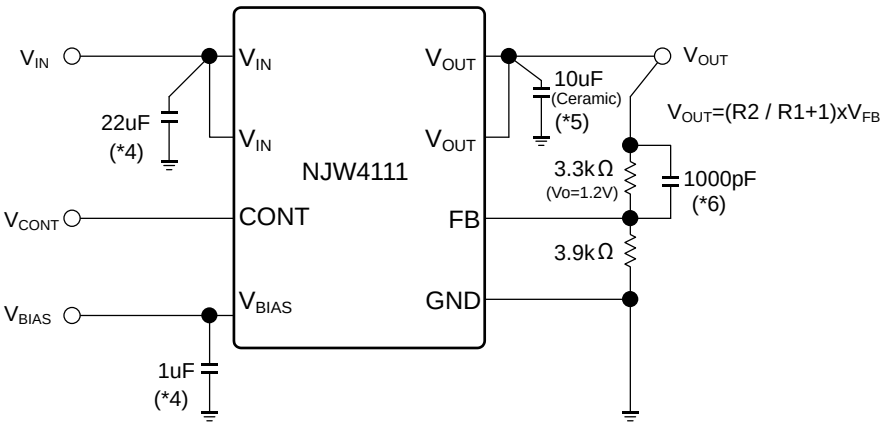
For prevention of malfunction on start up, this circuit becomes invalid at the time of the start (effective Soft start function) temporarily.

■ TEST CIRCUIT



(*3)Provision for supply impedance of the measuring instrument

■ TYPICAL APPLICATION



(*4) Input Capacitor $C_{IN,}$ Bias Capacitor C_{BIAS}

Input Capacitor C_{IN} and Bias Capacitor C_{BIAS} are required to prevent oscillation and reduce power supply ripple for applications with high power supply impedance or a long power supply line. Please use the C_{IN} of recommended value larger to avoid the problem.(C_{BIAS}≥1.0μF,C_{IN}≥22μF)

C_{IN} and C_{BIAS} should connect between GND and V_{IN}, V_{BIAS} as shortest path as possible.

Recommend large capacity value C_{IN} because tend to become unstable in input voltage (V_{IN}) when a load change is heavy.

Please for enough confirmation with the actual machine to strongly depend on the characteristic of power supply to use for inputs and the pattern of the board.

(*5) Output Capacitor C_O

Output capacitor (C_O) will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

This product is designed to work with a low ESR capacitor (C_O). However use of recommended capacitance or larger value is effective for stable operation.

Use of a smaller C_O may cause excess output noise or oscillation of the regulator due to lack of the phase compensation.

Therefore use C_O with the recommended capacitance or larger value and connect between Vo terminal and GND terminal with shortest path. The recommended capacitance depends on the output voltage rank. Low voltage regulator requires larger value C_O. Thus, check the recommended capacitance for each output voltage rank.

Uses of a larger C_O reduces output noise and ripple output, and also improves output transient response against rapid load change.

It depends on the pattern of the board and power supply use for input, Power supply(V_{IN}) becomes unstable and tends to be easy to cause an oscillation, aggravation of Ripple Rejection and output transient response characteristics when design it C_{IN}<C_O.

Therefore, like a mention of the (*4), please connect C_{IN} of enough capacity value, and improve stabilization of input power supply (V_{IN}).

(*6) Feedback Capacitor C_{FB}

Please insert the C_{FB} for stable operation by all means.

It correct phase compensation of the IC inside and can support the output capacitor of various kinds.

(*7) Output voltage setting resistance R1,R2

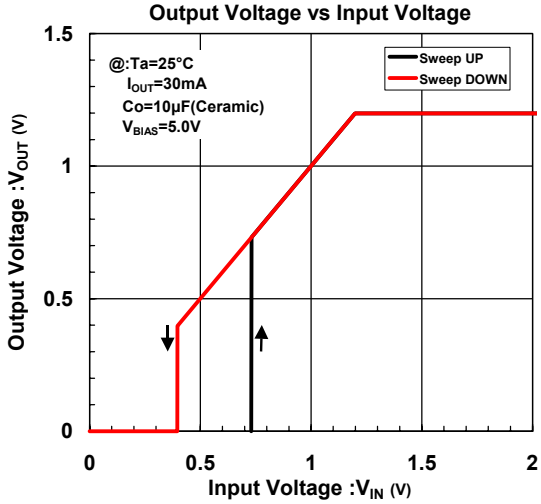
Output voltage can be set with a configuration formula (R2/R1+1)×V_{FB} using the values for the internal reference output voltage(V_{FB}) and the output voltage resistors(R1,R2).

Select resistance values that will avoid the influence of the Feedback Current I_{FB}(±100nA).

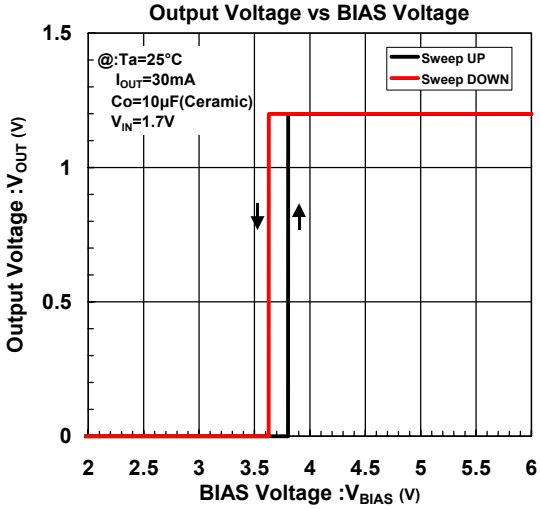
The recommended total resistance value is about 10kΩ

■ TYPICAL CHARACTERISTICS

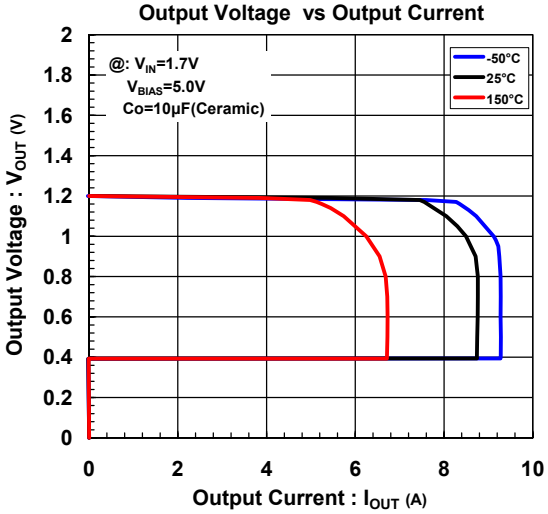
NJW4111_1.2V
Output Voltage vs Input Voltage



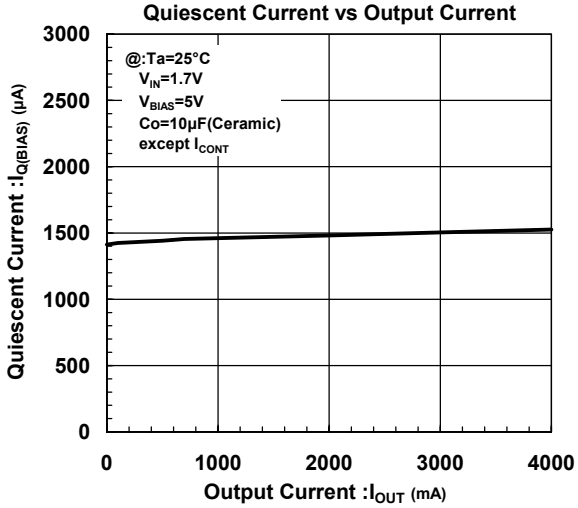
NJW4111_1.2V
Output Voltage vs BIAS Voltage



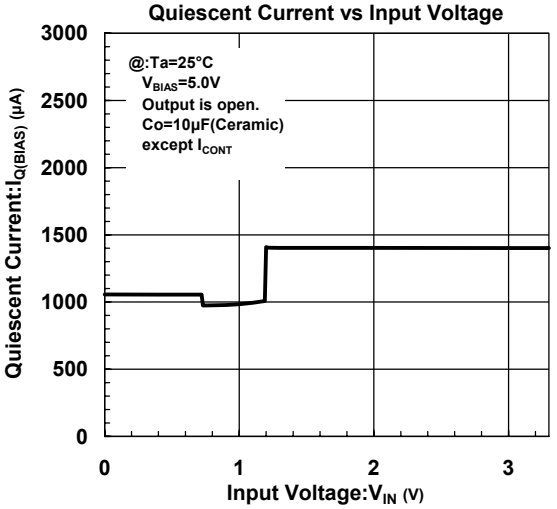
NJW4111_1.2V
Output Voltage vs Output Current



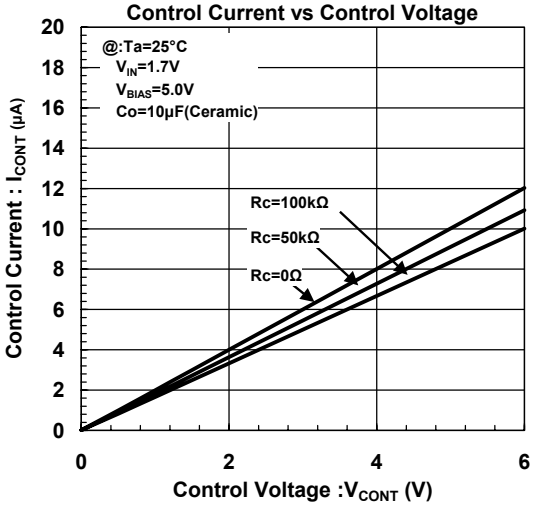
NJW4111_1.2V
Quiescent Current vs Output Current



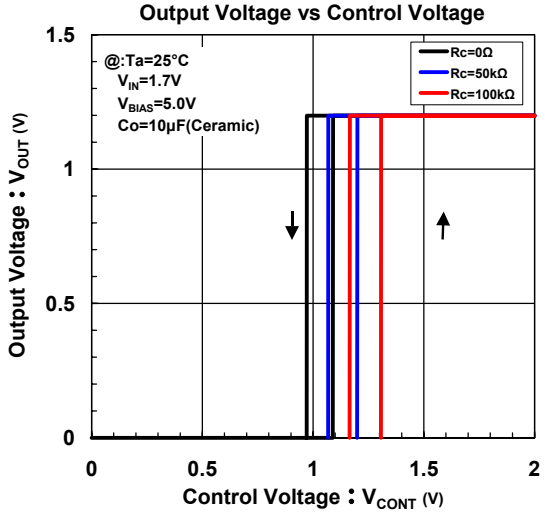
NJW4111_1.2V
Quiescent Current vs Input Voltage



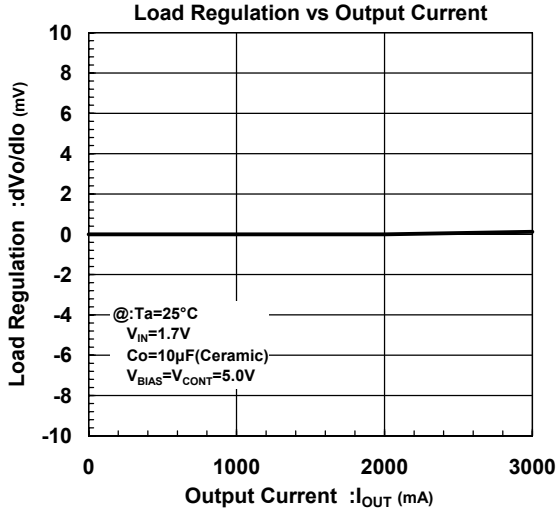
NJW4111_1.2V
Control Current vs Control Voltage



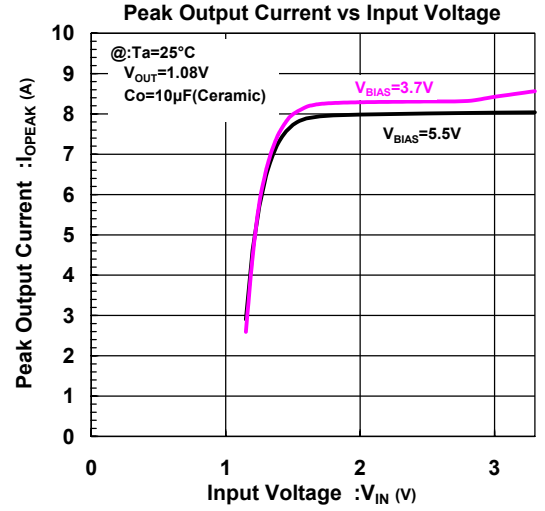
NJW4111_1.2V
Output Voltage vs Control Voltage



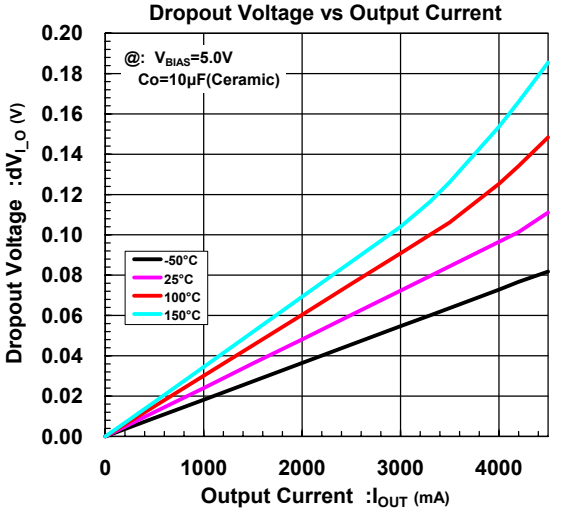
NJW4111_1.2V
Load Regulation vs Output Current



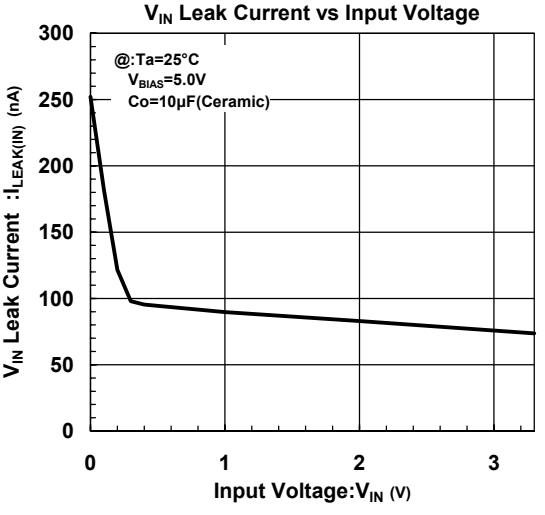
NJW4111_1.2V
Peak Output Current vs Input Voltage



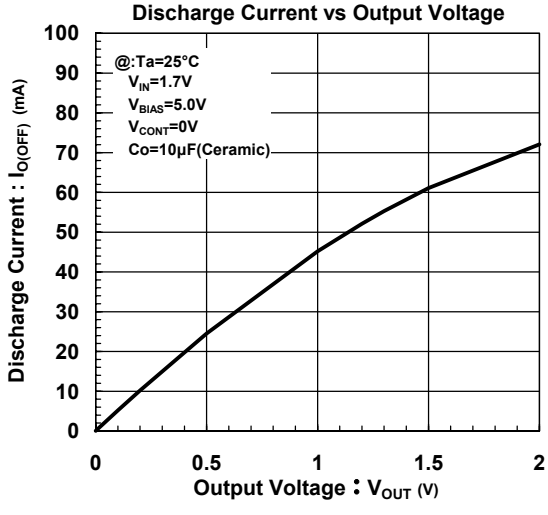
NJW4111_1.2V
Dropout Voltage vs Output Current



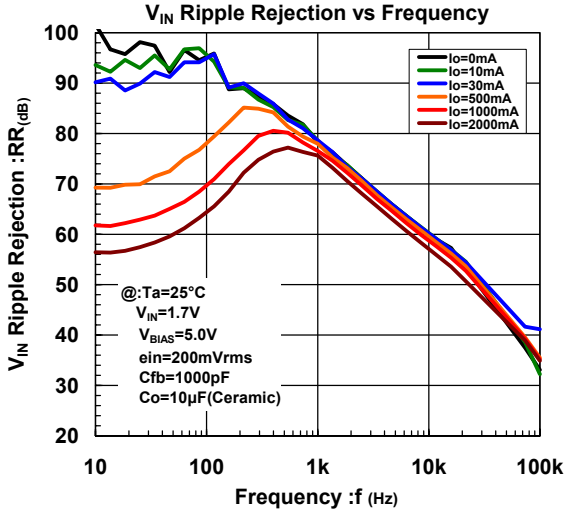
NJW4111_1.2V
VIN Leak Current vs Input Voltage



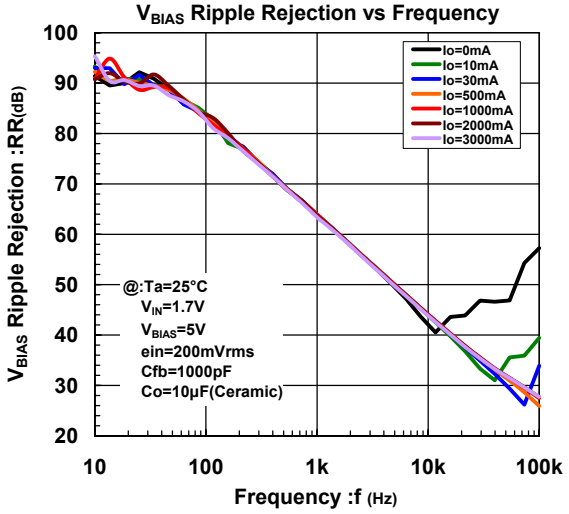
NJW4111_1.2V
Discharge Current vs Output Voltage



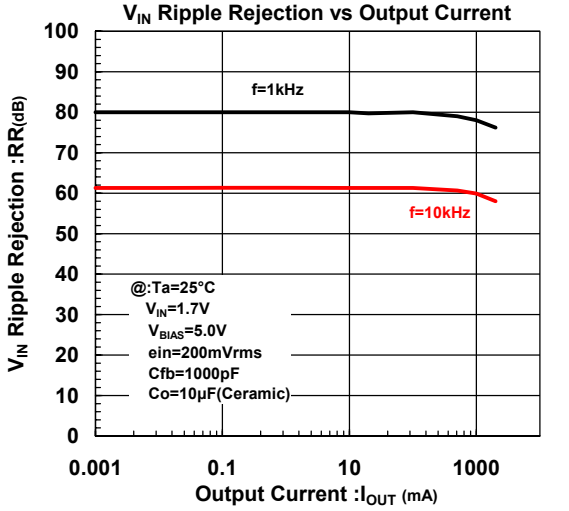
NJW4111_1.2V
V_{IN} Ripple Rejection vs Frequency



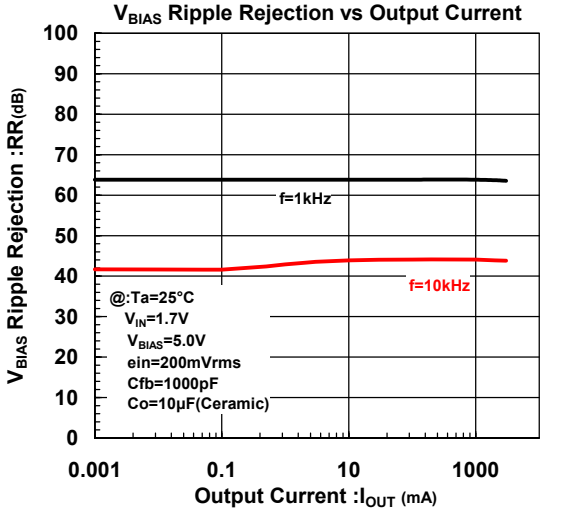
NJW4111_1.2V
V_{BIAS} Ripple Rejection vs Frequency



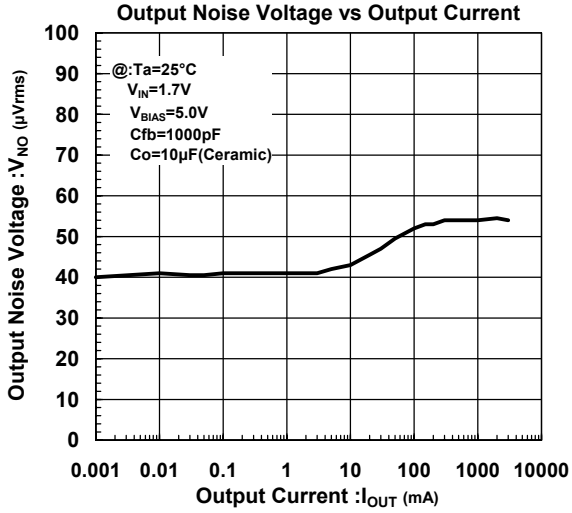
NJW4111_1.2V
V_{IN} Ripple Rejection vs Output Current



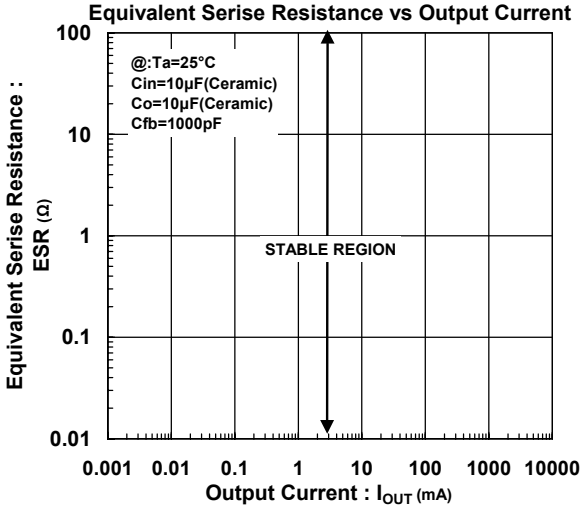
NJW4111_1.2V
V_{BIAS} Ripple Rejection vs Output Current



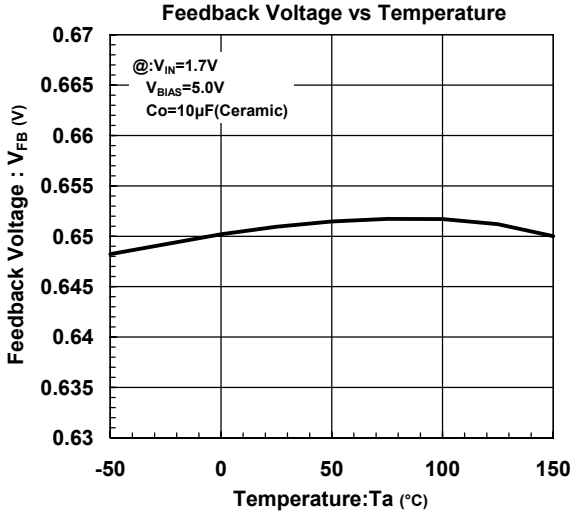
NJW4111_1.2V
Output Noise Voltage vs Output Current



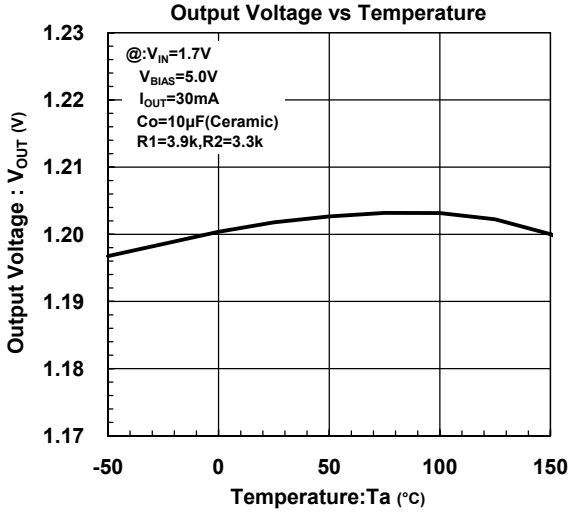
NJW4111_1.2V
Equivalent Serise Resistance vs Output Current



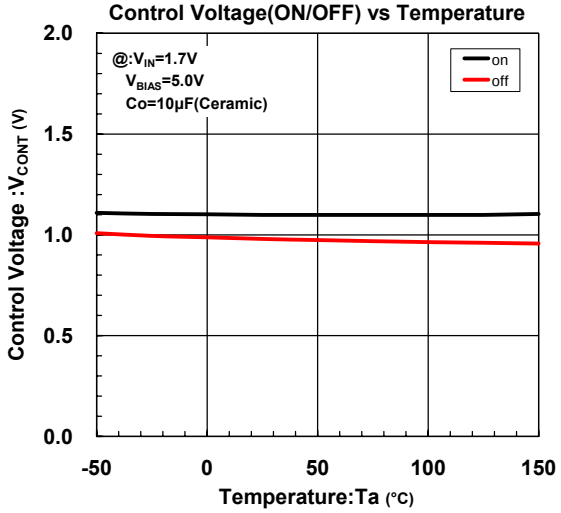
NJW4111_1.2V
Feedback Voltage vs Temperature



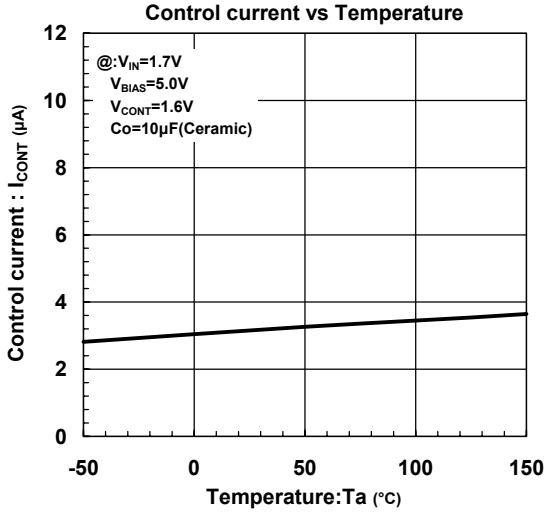
NJW4111_1.2V
Output Voltage vs Temperature



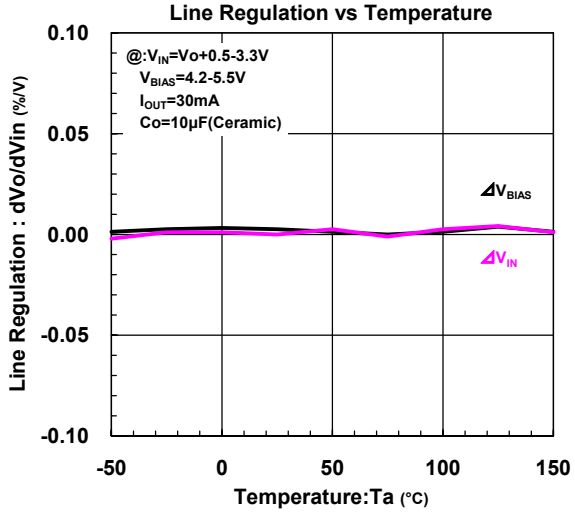
NJW4111_1.2V
Control Voltage(ON/OFF) vs Temperature



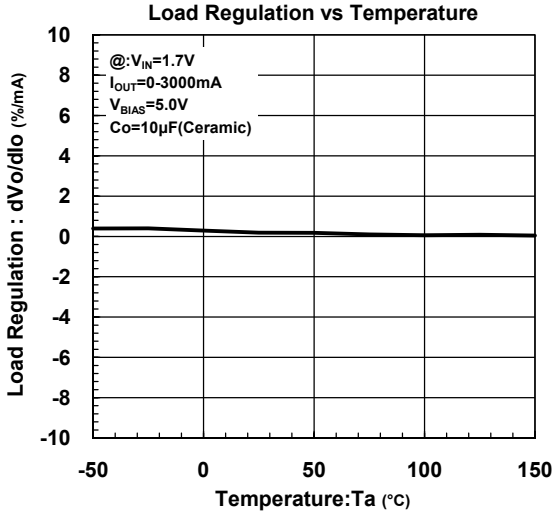
NJW4111_1.2V
Control current vs Temperature



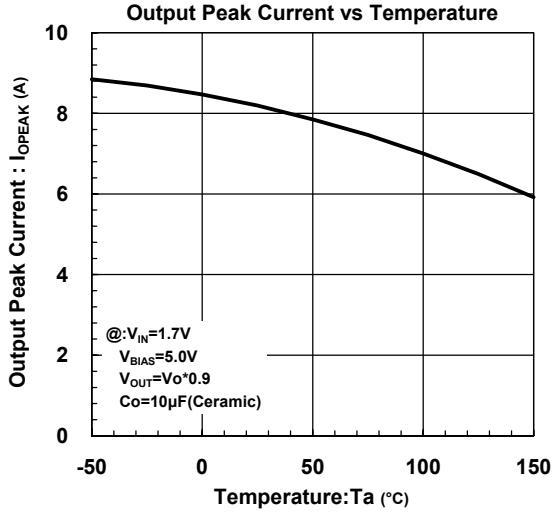
NJW4111_1.2V
Line Regulation vs Temperature



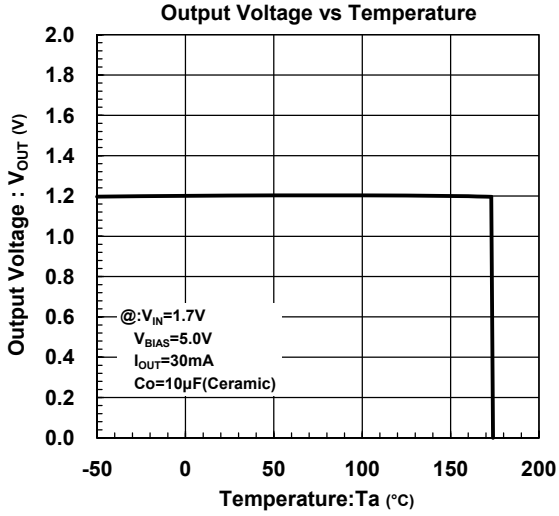
NJW4111_1.2V
Load Regulation vs Temperature



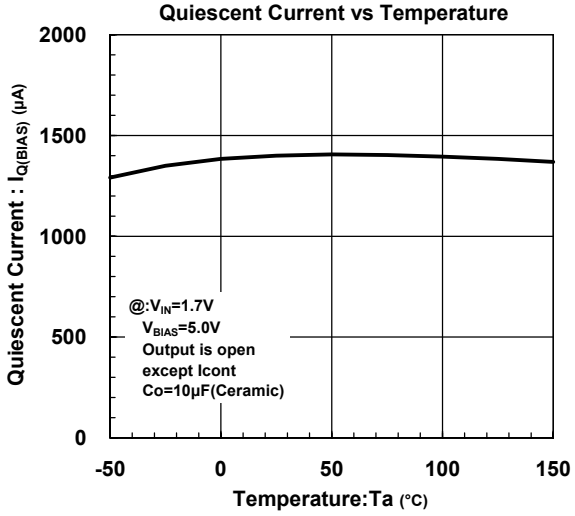
NJW4111_1.2V
Output Peak Current vs Temperature



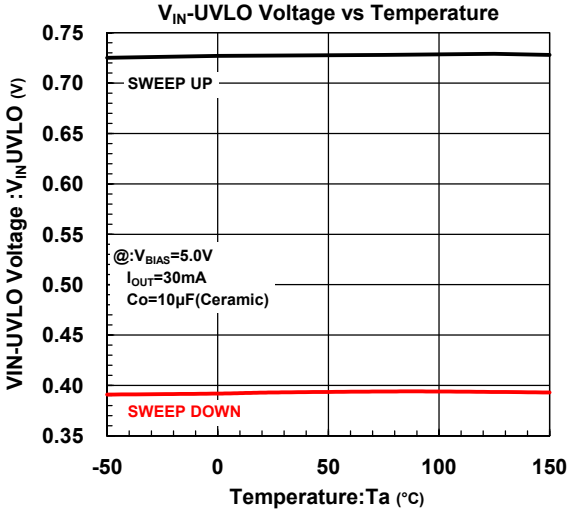
NJW4111_1.2V
Output Voltage vs Temperature



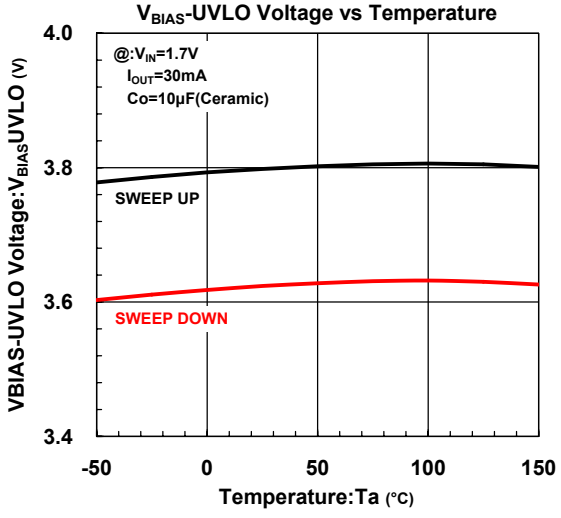
NJW4111_1.2V
Quiescent Current vs Temperature



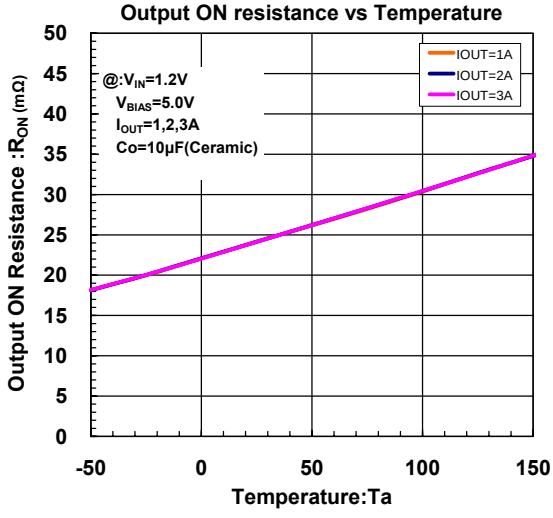
NJW4111_1.2V
V_{IN}-UVLO Voltage vs Temperature

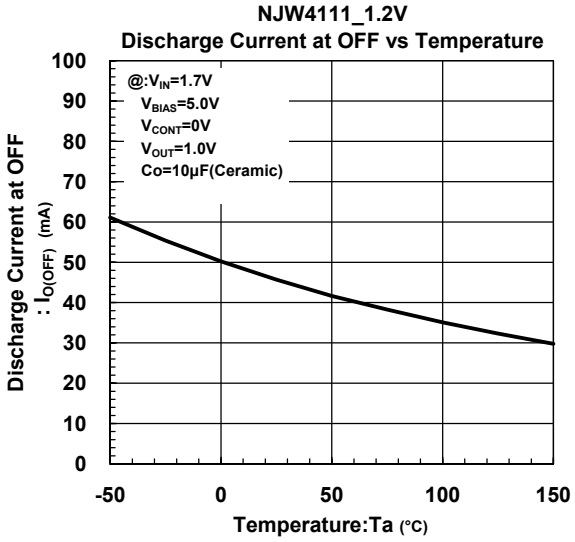


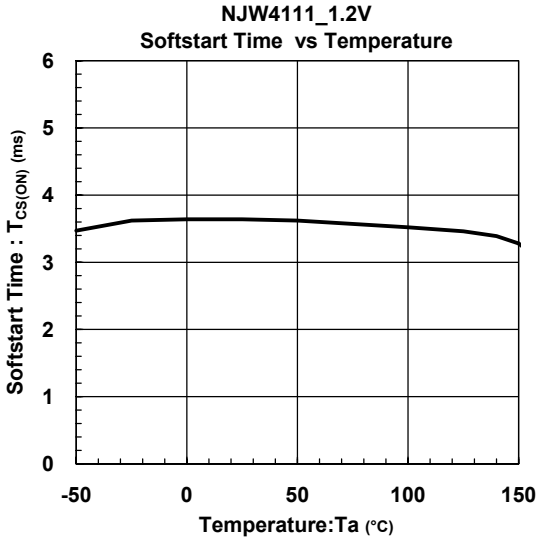
NJW4111_1.2V
V_{BIAS}-UVLO Voltage vs Temperature

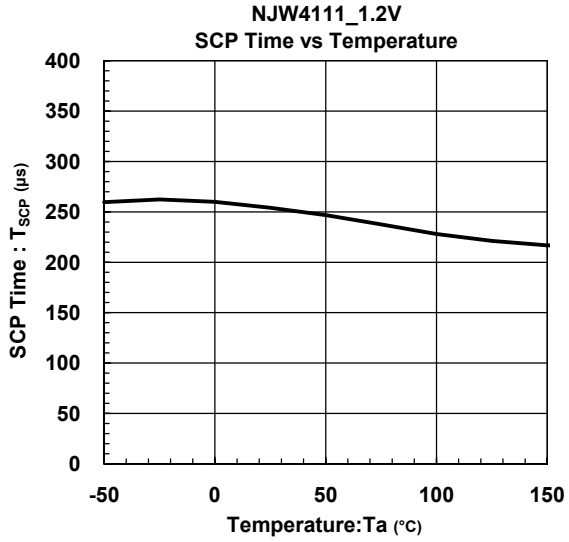


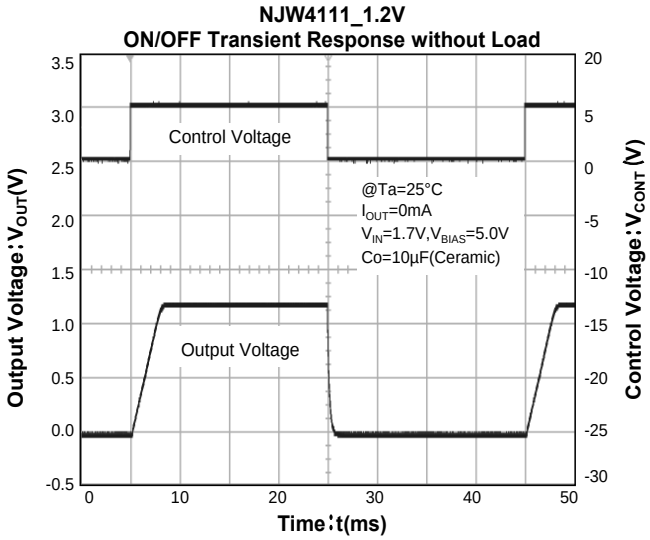
NJW4111_1.2V
Output ON resistance vs Temperature

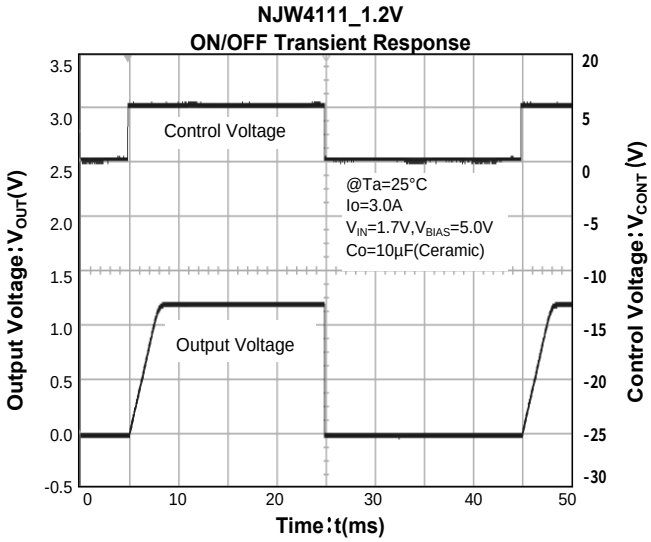


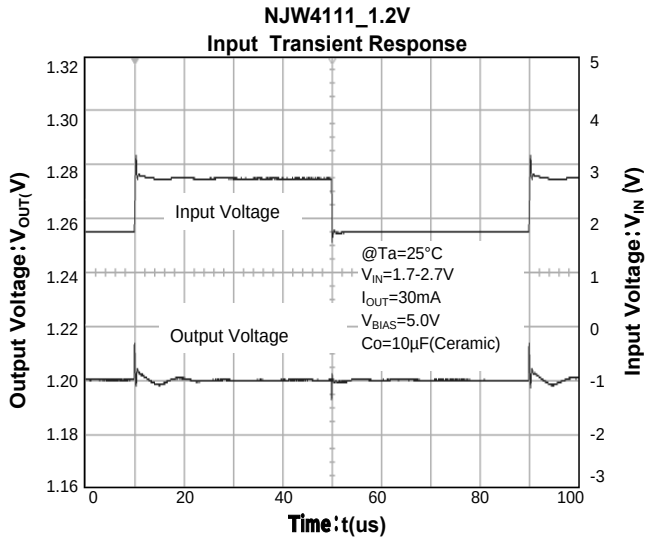

NJW4111_1.2V
Discharge Current at OFF vs Temperature
@:V_IN=1.7V
V_BIAS=5.0V
V_CONT=0V
V_OUT=1.0V
Co=10µF(Ceramic)
Discharge Current at OFF : I_O(OFF) (mA)
Temperature:Ta (°C)

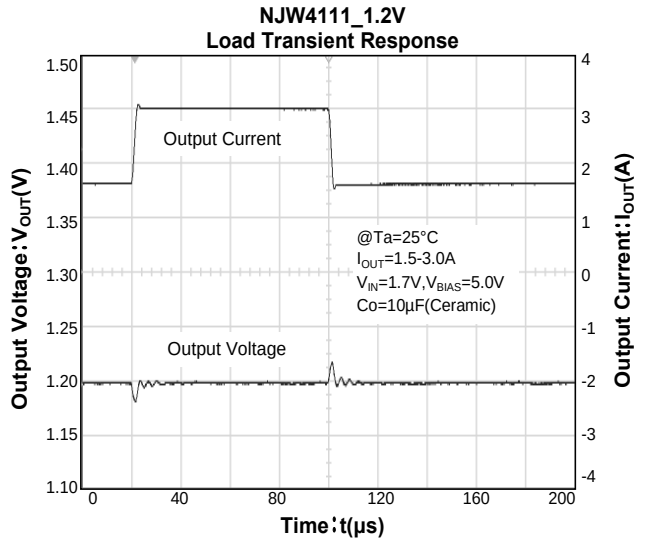

NJW4111_1.2V
Softstart Time vs Temperature
Softstart Time : T_CS(ON) (ms)
Temperature:Ta (°C)


NJW4111_1.2V
SCP Time vs Temperature
SCP Time : T_SCP (µs)
Temperature:Ta (°C)


NJW4111_1.2V
ON/OFF Transient Response without Load
Control Voltage
Output Voltage
@Ta=25°C
I_OUT=0mA
V_IN=1.7V,V_BIAS=5.0V
Co=10µF(Ceramic)
Output Voltage:V_OUT(V)
Control Voltage:V_CONT (V)
Time:t(ms)


NJW4111_1.2V
ON/OFF Transient Response
Control Voltage
Output Voltage
@Ta=25°C
Io=3.0A
V_IN=1.7V,V_BIAS=5.0V
Co=10µF(Ceramic)
Output Voltage:V_OUT(V)
Control Voltage:V_CONT (V)
Time:t(ms)


NJW4111_1.2V
Input Transient Response
Input Voltage
Output Voltage
@Ta=25°C
V_IN=1.7-2.7V
I_OUT=30mA
V_BIAS=5.0V
Co=10µF(Ceramic)
Output Voltage:V_OUT(V)
Input Voltage:V_IN (V)
Time:t(us)


NJW4111_1.2V
Load Transient Response
Output Current
Output Voltage
@Ta=25°C
I_OUT=1.5-3.0A
V_IN=1.7V,V_BIAS=5.0V
Co=10µF(Ceramic)
Output Voltage:V_OUT(V)
Output Current:I_OUT(A)
Time:t(µs)