

## Low Dropout Voltage Regulator with Reset

### ■ GENERAL DISCRIPTION

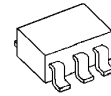
The NJU7272 is a low drop out voltage regulator with input-monitor reset function with delay.

Advanced CMOS technology achieves ultra low current consumption and high accuracy.

It delivers up to 5V/100mA output power with the maximum input voltage of 9V.

The NJU7272 suitable for MPU applications.

### ■ PACKAGE OUTLINE

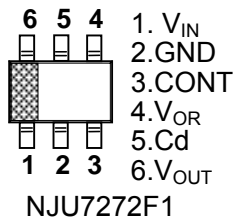


NJU7272F1

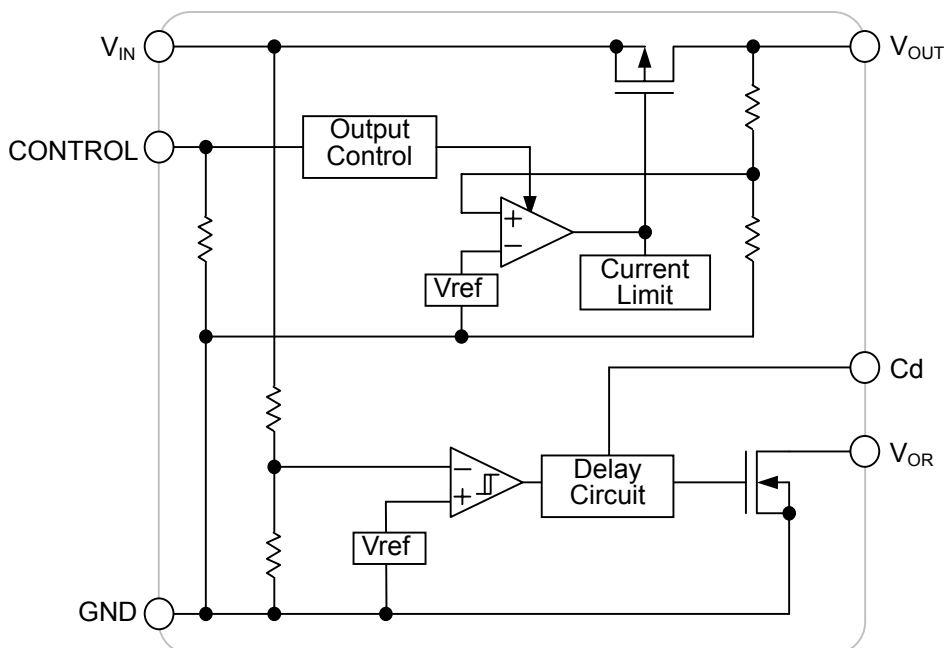
### ■ FEATURES

- Ultra Low Quiescent Current  $I_q = 3.5\mu\text{A typ. (I}_o = 0\text{mA)}$
- Output Voltage Accuracy  $V_o = \pm 1.0\%$
- Reset Voltage Accuracy  $V_{RT} = \pm 1.0\%$
- Input Voltage Monitor type
- Adjustable delay time with external capacitor
- Output Current  $I_o(\text{max.}) = 100\text{mA}$
- Output capacitor with 0.1 $\mu\text{F}$  ceramic capacitor
- Nch Open Drain Output
- Internal Short Circuit Current Limit
- CMOS Technology
- Package Outline SOT-23-6

### ■ PIN CONFIGURATION



### ■ EQUIVALENT CIRCUIT



# NJU7272

## ■ OUTPUT VOLTAGE/ DETECTION VOLTAGE

Device Name	Output Voltage	Detection Voltage
NJU7272F1-1502A	1.5V	2.0V
NJU7272F1-3342A	3.3V	4.2V
NJU7272F1-0555A	5.0V	5.5V

Output voltage options available : 1.8 ~ 5.0V (0.1V step)

Detection voltage options available : 1.3 ~ 4.5V (0.1V step)

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	$V_{IN}$	+11	V
Control Voltage	$V_{CONT}$	+11	V
Cd Pin Input Voltage	$V_{Cd}$	+11	V
$V_{OR}$ Pin Output Voltage	$V_{OR}$	GND - 0.3 ~ +11	V
$V_{OR}$ Pin Output Current	$I_{OR}$	50	mA
Power Dissipation	$P_D$	200(*1) 400(*2)	mW
Operating Temperature Range	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +125	°C

(\*1): Device itself

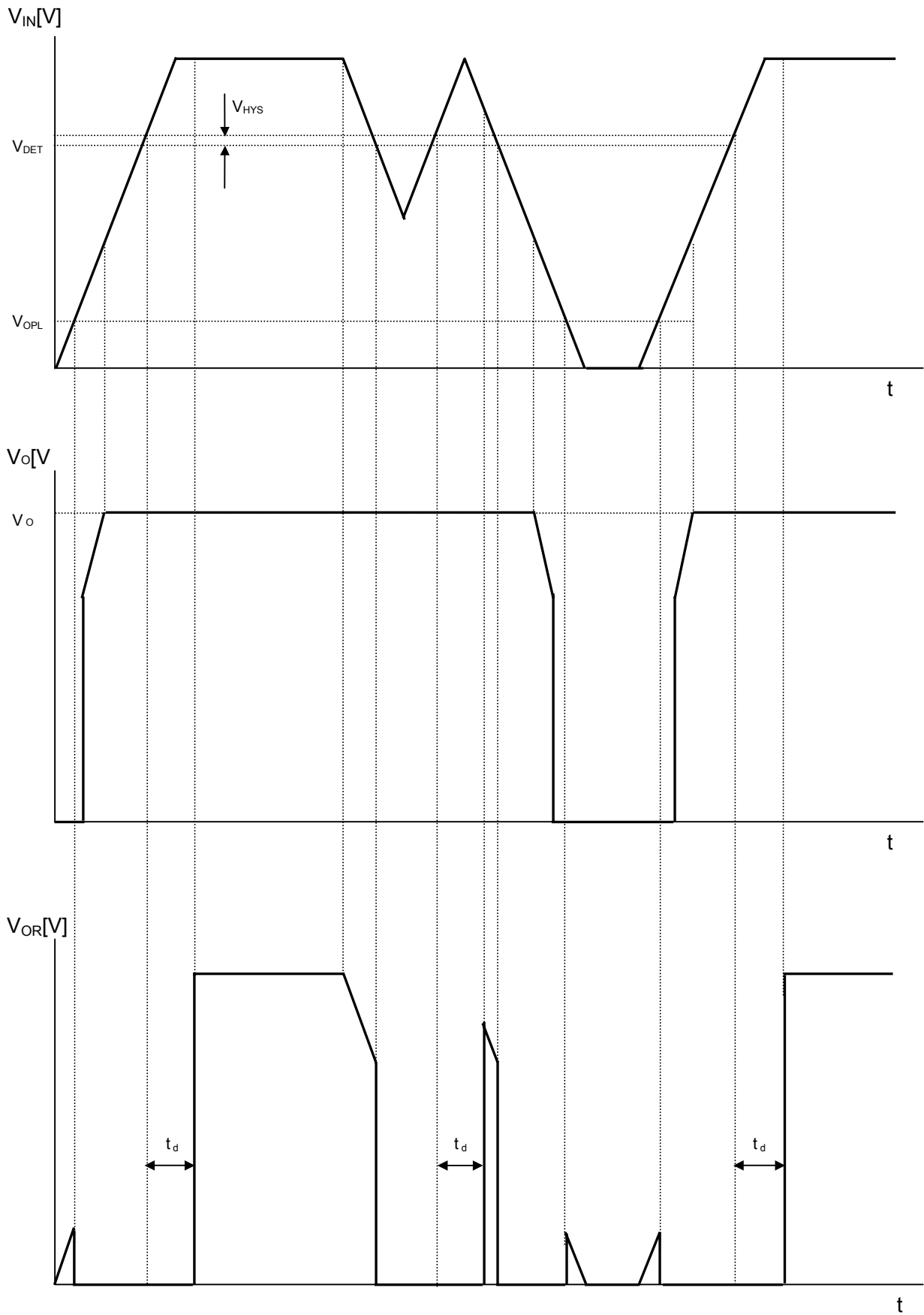
(\*2): Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers)

■ ELECTRICAL CHARACTERISTICS ( $V_{IN}=V_O+1$ ,  $C_{IN}=0.1\mu F$ ,  $C_O=0.1\mu F$ ,  $T_a=25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
<b>General Characteristics</b>							
Quiescent Current	$I_Q$	$V_{IN}=V_O+2$ , $V_{CONT}=V_{IN}$ , $I_O=0mA$	-	3.5	8.2	$\mu A$	
Quiescent Current at Control OFF	$I_{Q(OFF)}$	$V_{IN}=V_O+2$ , $V_{CONT}=0V$ , $I_O=0mA$	-	1.0	2.0	$\mu A$	
<b>Regulator Block</b>							
Output Voltage	$V_O$	$I_O=30mA$	-1.0%	-	+1.0%	V	
Output Current	$I_O$	$V_O - 0.3V$	100	-	-	mA	
Line Regulation	$\Delta V_O/\Delta V_{IN}$	$V_{IN}=V_O+1V \sim V_O+6V (V_O < 3.0V)$ $V_{IN}=V_O+1V \sim 9V (V_O \geq 3.0V)$ $I_O=30mA$	-	-	0.3	%/V	
Load Regulation	$\Delta V_O/\Delta I_O$	$I_O=0 \sim 100mA$	-	-	0.15	%/mA	
Output Voltage Temperature Coefficient	$\Delta V_O/\Delta T_a$	$T_a=0 \sim 85^\circ C$ , $I_O=10mA$	-	$\pm 100$	-	ppm/ $^\circ C$	
Control Voltage for ON-State	$V_{CONT(ON)}$		1.6	-	$V_{IN}$	V	
Control Voltage for OFF-State	$V_{CONT(OFF)}$		0	-	0.3	V	
Pull-down Resistance	$R_{CONT}$		2	5	10	M $\Omega$	
Short Circuit Limit	$I_{LIM}$	$V_O=0V$	-	25	-	mA	
Input Voltage	$V_{IN}$		-	-	9	V	
Dropout Voltage	$\Delta V_{I-O}$	$I_O=40mA$	$1.5V \leq V_O \leq 2.0V$	-	0.19	0.60	V
			$2.1V \leq V_O \leq 2.4V$	-	0.19	0.29	V
		$I_O=60mA$	$2.5V \leq V_O \leq 2.7V$	-	0.18	0.27	V
			$2.8V \leq V_O \leq 3.3V$	-	0.17	0.26	V
			$3.4V \leq V_O \leq 5.0V$	-	0.16	0.24	V
			$5.1V \leq V_O \leq 6.0V$	-	0.15	0.22	V
<b>Reset Block</b>							
Detection Voltage	$V_{DET}$		-1.0%	-	+1.0%	V	
Hysteresis Voltage	$V_{HYS}$		70	90	130	mV	
$V_{OR}$ Pin Output Current	$I_{OR}$	$Nch$ , $V_{DS}=0.5V$ $V_{CONT}=0V$	$V_{IN}=1.2V$ 0.75 $V_{IN}=2.4V$ 4.50 ( $V_{DET} \geq 2.7V$ Version)	2.00	-	mA	
Output Leak Current	$I_{LEAK}$	$V_{IN}=V_{OR}=V_{CONT}=9V$	-	-	0.1	$\mu A$	
Detection Voltage Temperature Coefficient	$\Delta V_{DET}/\Delta T_a$	$T_a=0 \sim 85^\circ C$	-	$\pm 100$	-	ppm/ $^\circ C$	
Delay Time	$t_d$	$V_{IN}=V_{DET} + 1$ , $C_d=4.7nF$	8	10	12	ms	
Operating Voltage(*4)	$V_{OPL}$	$R_L=100k\Omega$	-	-	0.8	V	

(\*3): The value condition that  $V_{OR}$  become 10% or less of  $V_{IN}$ .

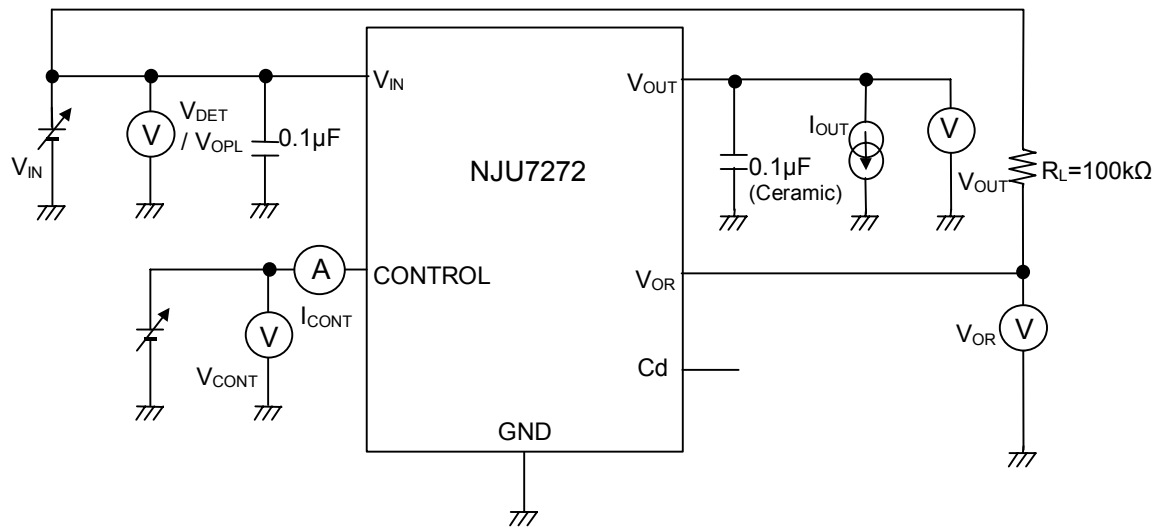
## ■ TIMING CHART



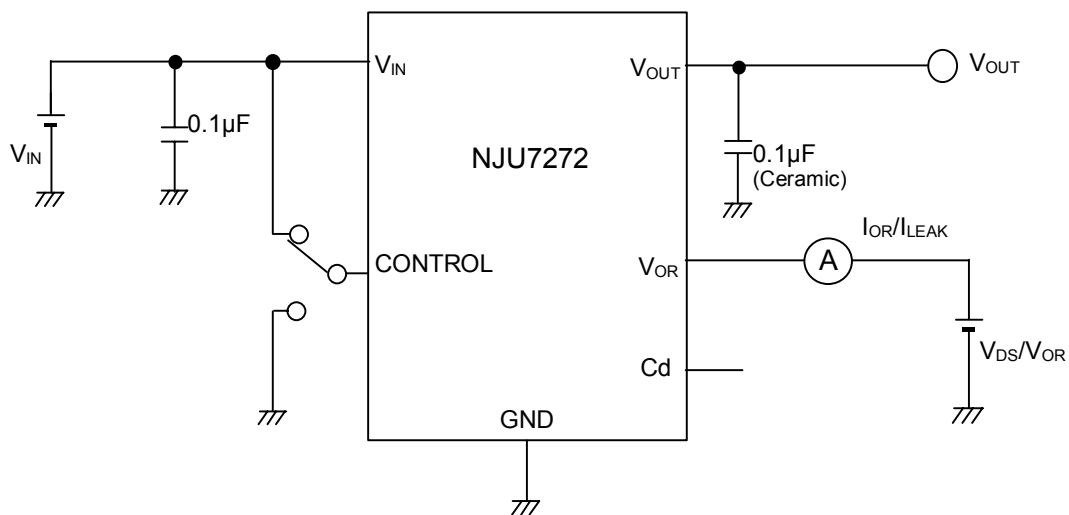
\*  $V_{OR}$  is the case where a pull-up is carried out to  $V_{IN}$  through resistance.

## ■ TEST CIRCUIT

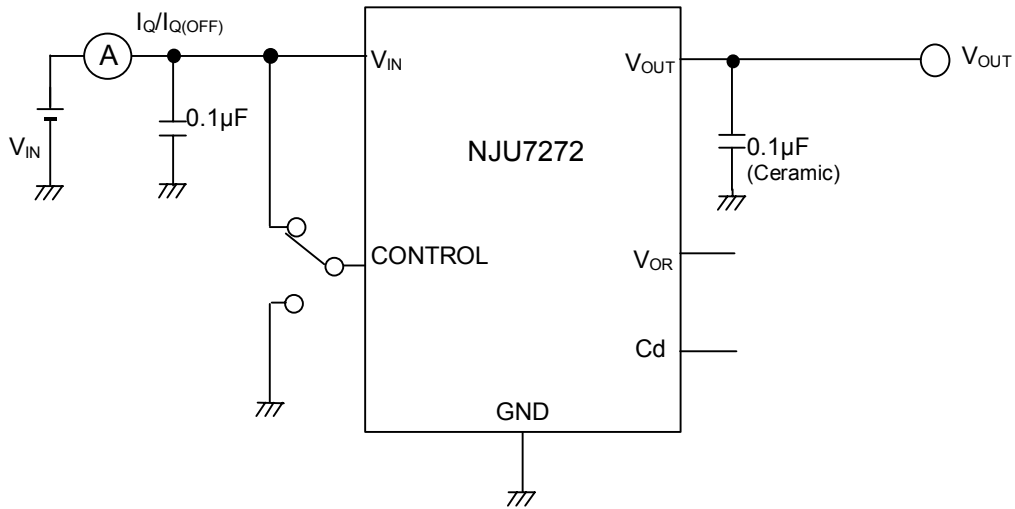
### ① COMMON TEST CIRCUIT



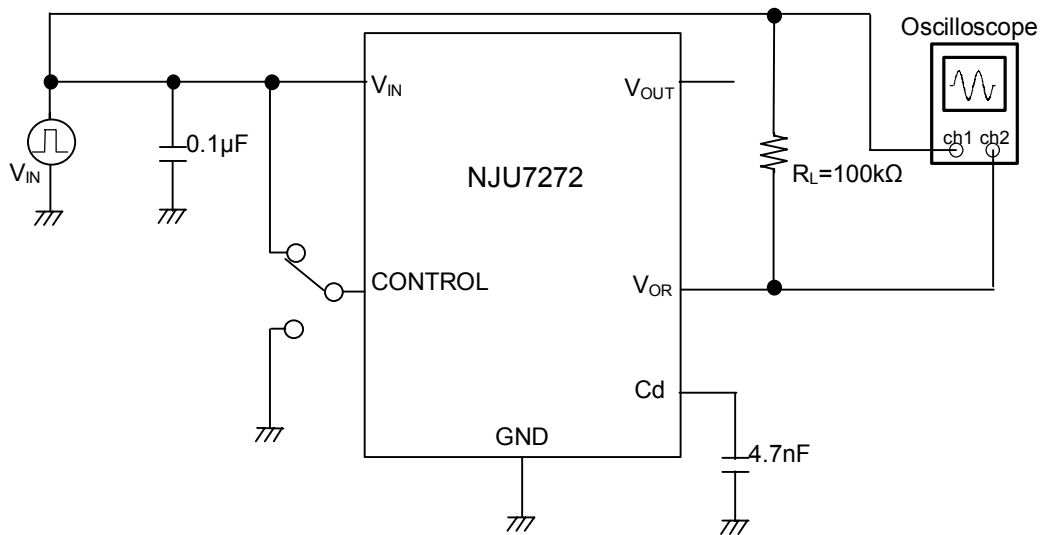
### ② OUTPUT CURRENT/OUTPUT LEAK CURRENT TEST CIRCUIT



## ③ QUIESCENT CURRENT TEST CIRCUIT

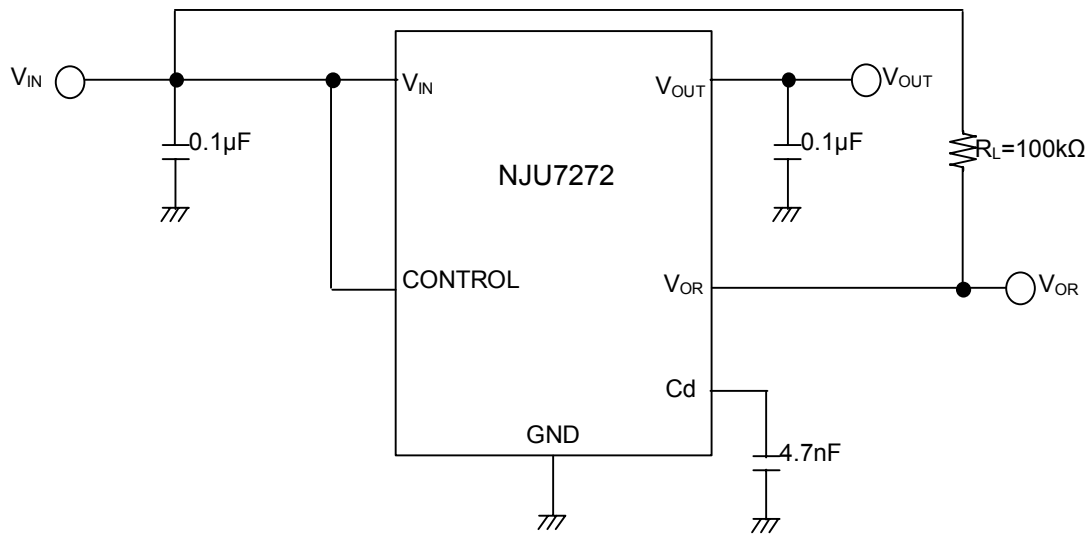


## ④ DELAY TIME TEST CIRCUIT



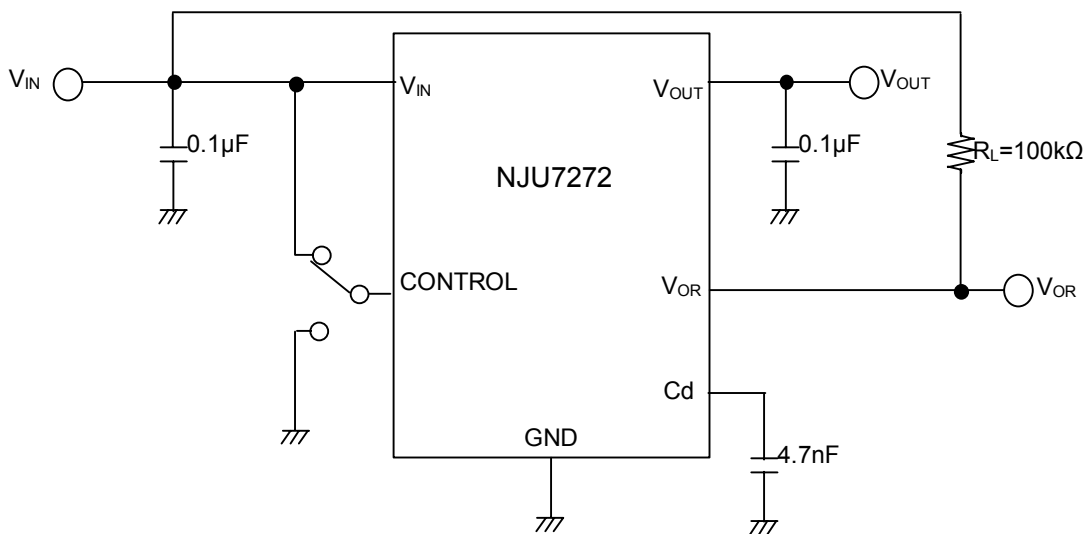
## ■ TYPICAL APPLICATION

① In case that ON/OFF Control is not required:



Connect control terminal to  $V_{IN}$  terminal.

② In use of ON/OFF Control:



State of control terminal:

- "H" → output is enabled.
- "L" or "open" → output is disabled.

## \*Input Capacitance $C_{IN}$

Input Capacitance  $C_{IN}$  is required to prevent oscillation and reduce power supply ripple for applications with high power supply impedance or a long power supply line.

Use the  $C_{IN}$  value of  $0.1\mu\text{F}$  greater to avoid the problem.

$C_{IN}$  should connect between GND and  $V_{IN}$  as short as possible.

## \*Output Capacitance $C_o$

Output capacitor ( $C_o$ ) is required for a phase compensation of the internal error amplifier. The capacitance and the equivalent series resistance (ESR) influence stability of the regulator.

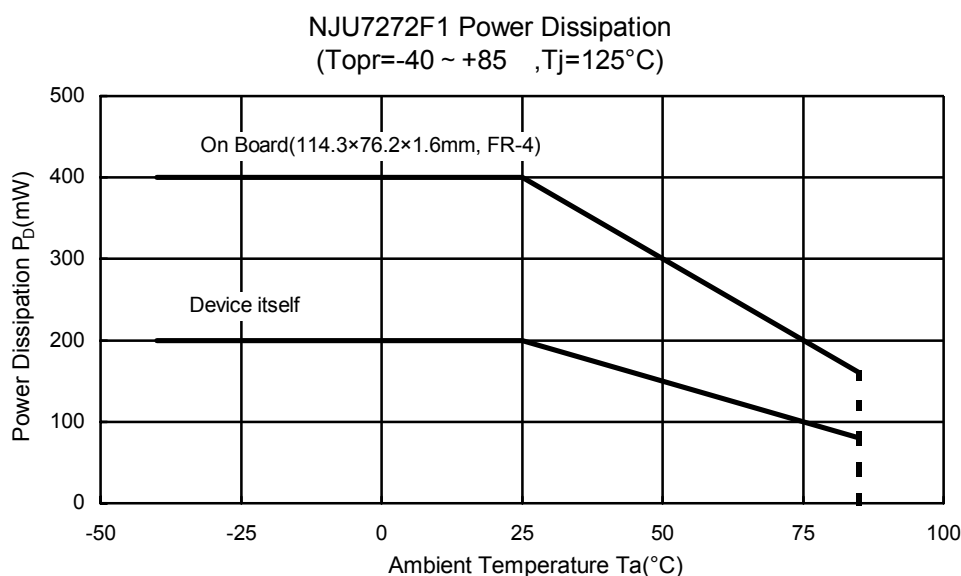
If use a smaller  $C_o$ , it may cause excess output noise or oscillation of the regulator due to lack of the phase compensation. Therefore, use  $C_o$  with the recommended capacitance or greater value and connect between  $V_o$  terminal and GND terminal with minimal wiring.

The recommended capacitance depends on the output voltage. Low voltage regulator requires greater value of the  $C_o$ . Thus, check the recommended capacitance for each output voltage.

Use of a greater  $C_o$  reduces output noise and ripple output, and also improves transient response of the output voltage against rapid load change.

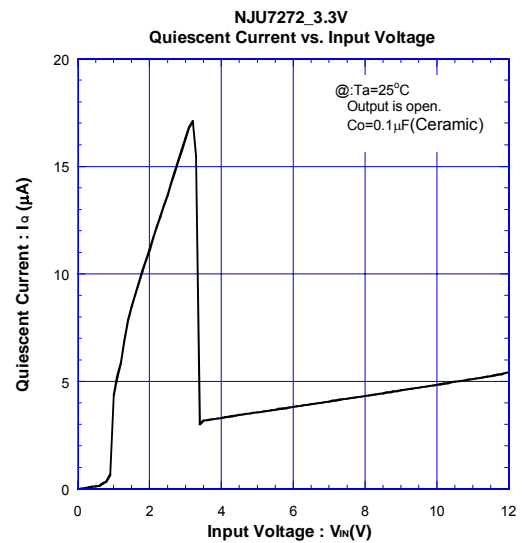
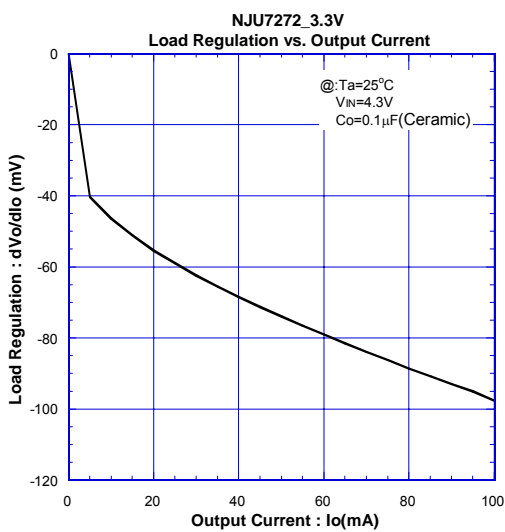
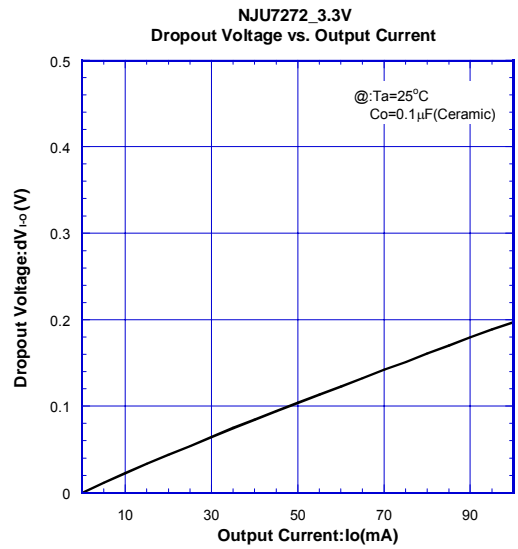
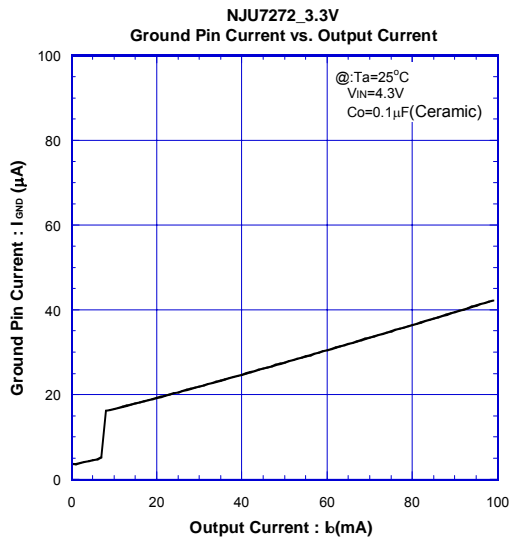
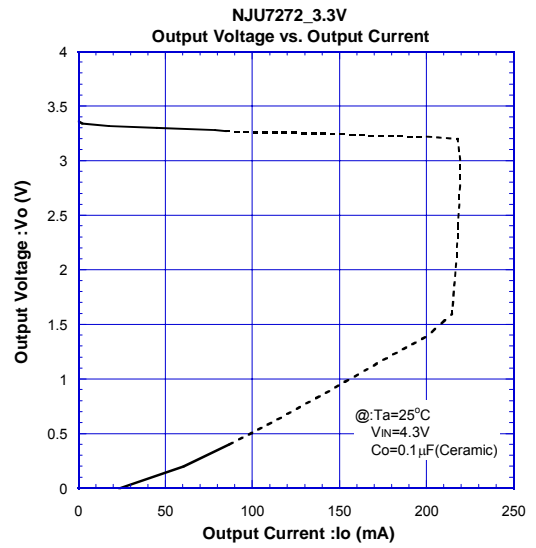
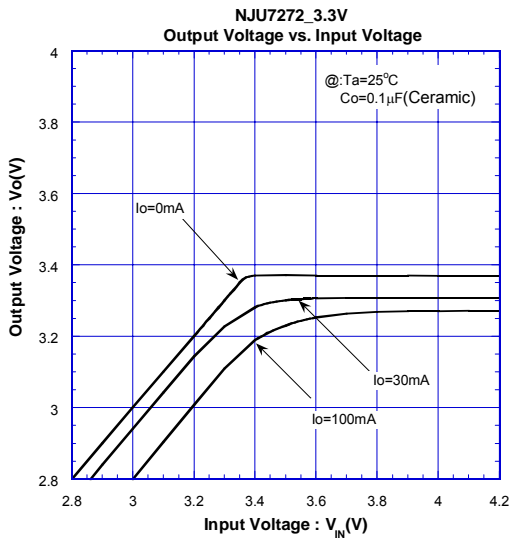
This product is designed to work with any capacitor including a low ESR capacitor for the  $C_o$ ; however, refer "Equivalent Series Resistance vs. Output Current" and choose suitable capacitor.

## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

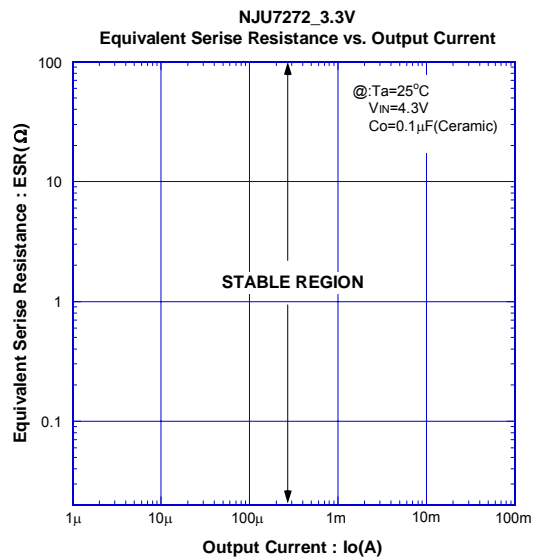
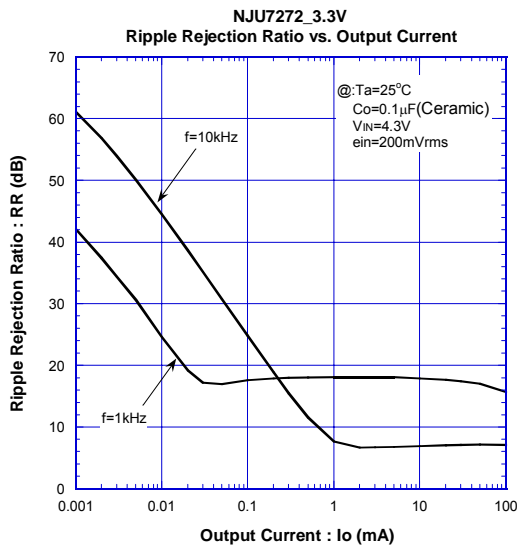
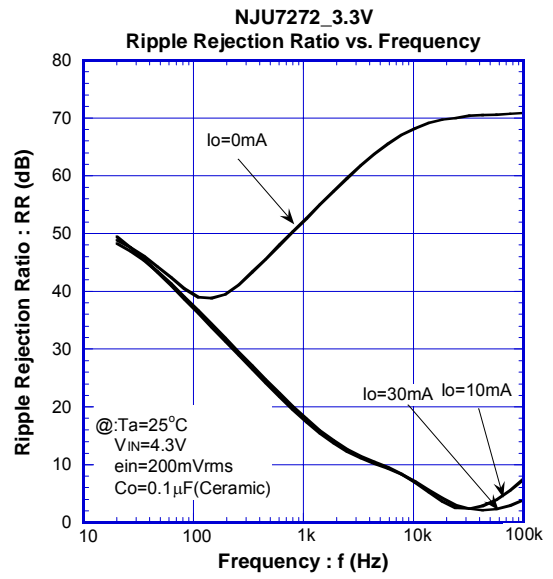
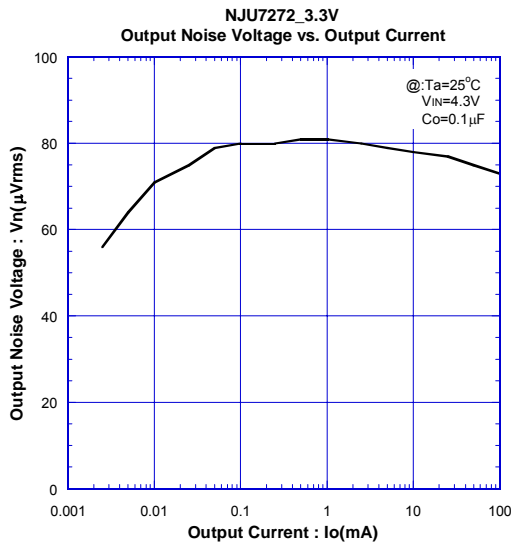




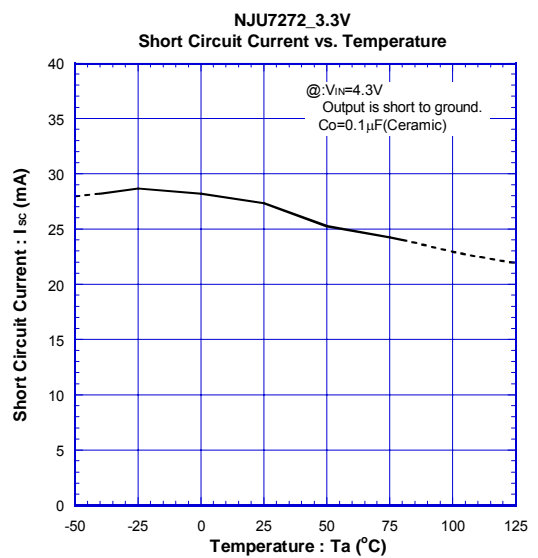
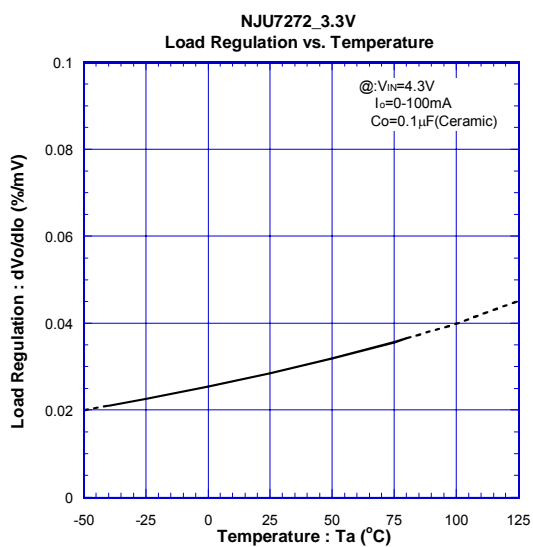
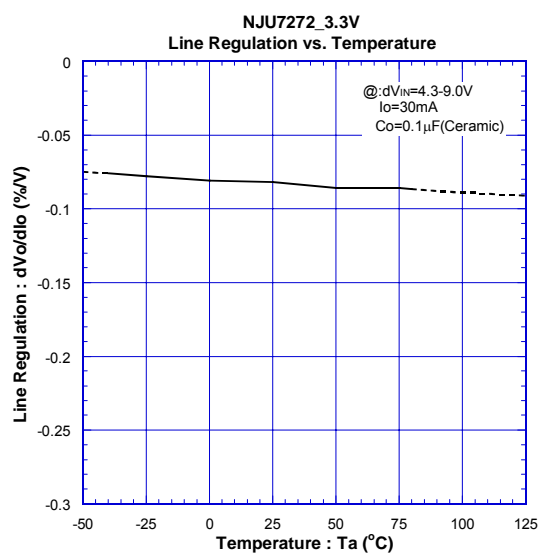
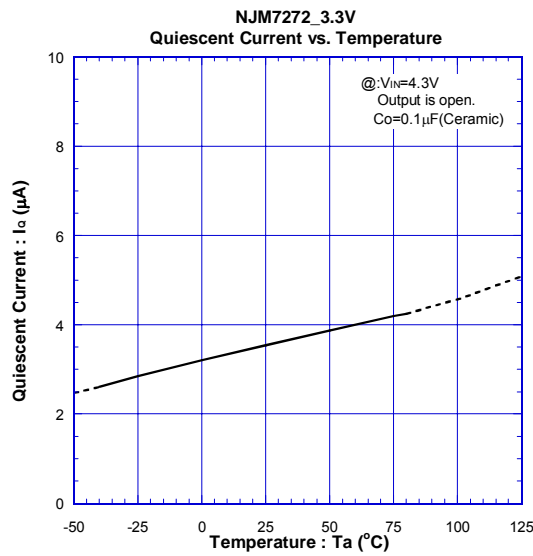
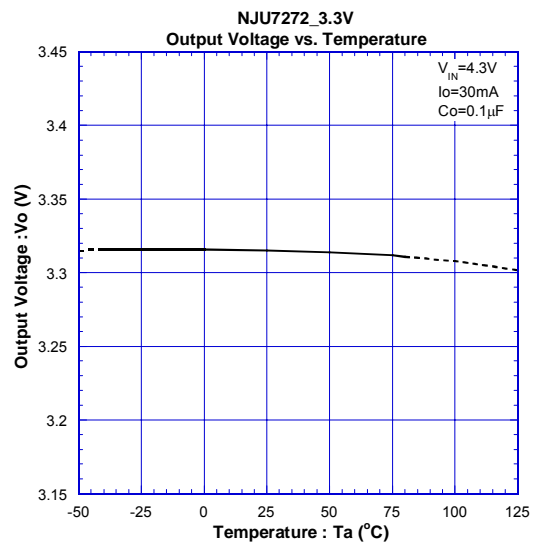
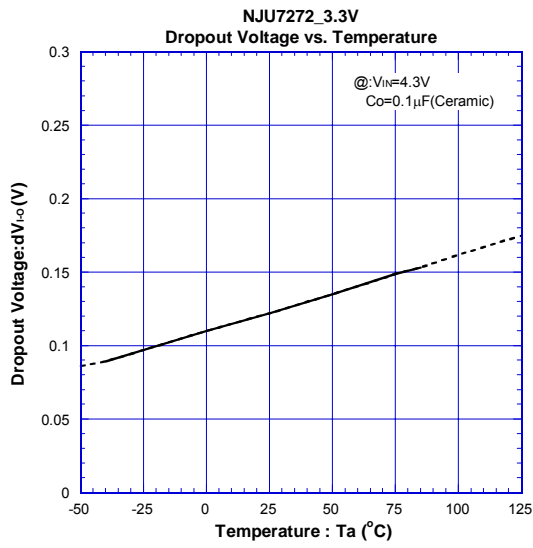
## ■ TYPICAL CHARACTERISTICS (LDO BLOCK)



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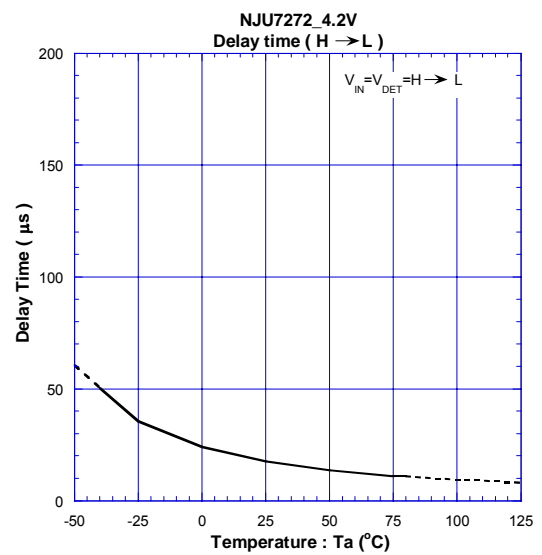
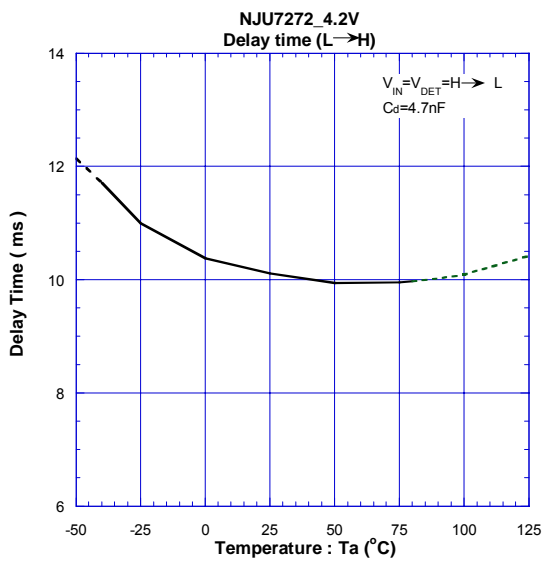
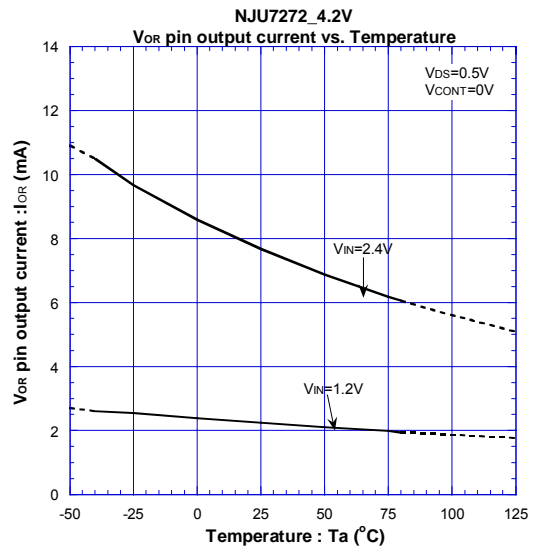
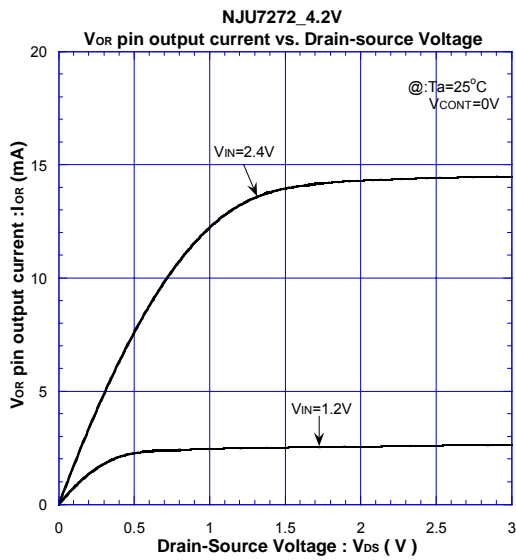
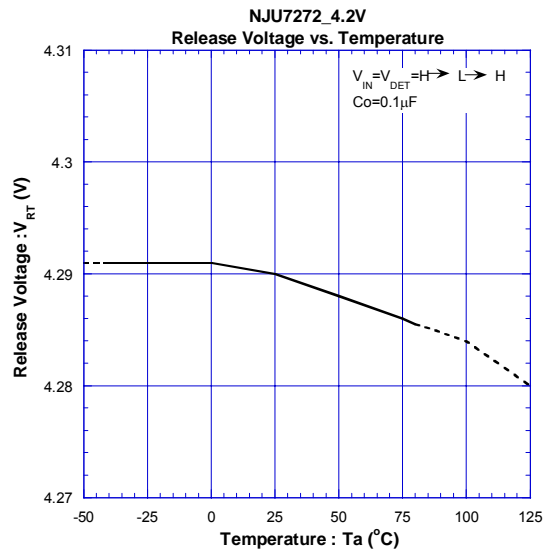
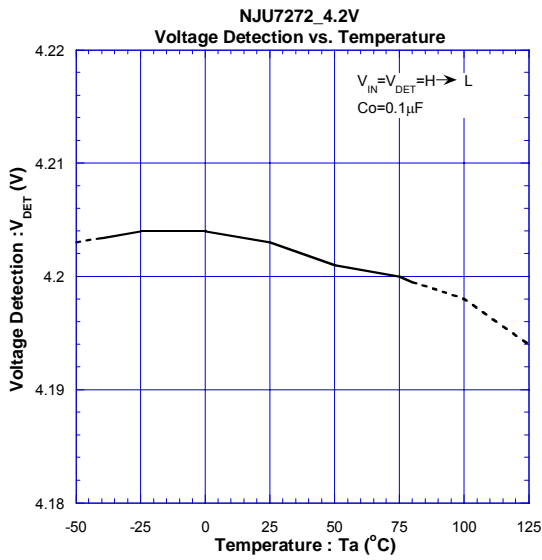


## ■ TYPICAL CHARACTERISTICS (LDO BLOCK)



# NJU7272

## ■ TYPICAL CHARACTERISTICS (RESET BLOCK)



[CAUTION]

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