SDRAM

512K x 32 Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

ORDERING INFORMATION

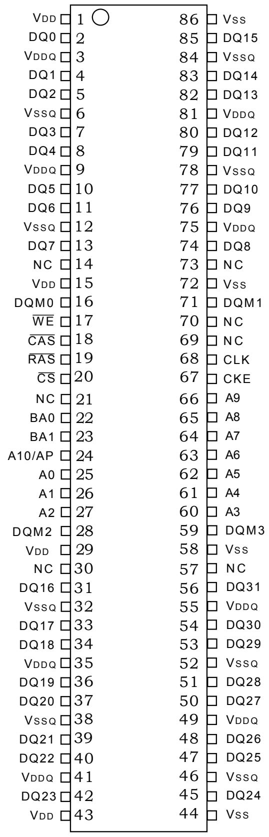
Product ID	Max Freq.	Package	Comments
M12L64322A-5TIG2S	200MHz	86 TSOPII	Pb-free
M12L64322A-6TIG2S	166MHz	86 TSOPII	Pb-free
M12L64322A-7TIG2S	143MHz	86 TSOPII	Pb-free
M12L64322A-5BIG2S	200MHz	90 BGA	Pb-free
M12L64322A-6BIG2S	166MHz	90 BGA	Pb-free
M12L64322A-7BIG2S	143MHz	90 BGA	Pb-free

GENERAL DESCRIPTION

The M12L64322A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 524,288 words by 32 bits. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

BALL CONFIGURATION (TOP VIEW)

(TSOPII 86L, 400milX875mil Body, 0.5mm Pin Pitch)

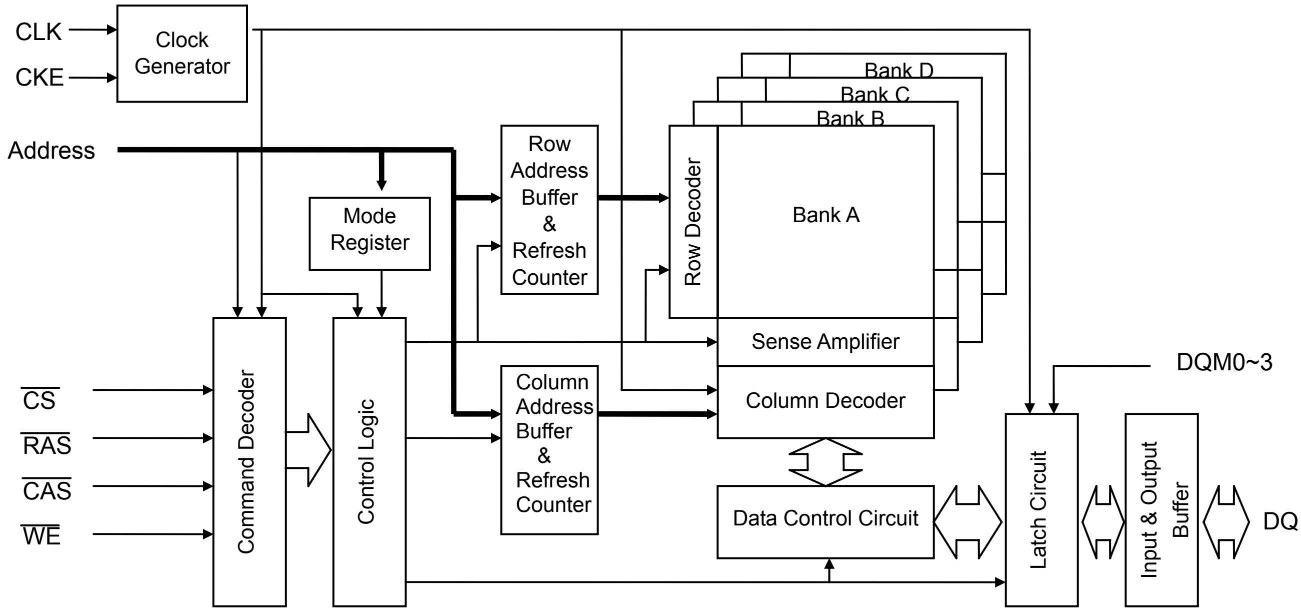


BALL CONFIGURATION (TOP VIEW)

(BGA 90, 8mmX13mmX1mm Body, 0.8mm Ball Pitch)

	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	VSS				VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ				VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25				DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30				DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC				NC	DQ16	VSSQ
F	VSS	DQM3	A3				A2	DQM2	VDD
G	A4	A5	A6				A10	A0	A1
H	A7	A8	NC				NC	BA1	NC
J	CLK	CKE	A9				BA0	$\overline{CS}$	$\overline{RAS}$
K	DQM1	NC	NC				$\overline{CAS}$	$\overline{WE}$	DQM0
L	VDDQ	DQ8	VSS				VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9				DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14				DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ				VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS				VDD	DQ0	DQ2

BLOCK DIAGRAM



PIN DESCRIPTION

PIN	NAME	INPUT FUNCTION
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM0-3.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby.
A0 ~ A10/AP	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA10, column address : CA0~CA7
BA0 , BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0~3	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ DQ31	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
V_{DD} / V_{SS}	Power Supply / Ground	Power and ground for the input buffers and the core logic.
V_{DDQ} / V_{SSQ}	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Operating ambient temperature	T_A	-40 ~ +85	℃
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITION

Recommended operating conditions (Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD} + 0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	μA	3
Output leakage current	I_{OL}	-5	-	5	μA	4

Note:

1. V_{IH}(max) = 4.6V AC for pulse width $\leq$ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width $\leq$ 10ns acceptable.
3. Any input 0V $\leq V_{IN} \leq V_{DD}$, all other pins are not under test = 0V.
4. Dout is disabled, 0V $\leq V_{OUT} \leq V_{DD}$.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25 °C , f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A10, BA0 ~ BA1)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ0 ~ DQ31)	C_{OUT}	2	6	pF

DC CHARACTERISTICS

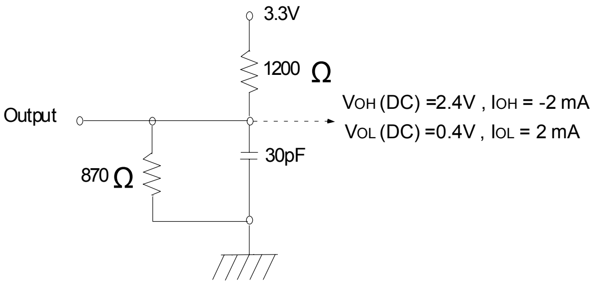
Recommended operating condition unless otherwise noted

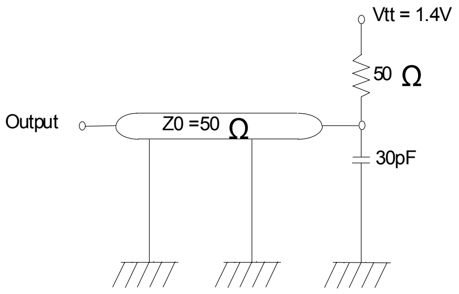
Parameter	Symbol	Test Condition	Version			Unit	Note
			-5	-6	-7		
Operating Current (One Bank Active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC}$ (min), $t_{CC} \geq t_{CC}$ (min), I_{OL}= 0mA	180	160	140	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE $\leq V_{IL}$(max), t_{CC} = 15ns	2			mA	
	I_{CC2PS}	CKE & CLK $\leq V_{IL}$(max), t_{CC} = ∞	2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 15ns Input signals are changed one time during 30ns	30			mA	
	I_{CC2NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), t_{CC} = ∞ input signals are stable	10				
Active Standby Current in power-down mode	I_{CC3P}	CKE $\leq V_{IL}$(max), t_{CC} = 15ns	10			mA	
	I_{CC3PS}	CKE & CLK $\leq V_{IL}$(max), t_{CC} = ∞	10				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE $\geq V_{IH}$ (min), $\overline{CS} \geq V_{IH}$ (min), t_{CC}=15ns Input signals are changed one time during 2clks All other pins $\geq V_{DD}$-0.2V or $\leq$ 0.2V	40			mA	
	I_{CC3NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), t_{CC} = ∞ input signals are stable	10			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL}= 0mA, Page Burst All Band Activated, t_{CCD} = t_{CCD} (min)	280	260	240	mA	1
Refresh Current	I_{CC5}	$t_{RFC} \geq t_{RFC}$(min)	330	310	290	mA	2
Self Refresh Current	I_{CC6}	CKE $\leq$ 0.2V	2			mA	

Note: 1.Measured with outputs open. Addresses are changed only one time during t_{CC}(min).
2.Refresh period is 64ms. Addresses are changed only one time during t_{CC}(min).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall-time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	





OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-5	-6	-7		
Row active to row active delay		t_{RRD}(min)	10	12	14	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	15	18	21	ns	1
Row precharge time		t_{RP}(min)	15	18	21	ns	1
Row active time		t_{RAS}(min)	40	42	42	ns	1
		t_{RAS}(max)	100			us	
Row cycle time	@ Operating	t_{RC}(min)	55	60	63	ns	1
	@ Auto refresh	t_{RFC}(min)	55	60	63	ns	1, 5
Last data in to col. address delay		t_{CDL}(min)	1			CLK	2
Last data in to row precharge		t_{RDL}(min)	2			CLK	2
Last data in to burst stop		t_{BDL}(min)	1			CLK	2
Col. address to col. address delay		t_{CCD}(min)	1			CLK	3
Refresh period (4,096 rows)		t_{REF}(max)	64			ms	6
Number of valid Output data	CAS latency = 3		2			ea	4
	CAS latency = 2		1				

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.
6. A maximum of eight consecutive AUTO REFRESH commands (with t_{RFC}(min)) can be posted to any given SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8x15.6 μ s.

AC CHARACTERISTICS (AC operating condition unless otherwise noted)

Parameter		Symbol	-5		-6		-7		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency = 3	t_{CC}	5	1000	6	1000	7	1000	ns	1
	CAS latency = 2		10		10		10			
CLK to valid output delay	CAS latency = 3	t_{SAC}		5		5		6	ns	1,2
	CAS latency = 2			6		7		8		
Output data hold time	CAS latency = 3	t_{OH}	2		2		2		ns	2
	CAS latency = 2		2		2		2			
CLK high pulse width		t_{CH}	2		2		2.5		ns	3
CLK low pulse width		t_{CL}	2		2		2.5		ns	3
Input setup time		t_{SS}	1.5		2		2		ns	3
Input hold time		t_{SH}	1		1		1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency = 3	t_{SHZ}		5		5		6	ns	
	CAS latency = 2			6		7		8		

Note: 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns. (tr/2 - 0.5) ns should be considered.
3. Assumed input rise and fall time (tr & tf) =1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered.
i.e., [(tr + tf)/2 – 1] ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A9~A0	Note
Register	Mode Register set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
DQM			H	X					V	X			7
No Operating Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V = Valid, X = Don't Care. H = Logic High, L = Logic Low)

Note: 1.OP Code: Operating Code
A0~A10 & BA0~BA1: Program keys. (@ MRS)
2.MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3.Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge of command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4.BA0~BA1 : Bank select addresses.
If both BA1 and BA0 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA1 is "Low" and BA0 is "High" at read, write, row active and precharge, bank B is selected.
If both BA1 is "High" and BA0 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA1 and BA0 are "High" at read, write, row active and precharge, bank D is selected
If A10/AP is "High" at row precharge, BA1 and BA0 is ignored and all banks are selected.
5.During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6.Burst stop command is valid at every burst length.
7.DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after.(Read DQM latency is 2)

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA0~BA1	A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode			**CAS Latency**				**Burst Type**		**Burst Length**				
A8	**A7**	**Type**	**A6**	**A5**	**A4**	**Latency**	**A3**	**Type**	**A2**	**A1**	**A0**	**BT = 0**	**BT = 1**
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	**Length**		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length: 256

Note: 1. RFU (Reserved for future use) should stay “0” during MRS cycle.

2. If A9 is high during MRS cycle, “Burst Read single Bit Write” function will be enabled.

3. The full column burst (256 bit) is available only at sequential mode of burst type.

BURST SEQUENCE (BURST LENGTH = 4)

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around positive edge of the clock for proper functionality and I_{CC} specifications.

CLOCK ENABLE(CKE)

The clock enable (CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + t_{SS}" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESSES (BA0~BA1)

This SDRAM is organized as four independent banks of 524,288 words x 32 bits memory arrays. The BA0~BA1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The banks addressed BA0~BA1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0~A10)

The 19 address bits are required to decode the 524,288 word locations are multiplexed into 11 address input pins (A0~A10). The 11 row addresses are latched along with $\overline{RAS}$ and BA0~BA1 during bank active command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA0~BA1 during read or with command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high , The SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE = "H", DQM = "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

   The device is now ready for normal operation.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A10 and BA0~BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields into depending on functionality. The burst length field uses A0~A2, burst type uses A3, CAS latency (read latency from column address) use A4~A6, vendor specific options or test mode use A7~A8, A10/AP and BA0~BA1. The write burst length is programmed using A9. A7~A9, A10/AP and BA0~BA1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD} (min) from the time of bank activation. t_{RCD} is the internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD} (min) with cycle time of the clock and then rounding of the result to the next higher integer.

DEVICE OPERATIONS (Continued)

The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. t_{RRD} (min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} (min) specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS} (min). Every SDRAM bank activate command must satisfy t_{RAS} (min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS} (max) and t_{RAS} (max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD} (min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be complete by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DQM OPERATION

The DQM is used mask input and output operations. It works similar to $\overline{OE}$ during operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge is performed on an active bank by asserting low on clock cycles required between bank activate and clock cycles required between bank activate and $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A10/AP with valid BA0~BA1 of the bank to be procharged. The precharge command can be asserted anytime after t_{RAS} (min) is satisfy from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS} (max). Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to power-down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS} (min) and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst write by asserting high on A10/AP, the bank is precharge command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

ALL BANKS PRECHARGE

Four banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A10/AP after all banks have satisfied t_{RAS} (min) requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge all, all banks are in idle state.

DEVICE OPERATIONS (Continued)

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with all banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by t_{RFC} (min). The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us.

SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.

The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the refresh.

The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation. 4K cycles of burst auto refresh is required immediately before self refresh entry and immediately after self refresh exit.

COMMANDS

Mode register set command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = Low)

The device has a mode register that defines how the device operates. In this command, A0 through A10 and BA0~BA1 are the data input pins. After power on, the mode register set command must be executed to initialize the device.
The mode register can be set only when all banks are in idle state.
During 2CLK following this command, the device cannot accept any other commands.

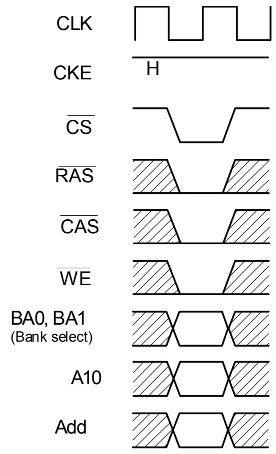


Fig. 1 Mode register set command

Activate command

($\overline{CS}$, $\overline{RAS}$ = Low, $\overline{CAS}$, $\overline{WE}$ = High)

The device has four banks, each with 2,048 rows.
This command activates the bank selected by BA1 and BA0 and a row address selected by A0 through A10.

This command corresponds to a conventional DRAM's $\overline{RAS}$ falling.

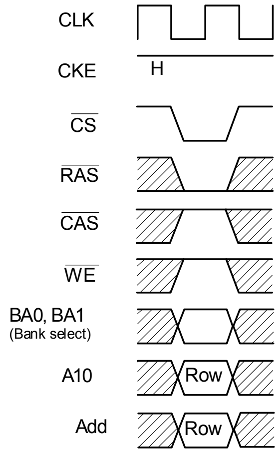


Fig. 2 Row address stroble and bank active command

Precharge command

($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ = Low, $\overline{CAS}$ = High)

This command begins precharge operation of the bank selected by BA1 and BA0. When A10 is High, all banks are precharged, regardless of BA1 and BA0. When A10 is Low, only the bank selected by BA1 and BA0 is precharged.
After this command, the device can't accept the activate command to the precharging bank during t_{RP} (precharge to activate command period).

This command corresponds to a conventional DRAM's $\overline{RAS}$ rising.

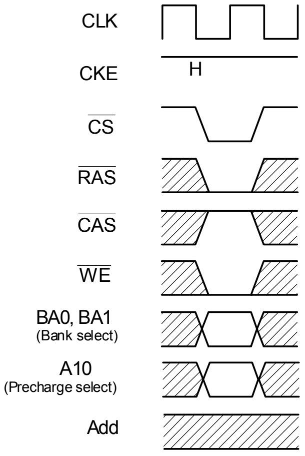


Fig. 3 Precharge command

Write command

($\overline{\text{CS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ = Low, $\overline{\text{RAS}}$ = High)

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst can be input with this command with subsequent data on following clocks.

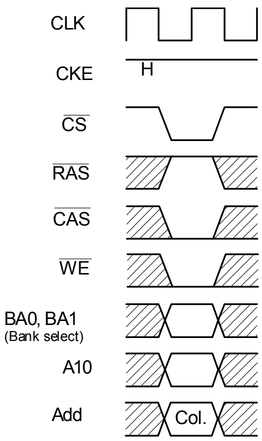


Fig. 4 Column address and write command

Read command

($\overline{\text{CS}}$, $\overline{\text{CAS}}$ = Low, $\overline{\text{RAS}}$, $\overline{\text{WE}}$ = High)

Read data is available after $\overline{\text{CAS}}$ latency requirements have been met.
This command sets the burst start address given by the column address.

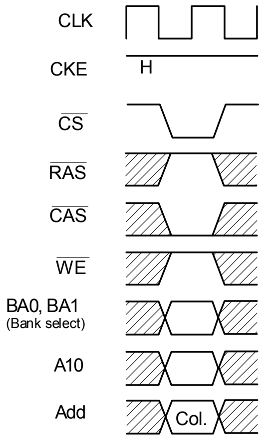


Fig. 5 Column address and read command

CBR (auto) refresh command

($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = Low, $\overline{\text{WE}}$, CKE = High)

This command is a request to begin the CBR refresh operation. The refresh address is generated internally.
Before executing CBR refresh, all banks must be precharged.
After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command.
During t_{RFC} period (from refresh command to refresh or activate command), the device cannot accept any other command.

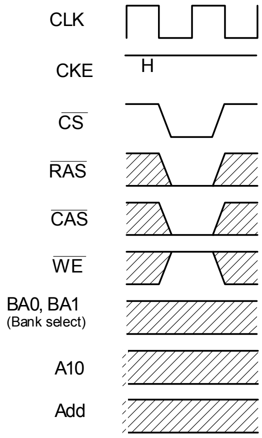


Fig. 6 Auto refresh command

Self refresh entry command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, CKE = Low , $\overline{WE}$ = High)

After the command execution, self refresh operation continues while CKE remains low. When CKE goes to high, the device exits the self refresh mode.
During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.
Before executing self refresh, all banks must be precharged.

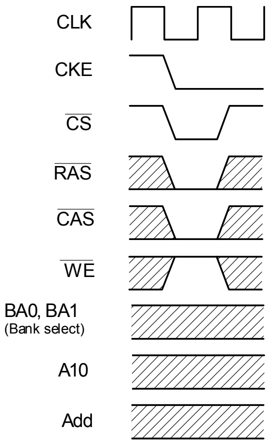


Fig. 7 Self refresh entry command

Burst stop command

($\overline{CS}$, $\overline{WE}$ = Low, $\overline{RAS}$, $\overline{CAS}$ = High)

This command terminates the current burst operation.
Burst stop is valid at every burst length.

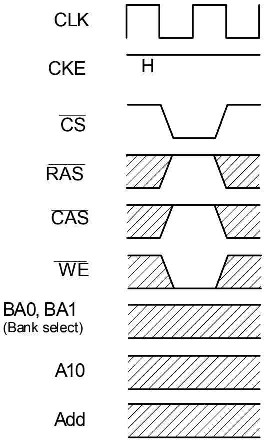


Fig. 8 Burst stop command

No operation

($\overline{CS}$ = Low , $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = High)

This command is not an execution command. No operations begin or terminate by this command.

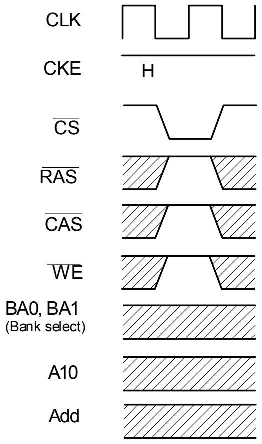
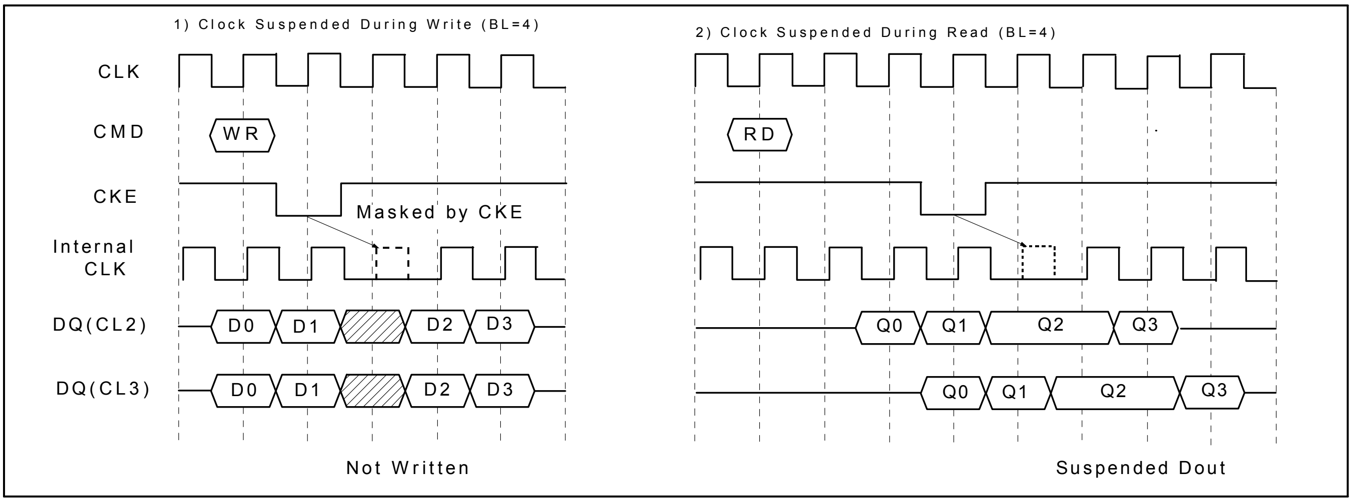


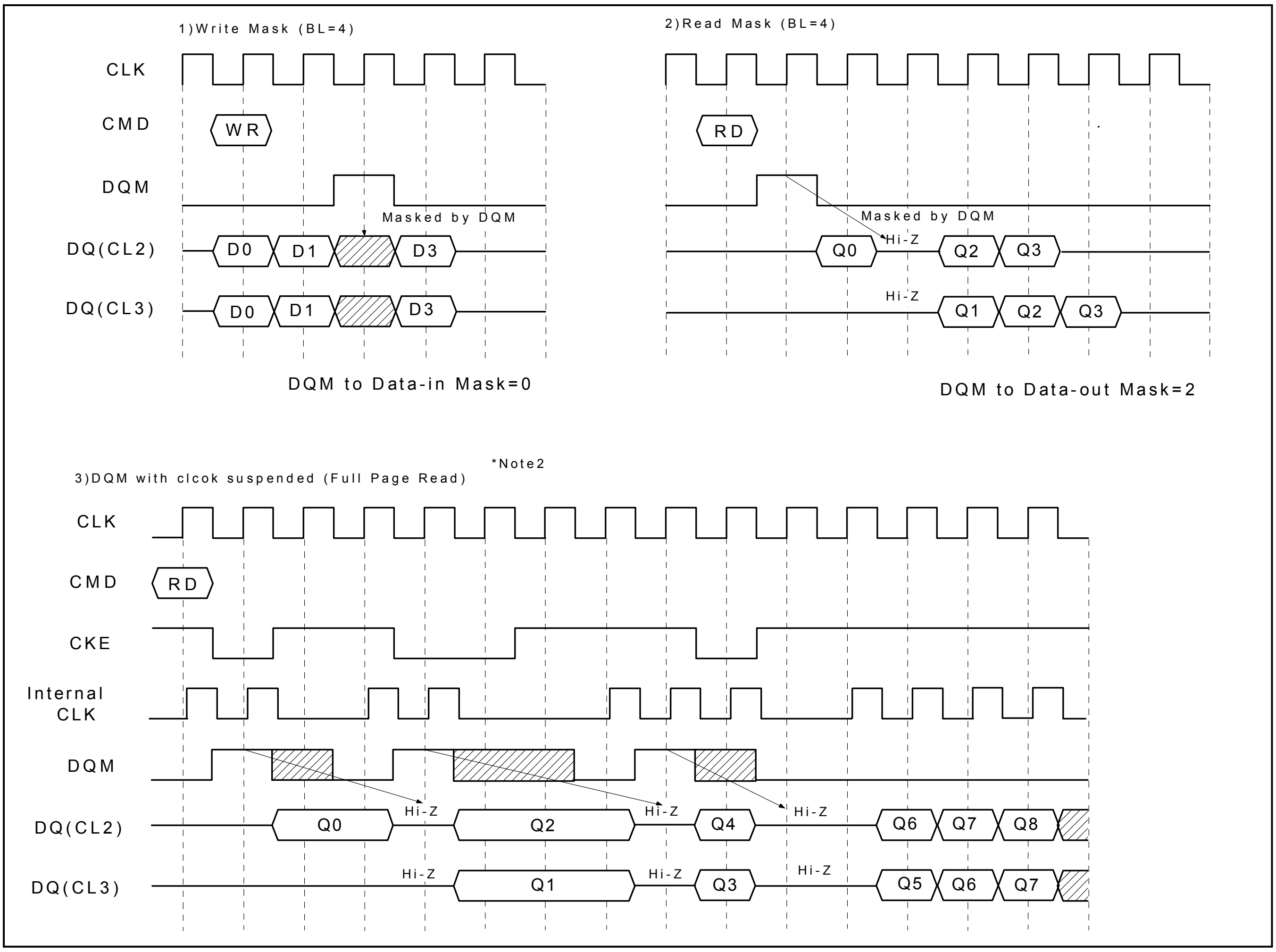
Fig. 9 No operation

BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend

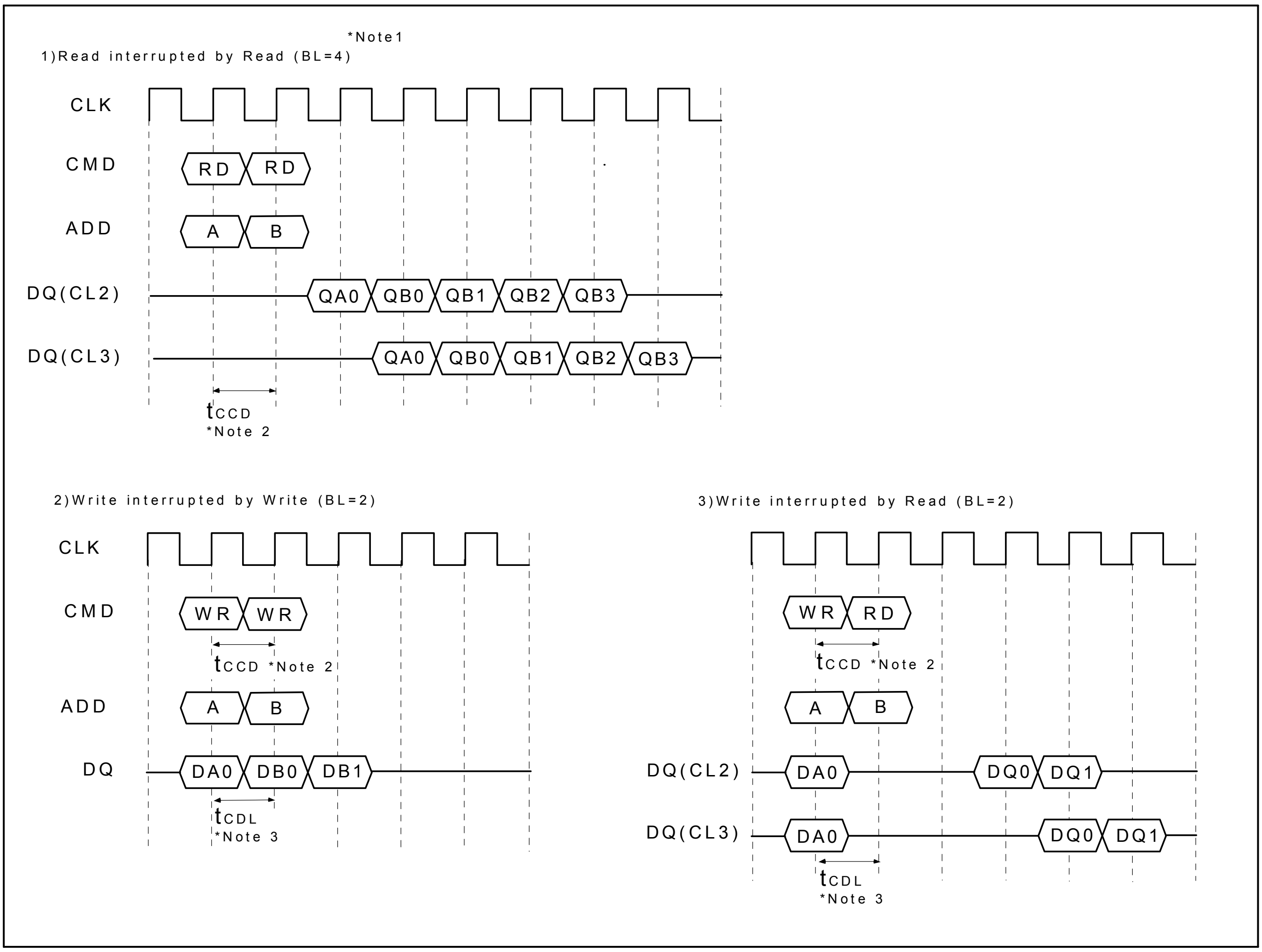


2. DQM Operation



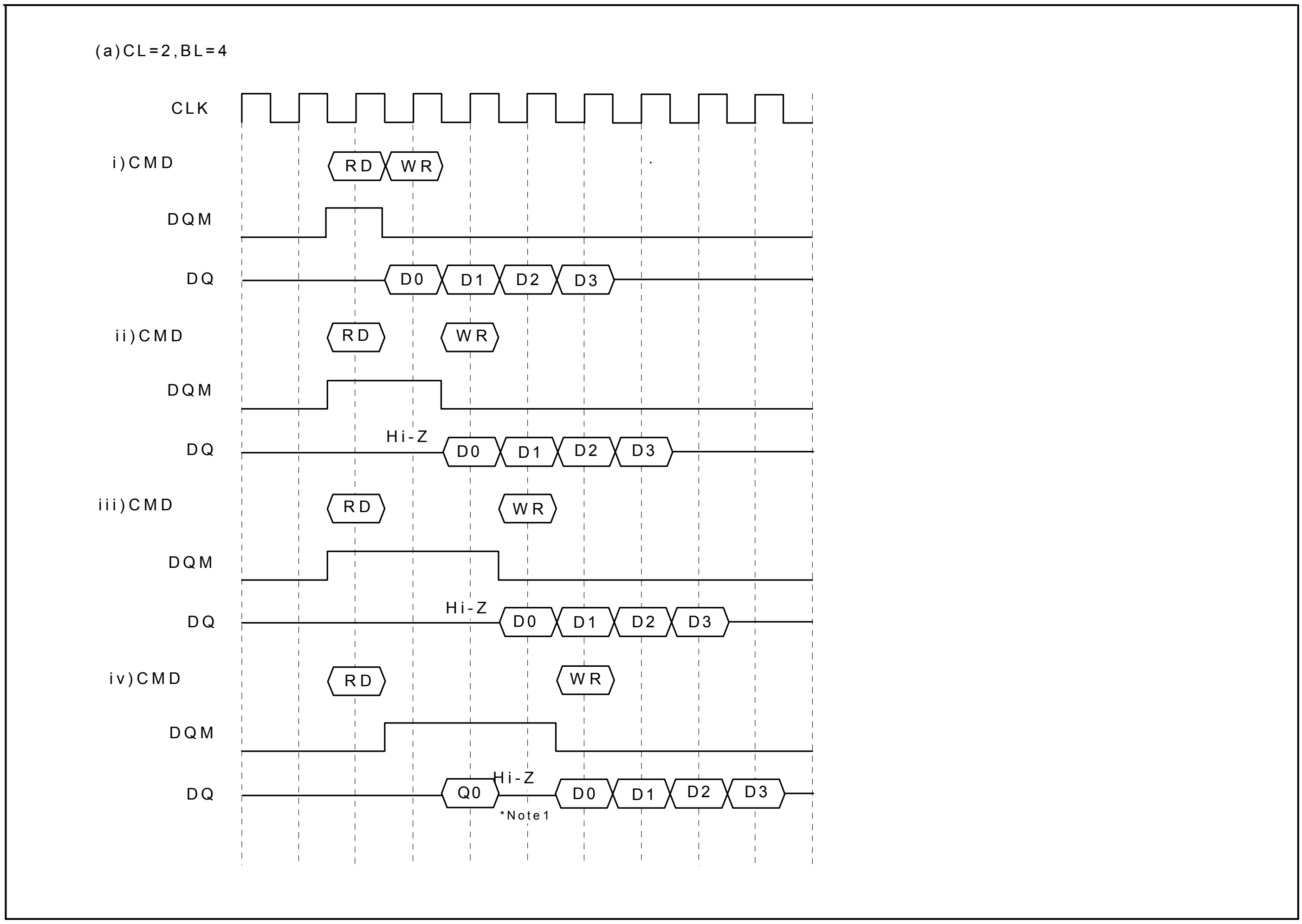
*Note: 1. CKE to CLK disable/enable = 1CLK.
2. DQM masks data out Hi-Z after 2CLKs which should masked by CKE ”L”.
3. DQM masks both data-in and data-out.

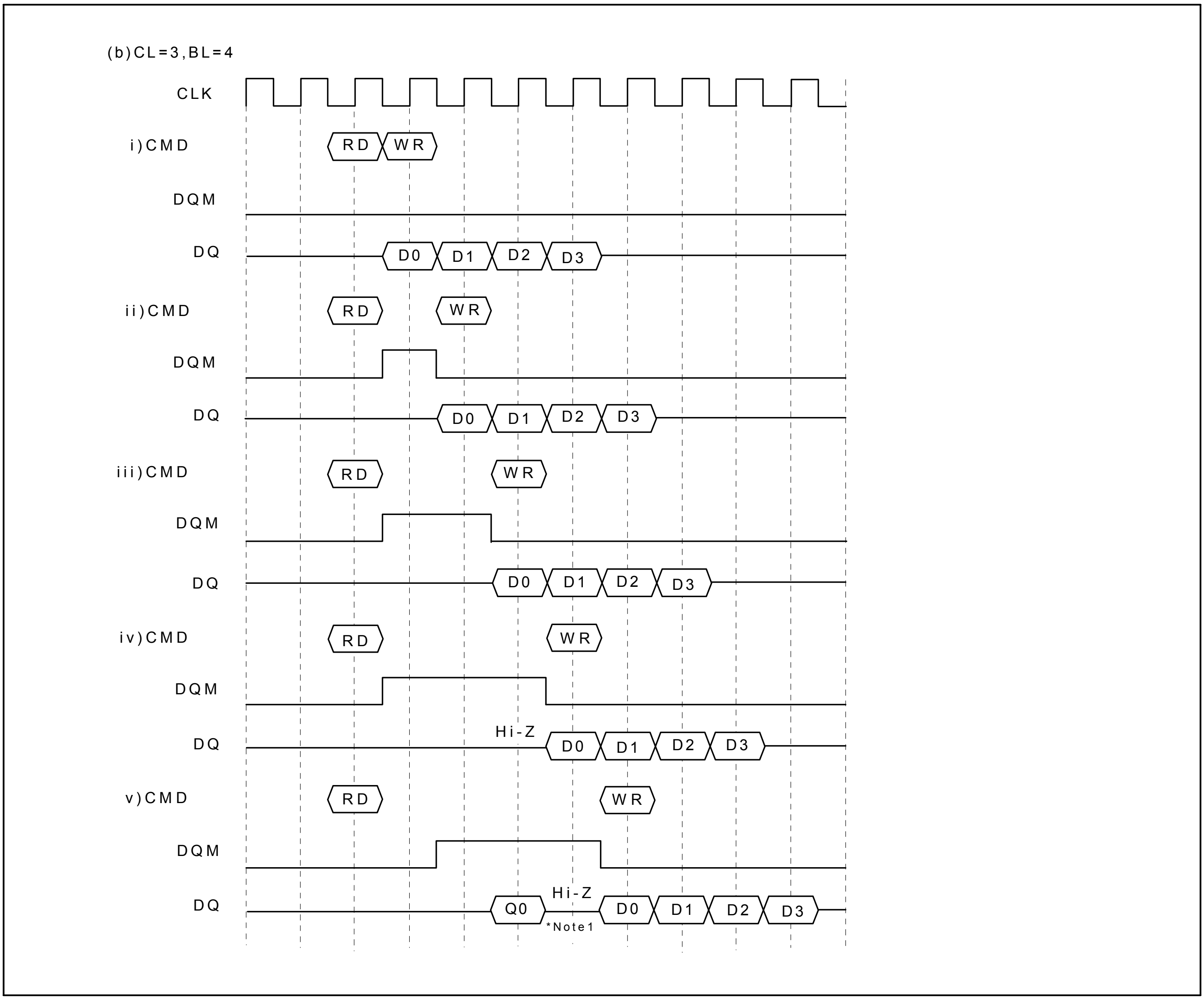
3. $\overline{\text{CAS}}$ Interrupt (I)



*Note: 1. By "interrupt" is meant to stop burst read/write by external before the end of burst.
By " $\overline{\text{CAS}}$ interrupt ", to stop burst read/write by $\overline{\text{CAS}}$ access ; read and write.
2. t_{CCD}: $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay. (=1CLK)
3. t_{CDL}: Last data in to new column address delay. (=1CLK)

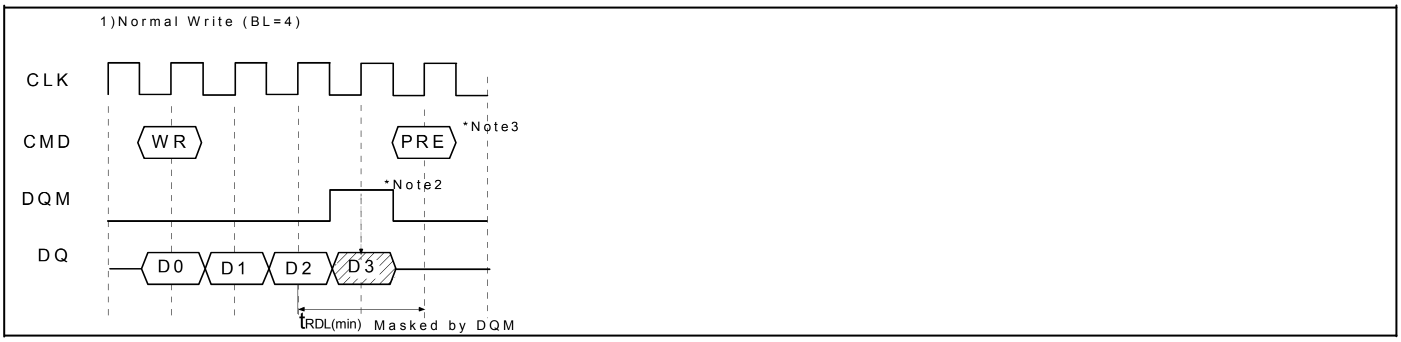
4. $\overline{\text{CAS}}$ Interrupt (II): Read Interrupted by Write & DQM





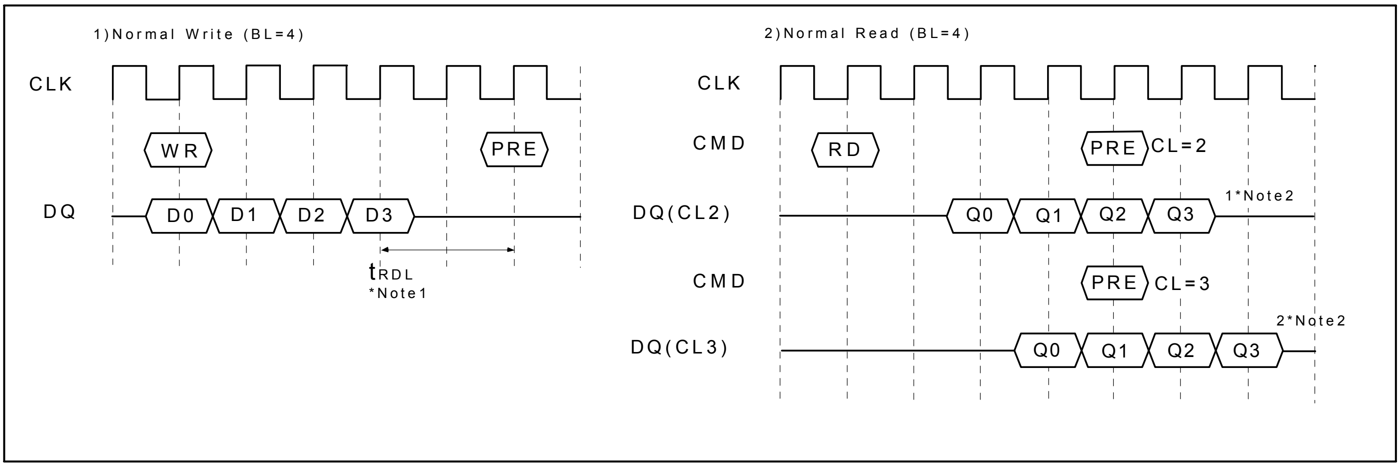
*Note: 1. To prevent bus contention, there should be at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM



*Note:
1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.

6. Precharge



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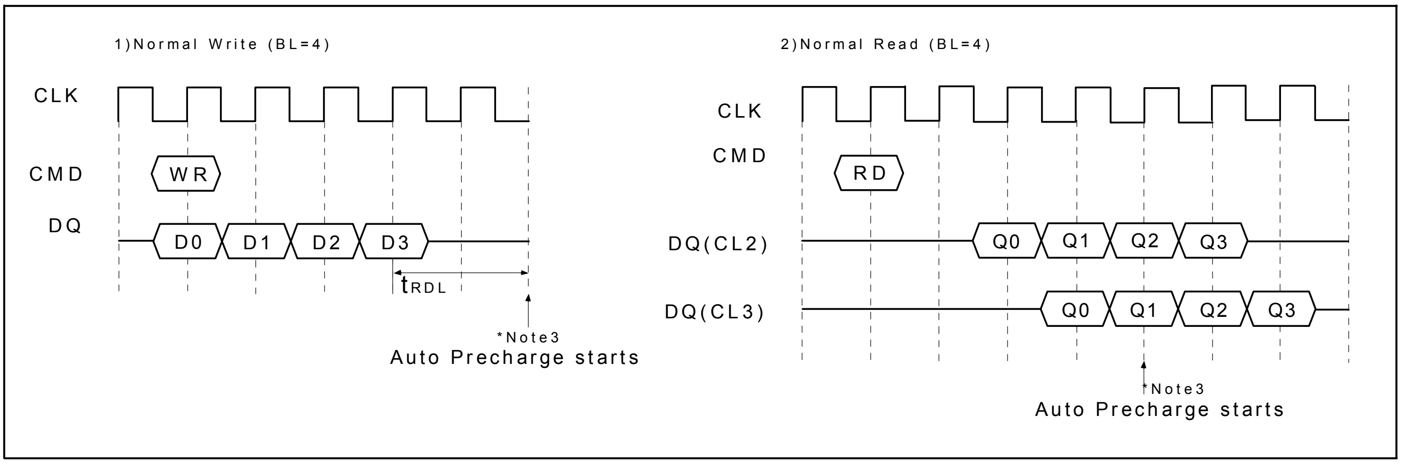
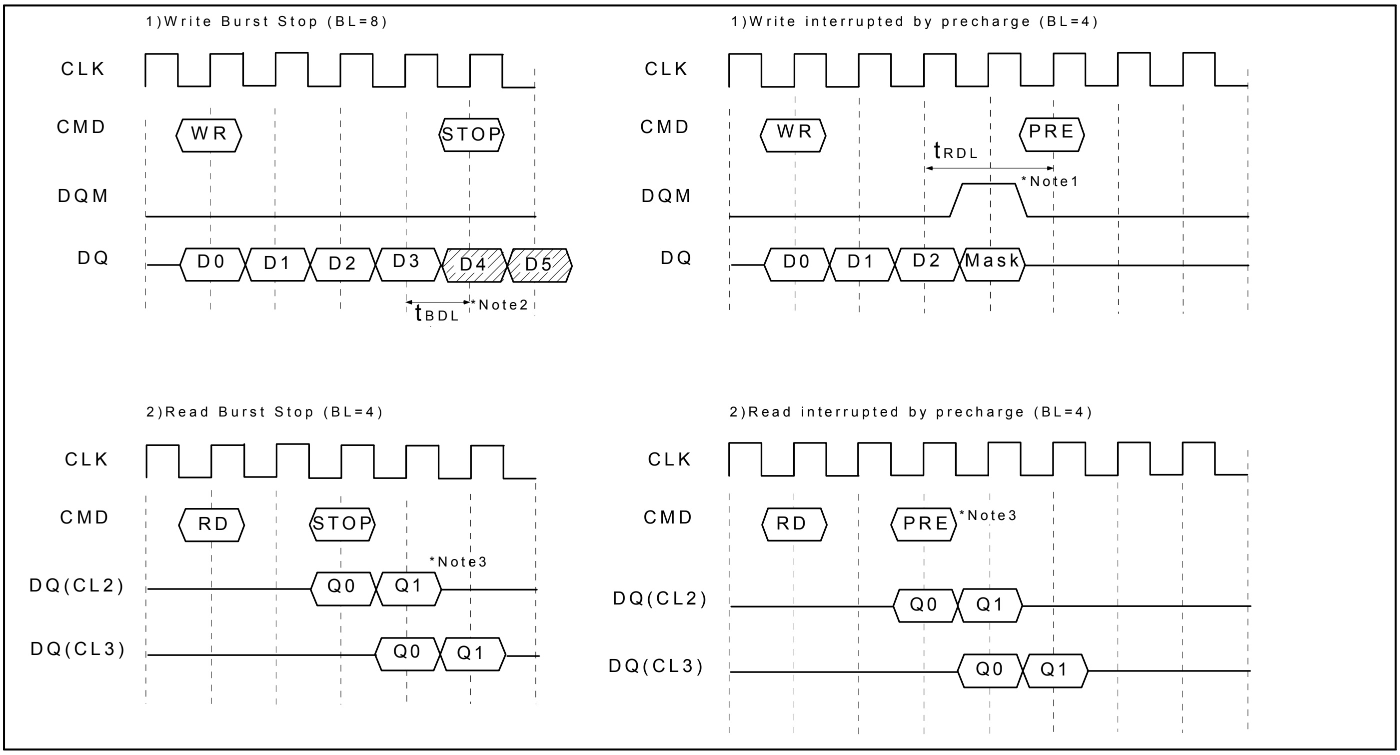
7. Auto Precharge

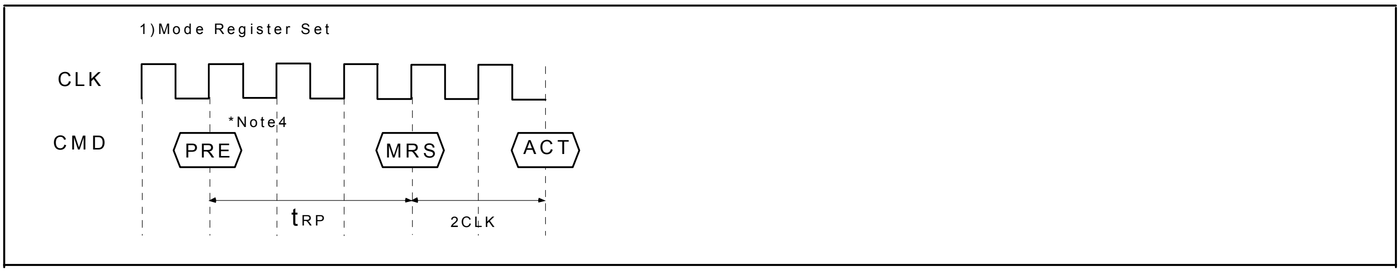


*Note:
1. t_{RDL}: Last data in to row precharge delay.
2. Number of valid output data after row precharge: 1, 2 for CAS Latency = 2, 3 respectively.
3. The row active command of the precharge bank can be issued after t_{RP} from this point.
   The new read/write command of other activated bank can be issued from this point.
   At burst read/write with auto precharge, $\overline{\text{CAS}}$ interrupt of the same/another bank is illegal.

8. Burst Stop & Interrupted by Precharge

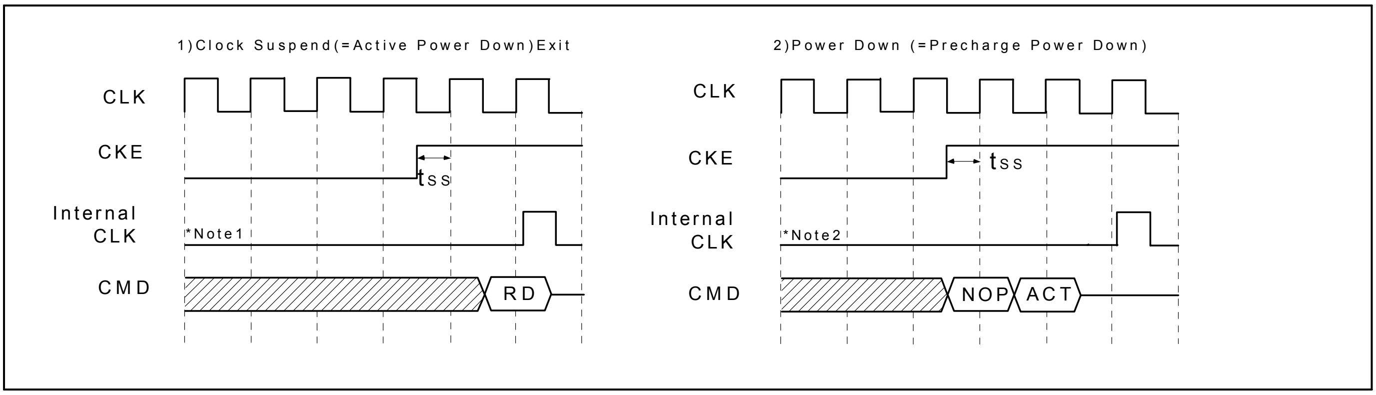


9. MRS

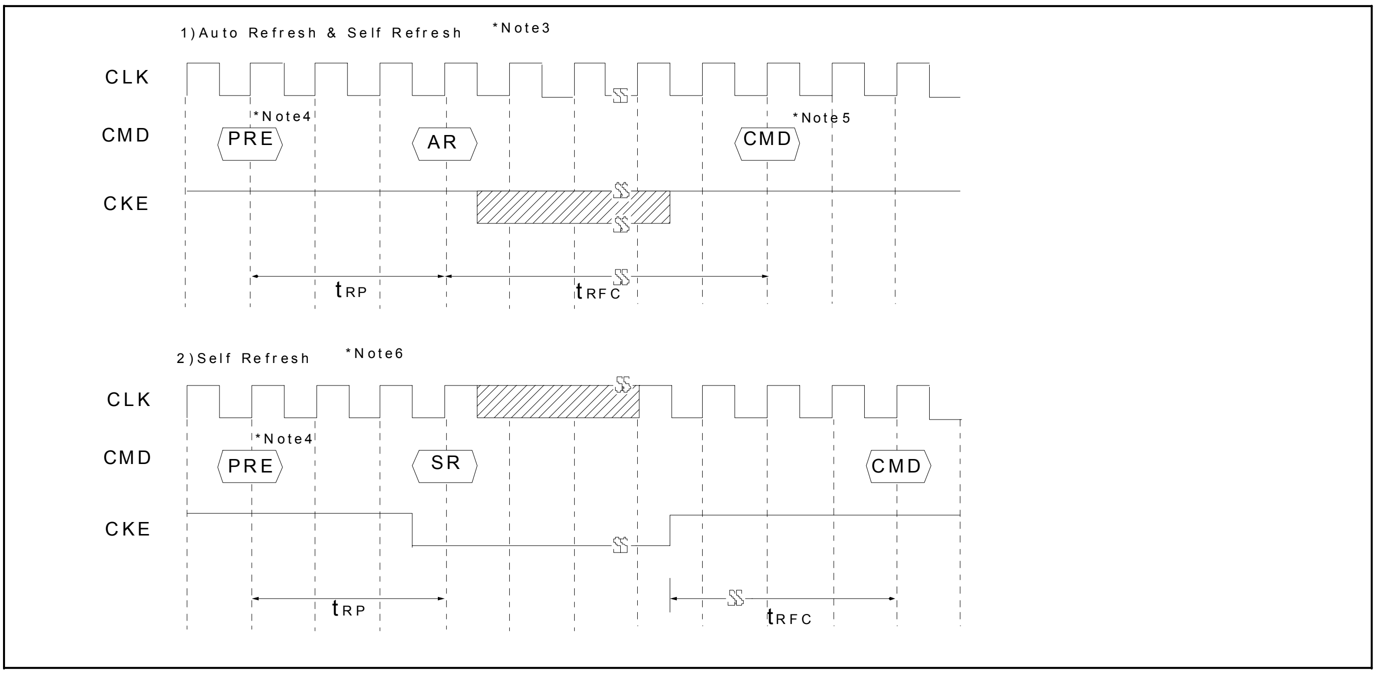


*Note: 1. t_{RDL}: 2 CLK; Last data in to Row Precharge.
2. t_{BDL}: 1 CLK ; Last data in to burst stop delay.
3. Number of valid output data after burst stop: 1, 2 for CAS latency = 2, 3 respectiviely.
4. PRE: All banks precharge, if necessary.
MRS can be issued only at all banks precharge state.

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



*Note:
1. Active power down: one or more banks active state.
2. Precharge power down: all banks precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
   No precharge commands are required after auto refresh command.
   During t_{RFC} from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, all banks must be idle state.
5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh entry, refresh interval and refresh operation are performed internally.
   After self refresh entry, self refresh mode is kept while CKE is low.
   During self refresh entry, all inputs expect CKE will be don’t cared, and outputs will be in Hi-Z state.
   For the time interval of t_{RFC} from self refresh exit command, any other command can not be accepted.
   4K cycles of burst auto refresh is required immediately before self refresh entry and immediately after self refresh exit.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A3 = "0". See the BURST SEQUENCE TABLE. (BL = 4,8) BL = 1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A3 = "1". See the BURST SEQUENCE TABLE. (BL = 4,8) BL = 4, 8 At BL =1, 2 interleave Counting = Sequential Counting
Random MODE	Random Column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS A210 = "000" At auto precharge. t_{RAS} should not be violated.
	2	At MRS A210 = "001" At auto precharge. t_{RAS} should not be violated.
	4	At MRS A210 = "010"
	8	At MRS A210 = "011"
	Full Page	At MRS A210 = "111" At the end of the burst length, burst is warp-around.
Random MODE	Burst Stop	t_{BDL} = 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst. Row precharge command of the same bank stops read /write burst with auto precharge. t_{RDL} = 1 with DQM , Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (&Bank) Active ; Latch RA	
	L	L	H	L	BA	A10/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A10/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A10/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	Term burst → Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	Term burst → Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	3
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End → Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End → Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	

Current State	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	**BA**	**ADDR**	**ACTION**	**Note**
Precharging	H	X	X	X	X	X	NOP → Idle after t_{RP}	
	L	H	H	H	X	X	NOP → Idle after t_{RP}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	NOP → Idle after t_{RDL}	4
	L	L	L	X	X	X	ILLEGAL	
Row Activating	H	X	X	X	X	X	NOP → Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP → Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP → Idle after t_{RFC}	
	L	H	H	X	X	X	NOP → Idle after t_{RFC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP → Idle after 2clocks	
	L	H	H	H	X	X	NOP → Idle after 2clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations:
RA = Row Address
BA = Bank Address
NOP = No Operation Command
CA = Column Address
AP = Auto Precharge

*Note:
1. All entries assume the CKE was active (High) during the precharge clock and the current clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BA, depending on the state of the bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharge or in idle state. May precharge bank indicated by BA (and A10/AP).
5. Illegal if any bank is not idle.

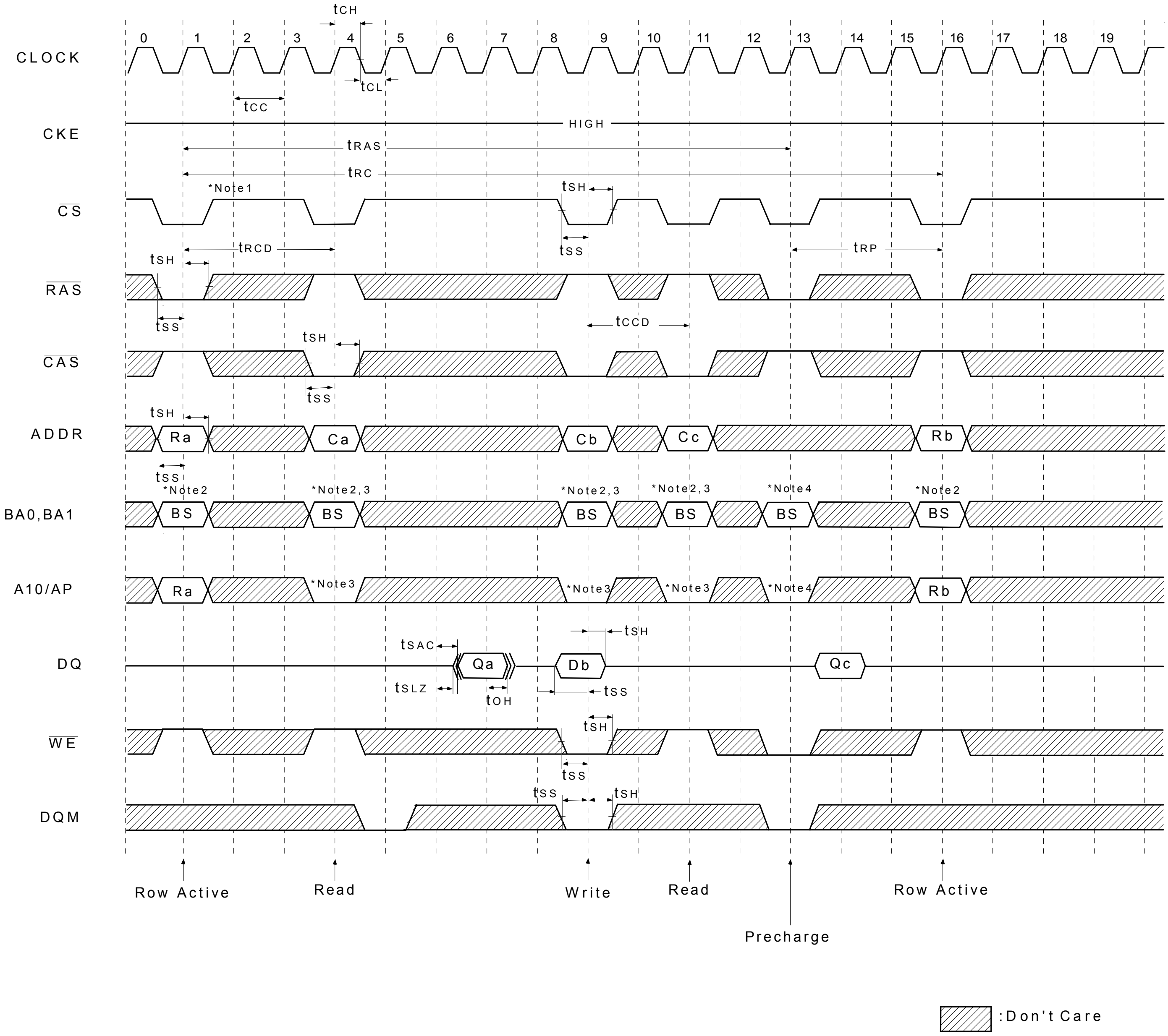
FUNCTION TRUTH TABLE (TABLE2)

Current State	CKE (n-1)	CKE n	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh → Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh → Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh → ABI	7
	L	H	L	H	H	H	X	Exit Self Refresh → ABI	7
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table1	
	H	L	H	X	X	X	X	Enter Power Down	8
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	L	H	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clock Suspend	

Abbreviations: ABI = All Banks Idle, RA = Row Address

*Note: 6.CKE low to high transition is asynchronous.
7.CKE low to high transition is asynchronous if restart internal clock.
A minimum setup time 1CLK + t_{SS} must be satisfy before any command other than exit.
8.Power down and self refresh can be entered only from the all banks idle state.
9.Must be a legal command.

Single Bit Read-Write-Read Cycle(Same Page) @ CAS Latency = 3, Burst Length = 1



Note: 1. All input expect CKE & DQM can be don’t care when $\overline{CS}$ is high at the CLK high going edge.

2. Bank active @ read/write are controlled by BA0~BA1.

BA1	BA0	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

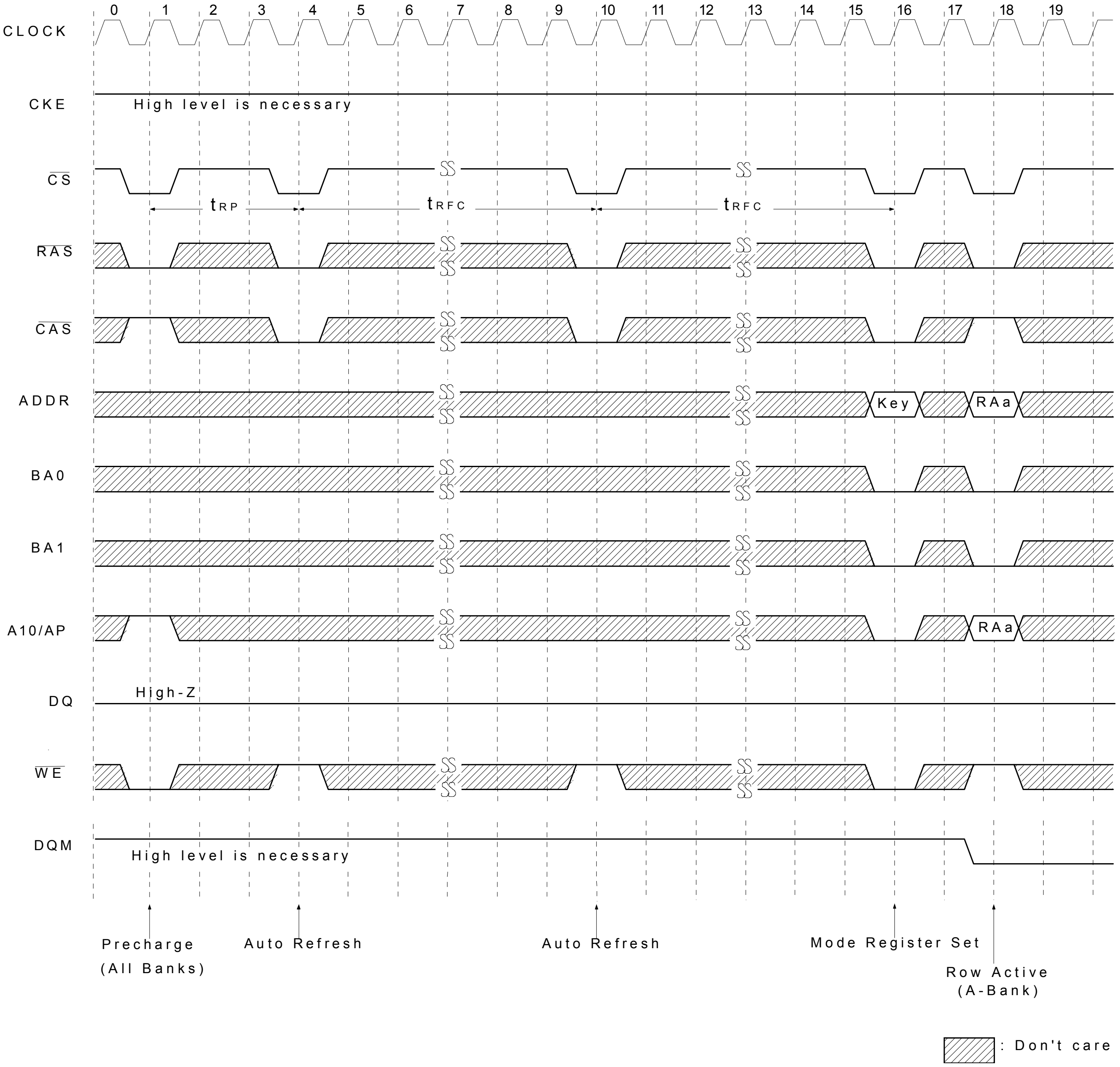
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command

A10/AP	BA1	BA0	Operating
0	0	0	Disable auto precharge, leave A bank active at end of burst.
	0	1	Disable auto precharge, leave B bank active at end of burst.
	1	0	Disable auto precharge, leave C bank active at end of burst.
	1	1	Disable auto precharge, leave D bank active at end of burst.
1	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	Enable auto precharge, precharge bank B at end of burst.
	1	0	Enable auto precharge, precharge bank C at end of burst.
	1	1	Enable auto precharge, precharge bank D at end of burst.

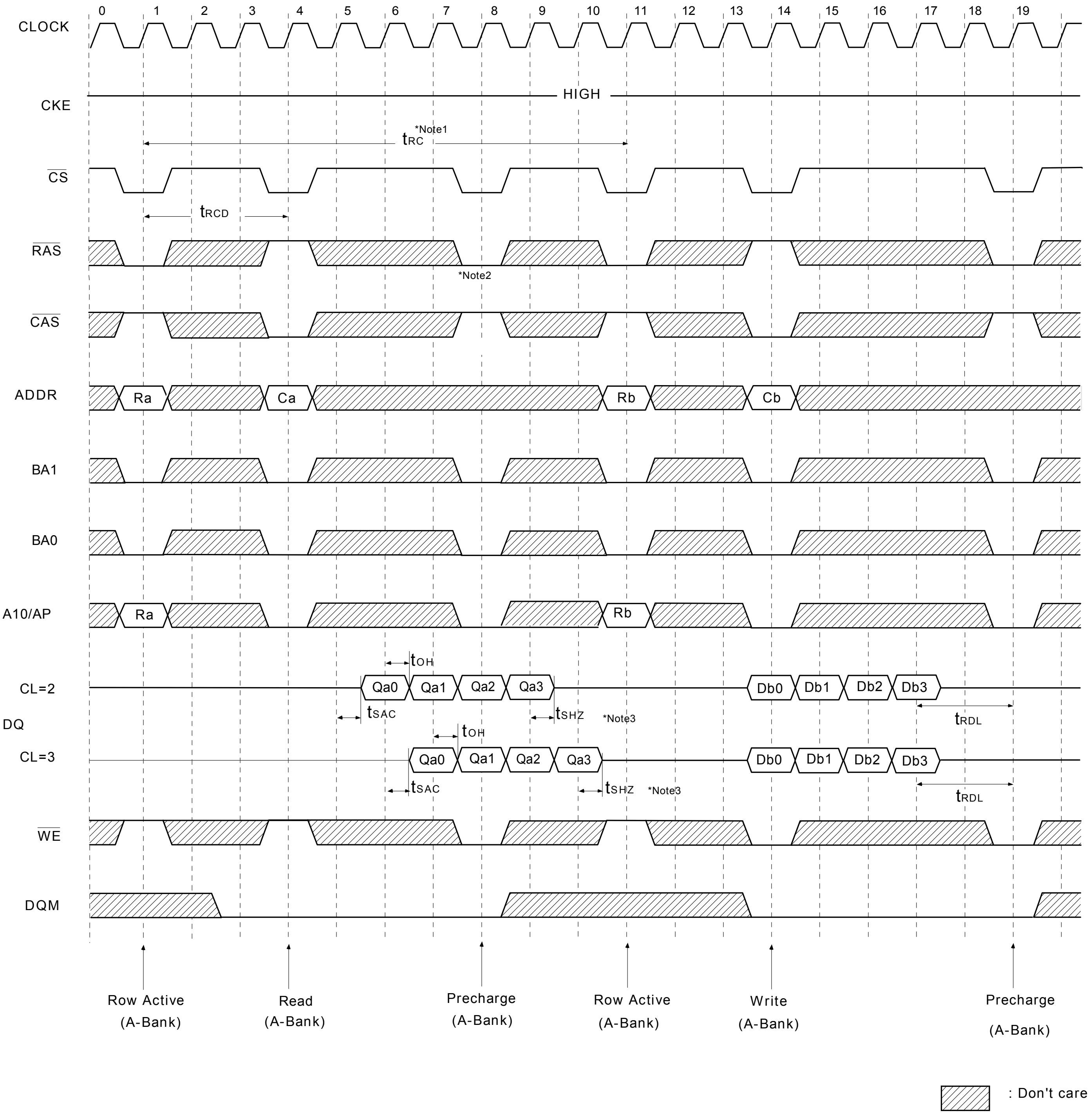
4. A10/AP and BA0~BA1 control bank precharge when precharge is asserted.

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	X	X	All Banks

Power Up Sequence

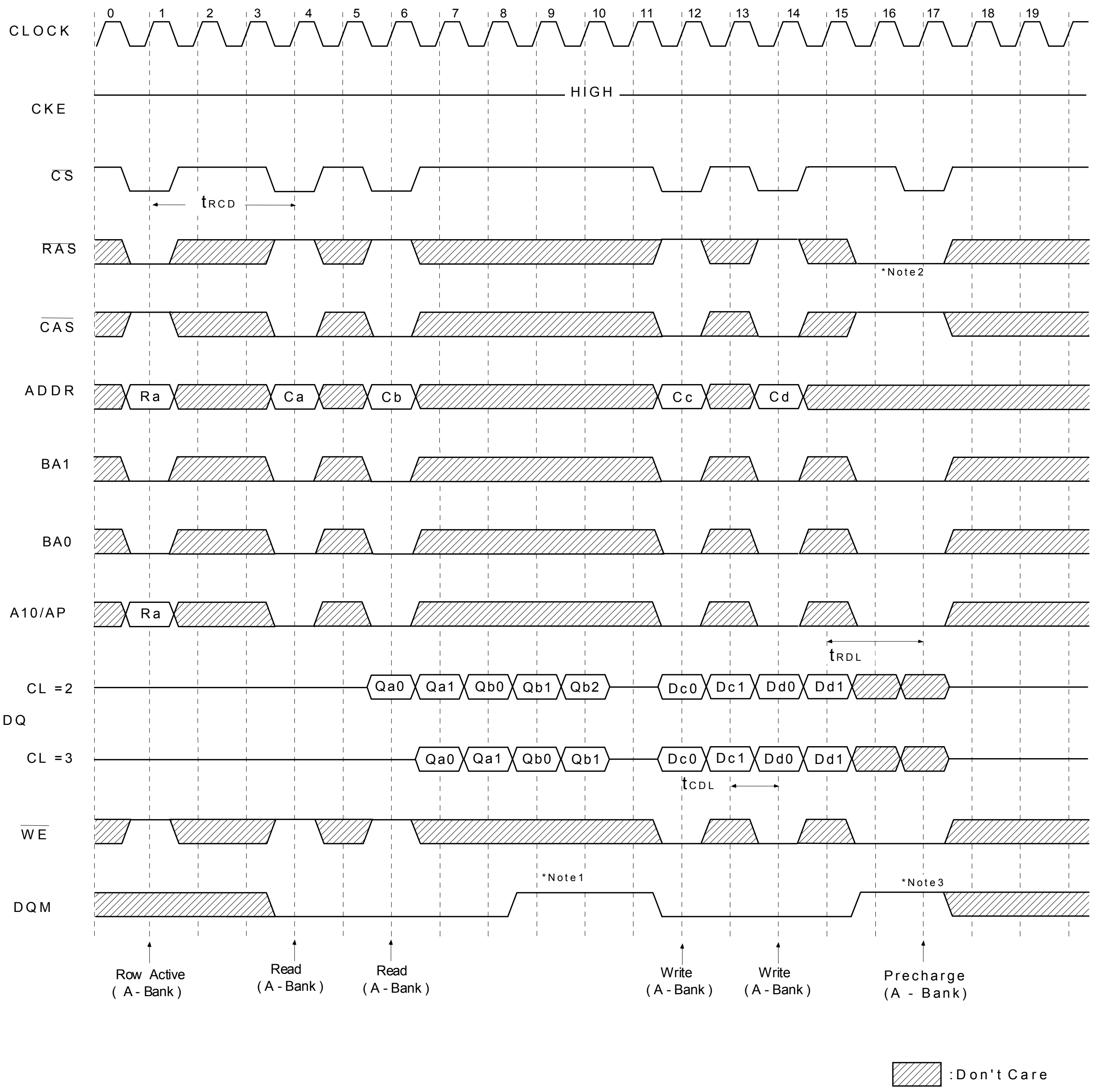


Read & Write Cycle at Same Bank @ Burst Length = 4



*Note:
1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency-1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z (t_{SHZ}) after the clock.
3. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

Page Read & Write Cycle at Same Bank @ Burst Length = 4

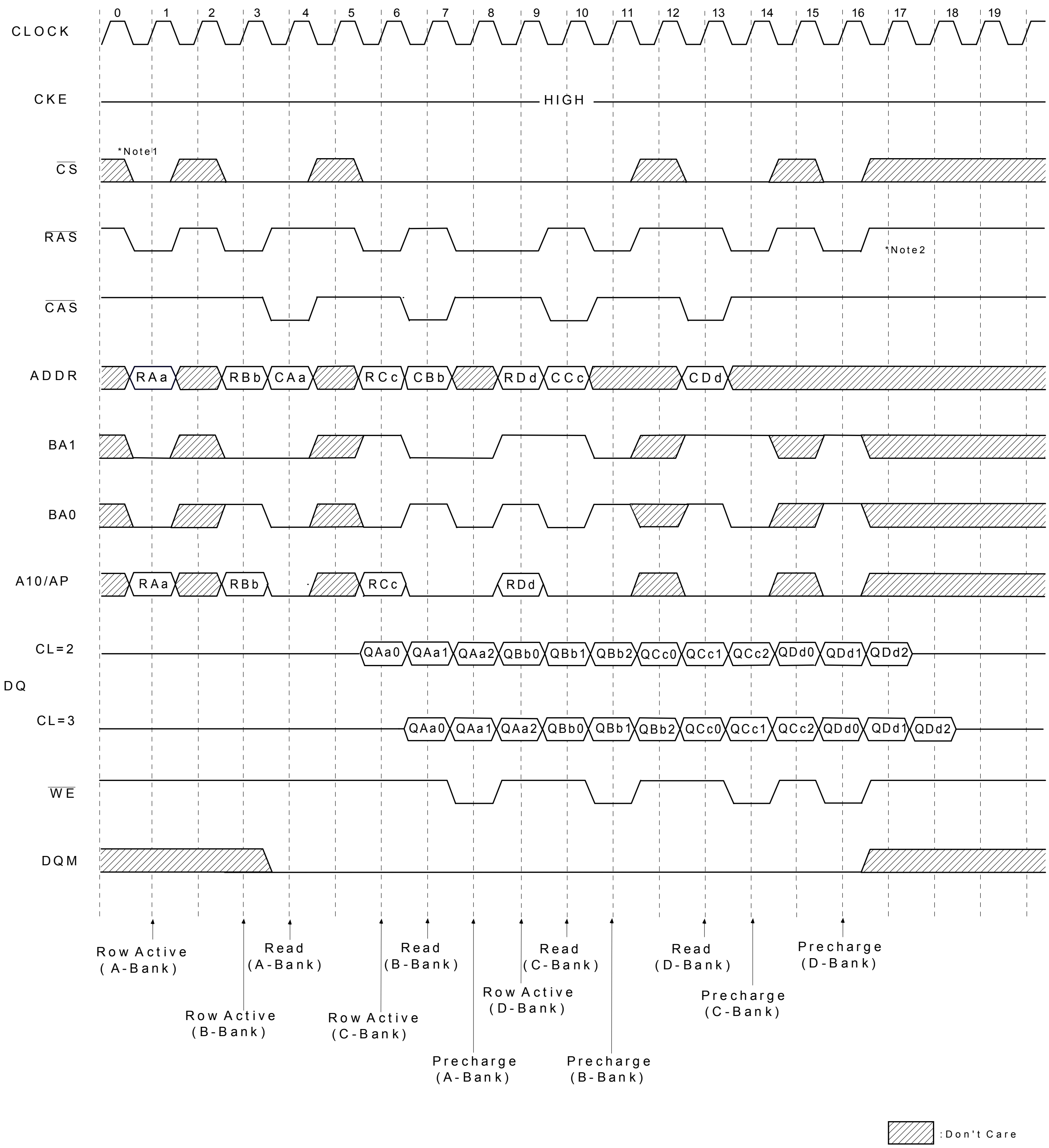


Note: 1. To Write data before burst read ends. DQM should be asserted three cycles prior to write command to avoid bus contention.

2. Row precharge will interrupt writing. Last data input, t_{RDL} before row precharge, will be written.

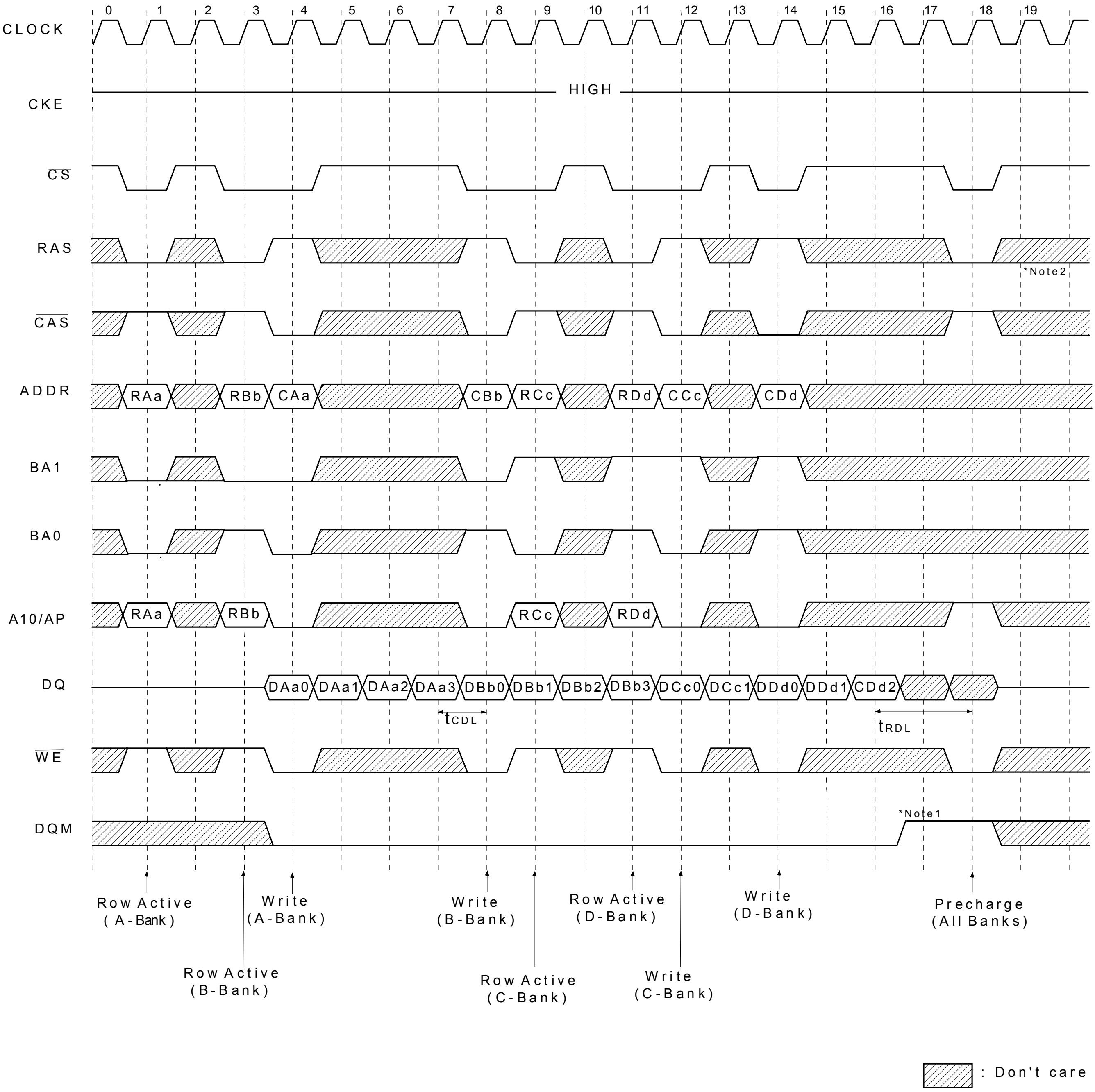
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

Page Read Cycle at Different Bank @ Burst Length = 4



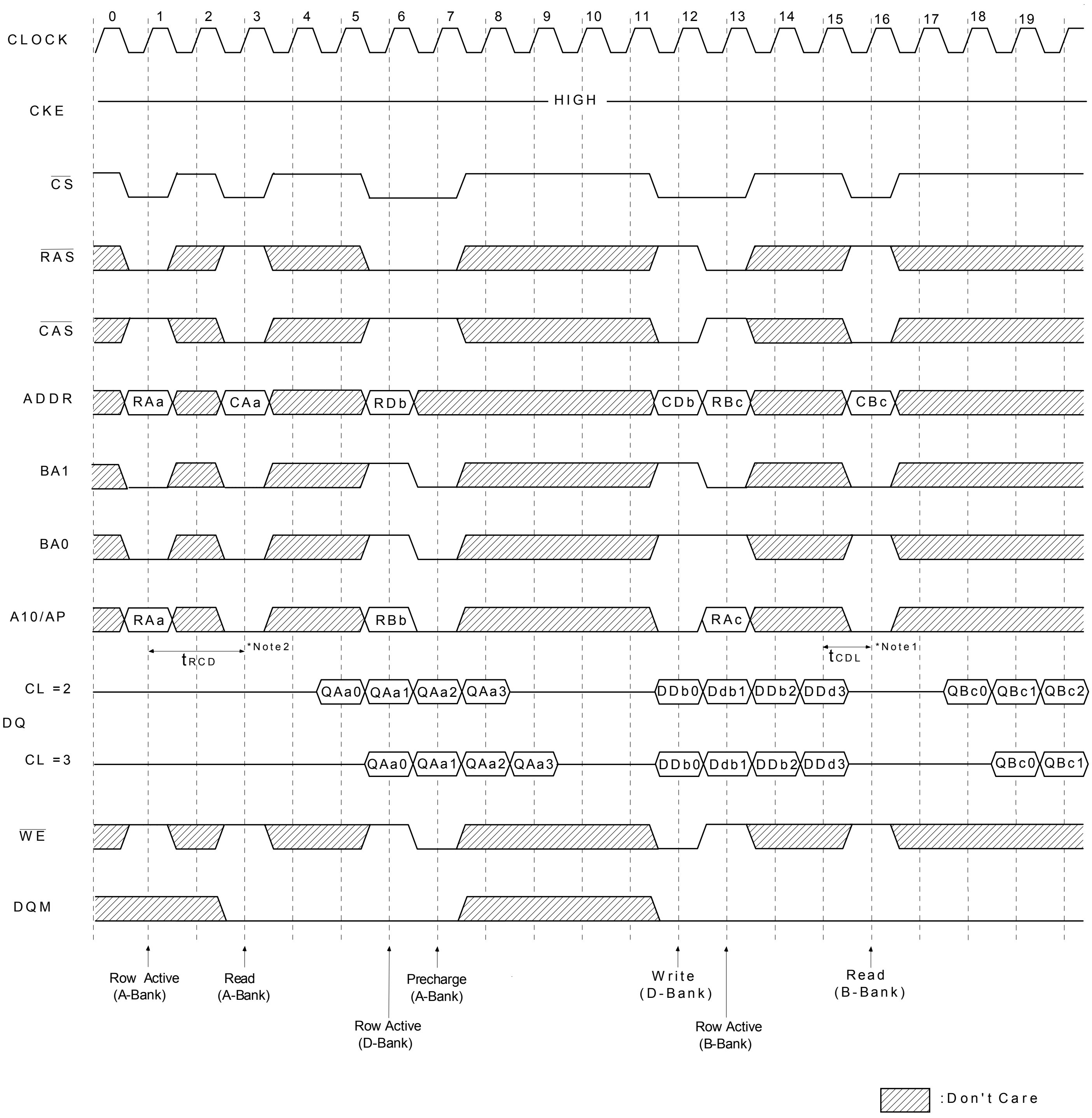
Note: 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going edge.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @ Burst Length = 4



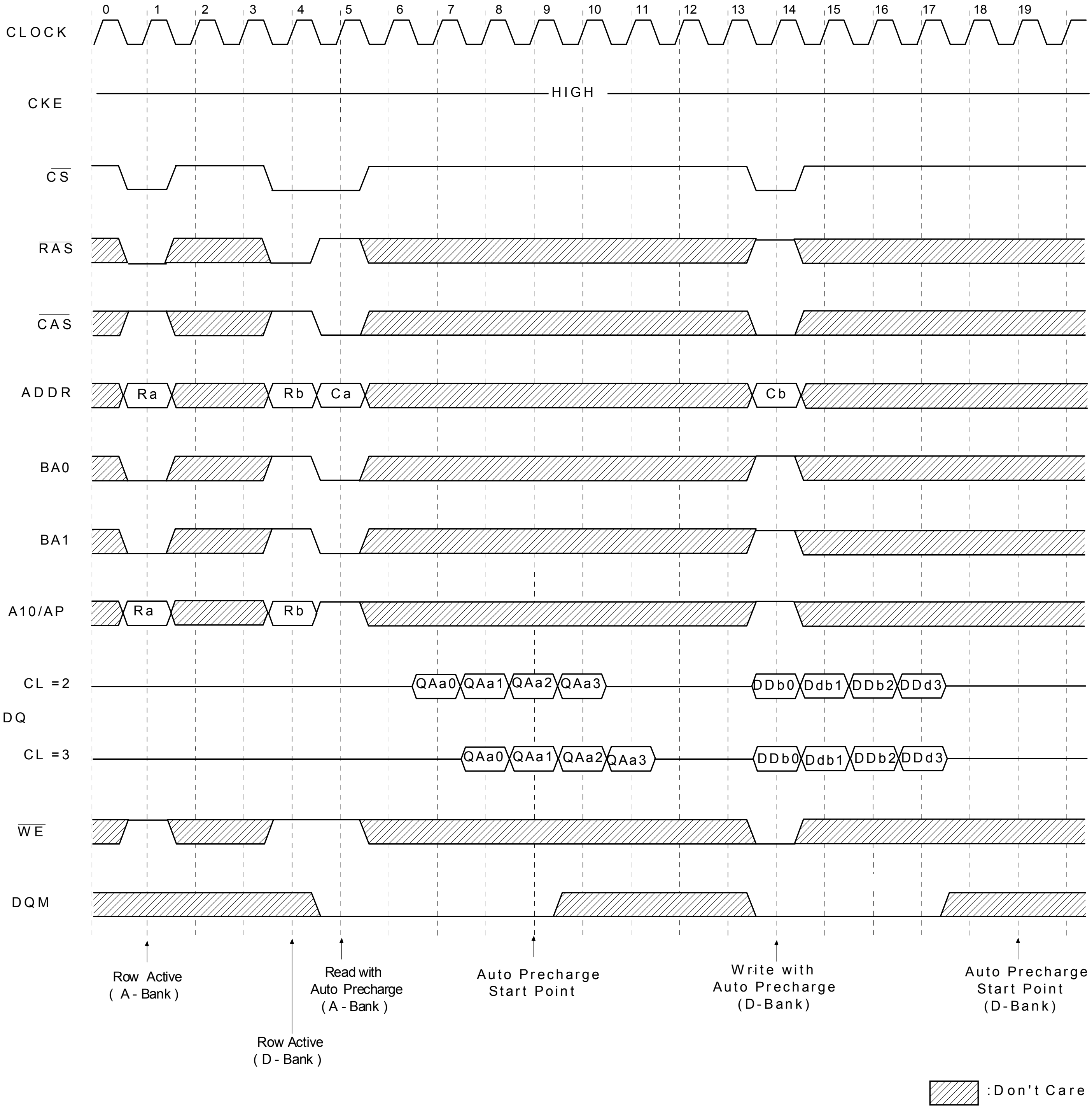
*Note: 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @ Burst Length = 4



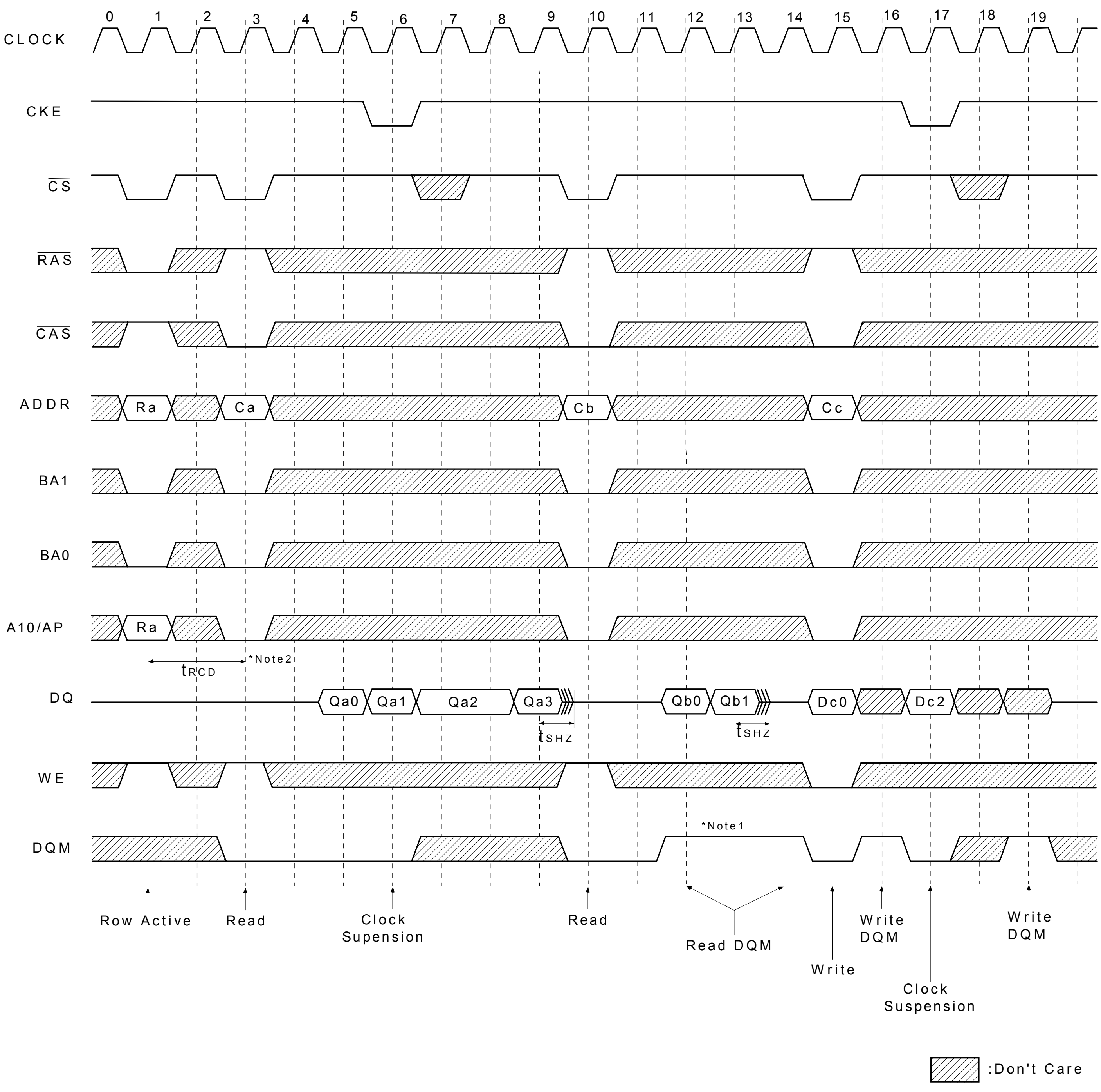
*Note: 1. t_{CDL} should be met to complete write.
2. t_{RCD} should be met.

Read & Write cycle with Auto Precharge @ Burst Length = 4



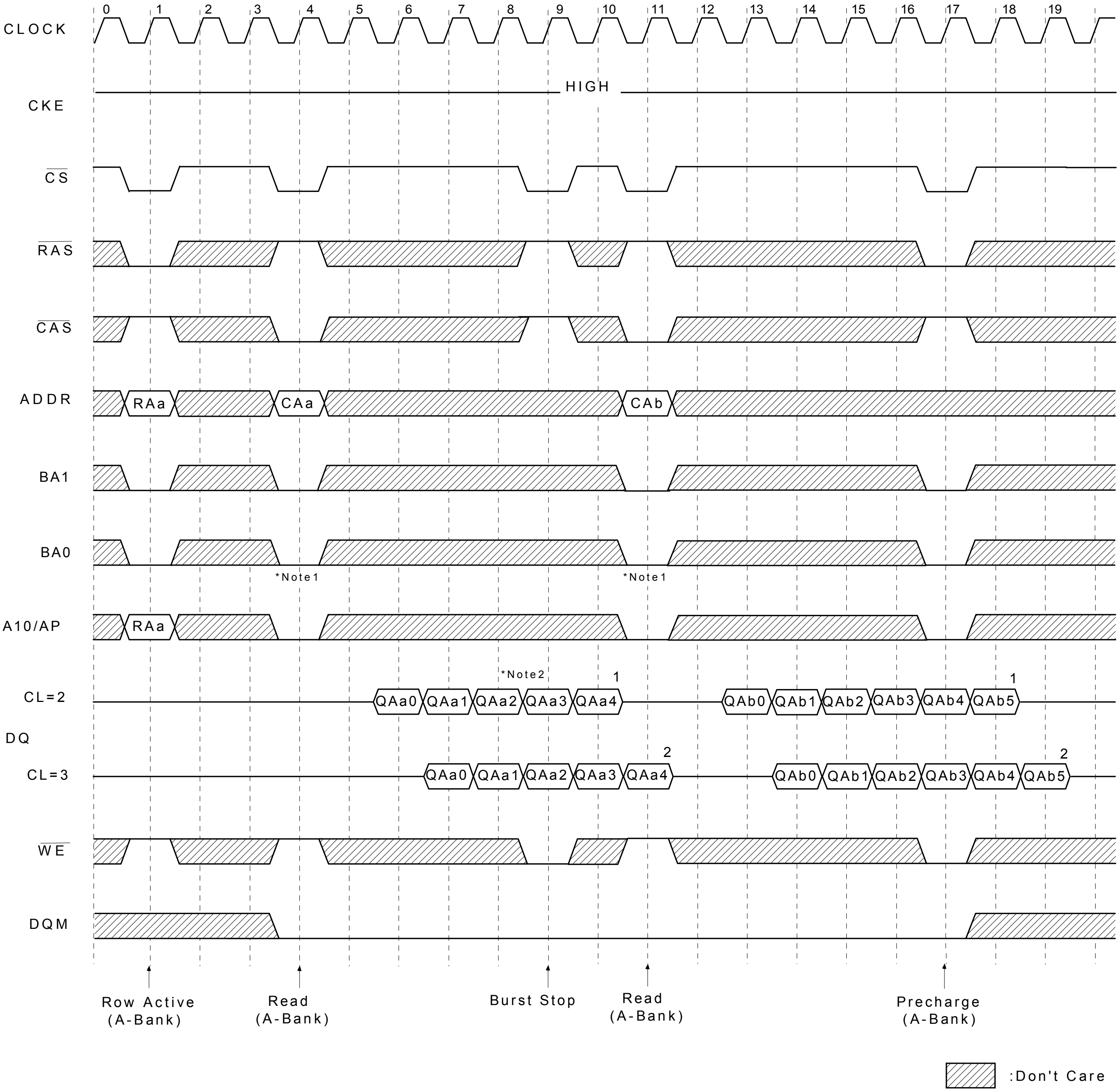
*Note: 1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start.
(In the case of Burst Length = 1 & 2)

Clock Suspension & DQM Operation Cycle @ CAS Latency = 2, Burst Length = 4



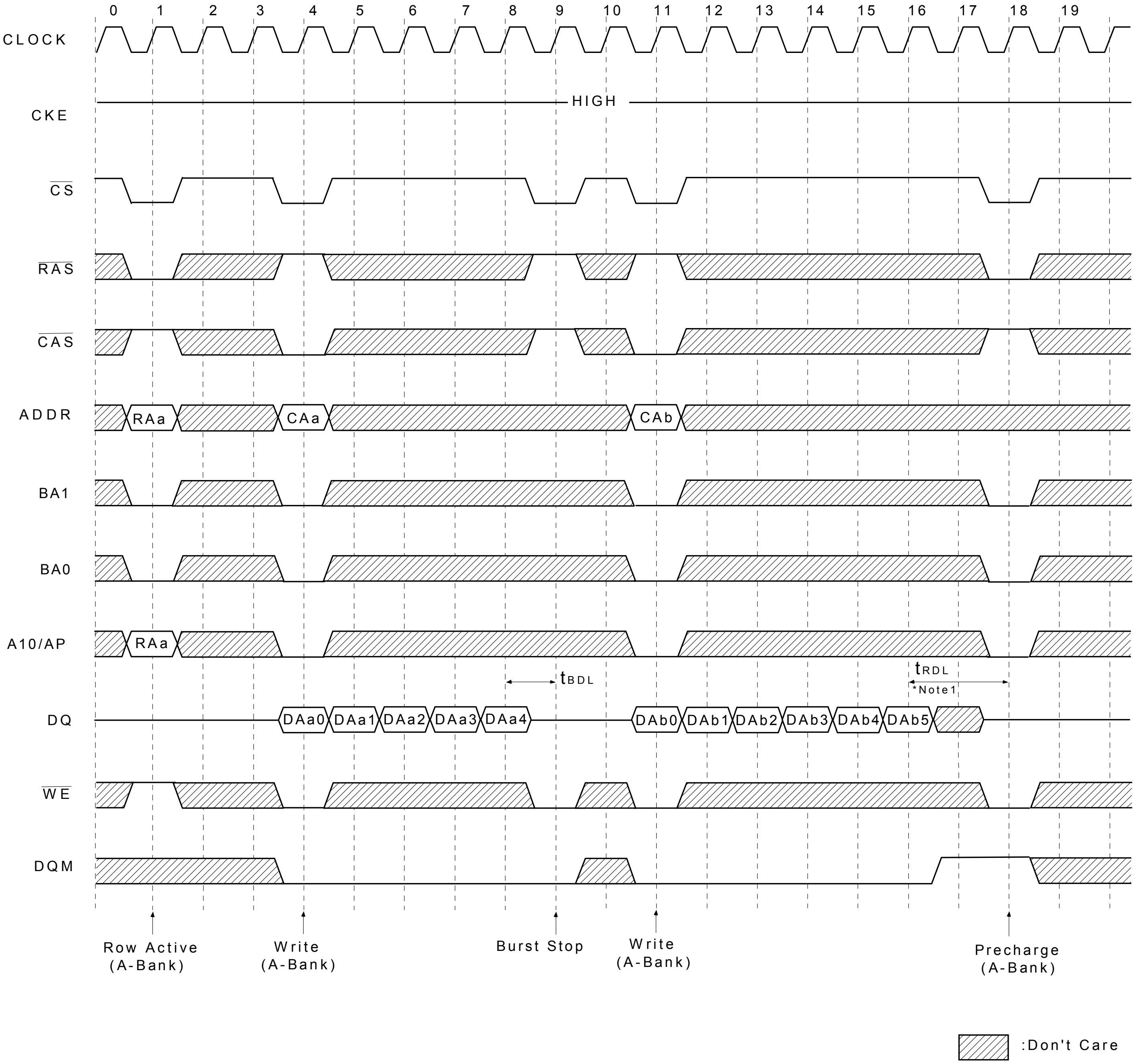
*Note: 1. DQM is needed to prevent bus contention.
2. t_{RCD} should be met.

Read interrupted by Precharge Command & Read Burst Stop Cycle @ Burst Length = Full page



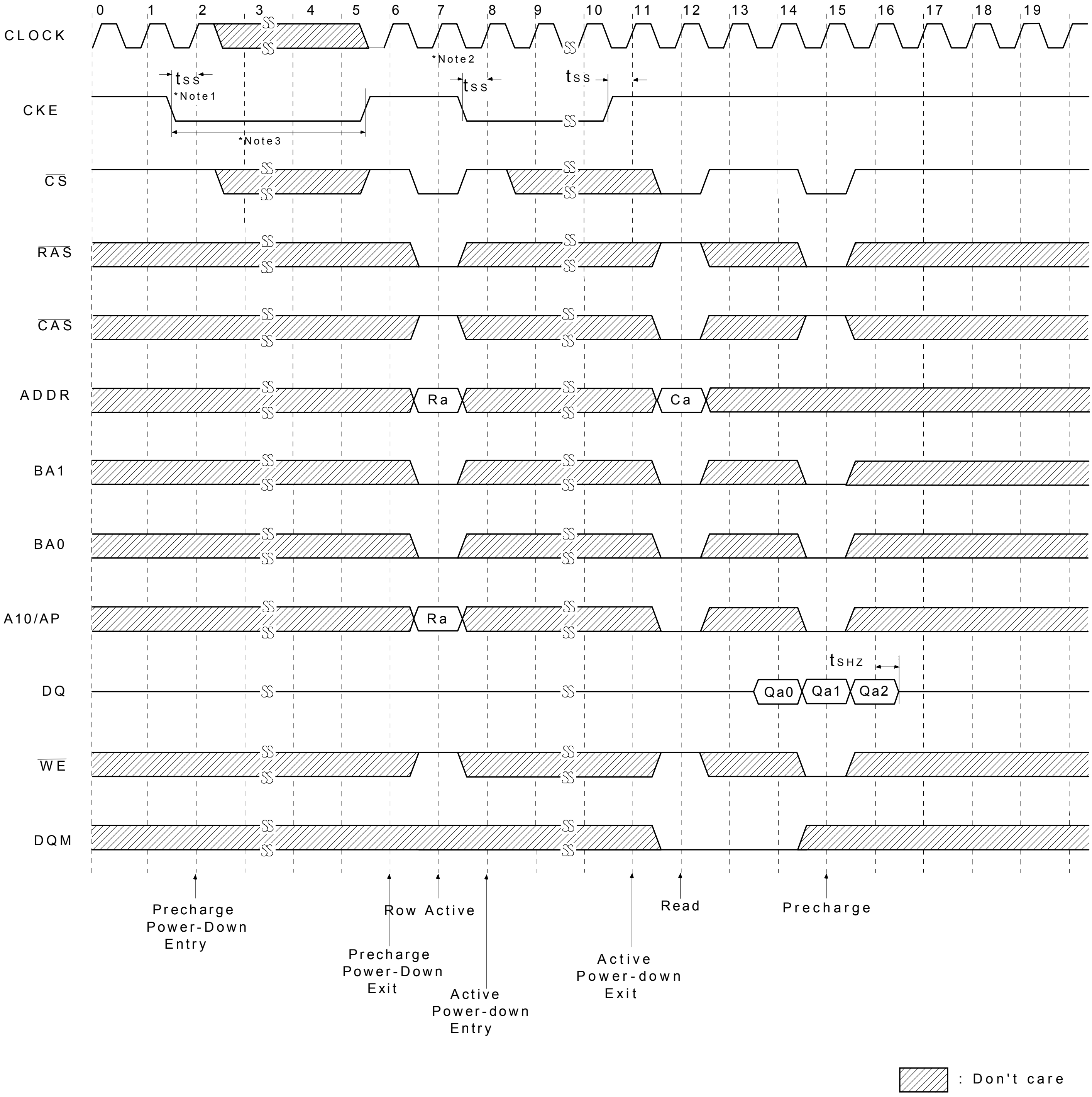
*Note: 1. About the valid DQs after burst stop, it is same as the case of $\overline{\text{RAS}}$ interrupt. Both cases are illustrated above timing diagram. See the label 1, 2 on them. But at burst write, Burst stop and $\overline{\text{RAS}}$ interrupt should be compared carefully. Refer the timing diagram of “Full page write burst stop cycles”.
2. Burst stop is valid at every burst length.
3. At full page mode, burst is finished by burst stop or precharge.

Write interrupted by Precharge Command & Write Burst Stop Cycle @ Burst Length = Full page



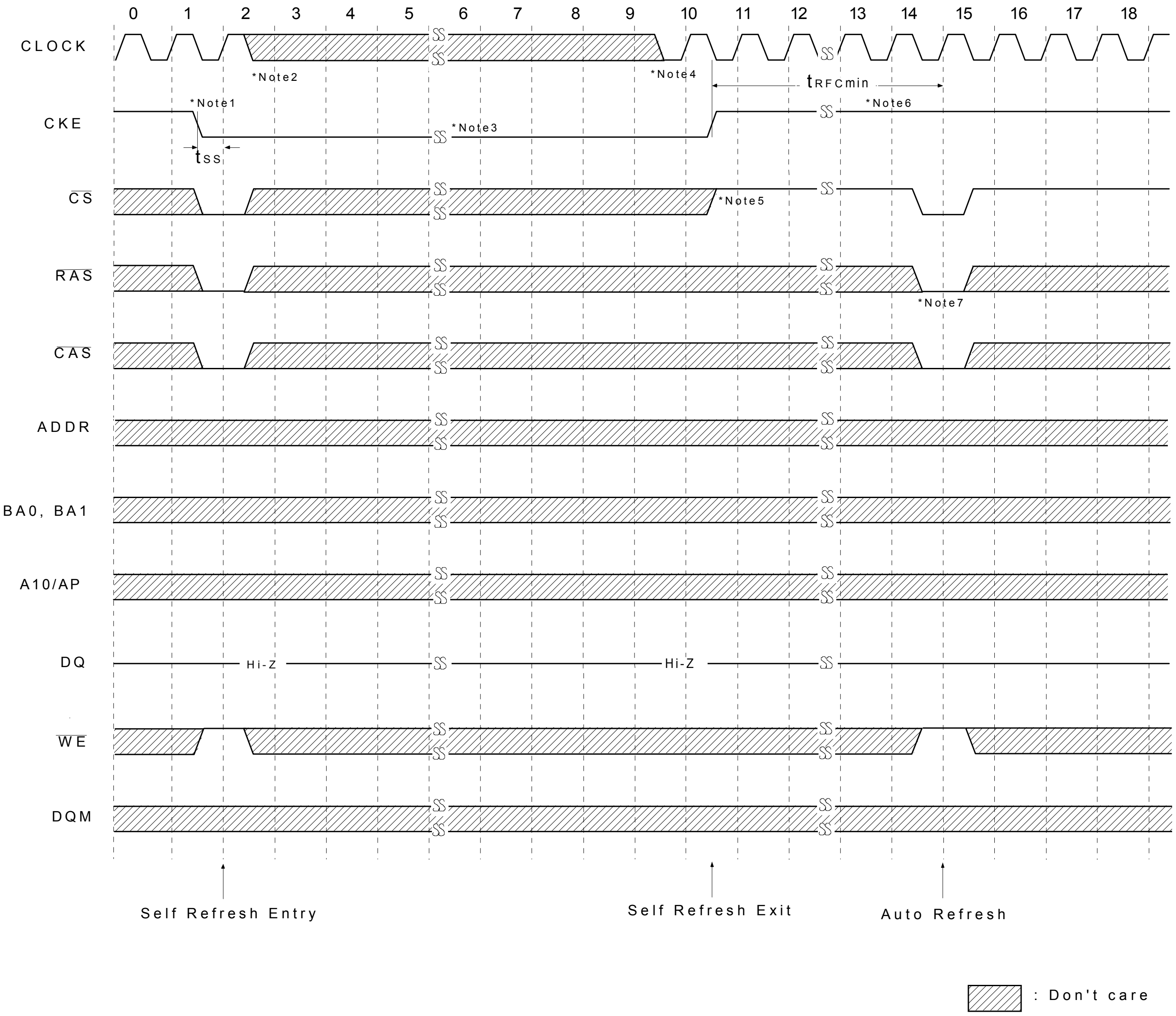
*Note: 1. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
DQM at write interrupted by precharge command is needed to prevent invalid write.
DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
2. Burst stop is valid at every burst length.
3. At full page mode, burst is finished by burst stop or precharge.

Active/Precharge Power Down Mode @ CAS Latency = 2, Burst Length = 4



*Note: 1. All banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + t_{SS} prior to Row active command.

Self Refresh Entry & Exit Cycle



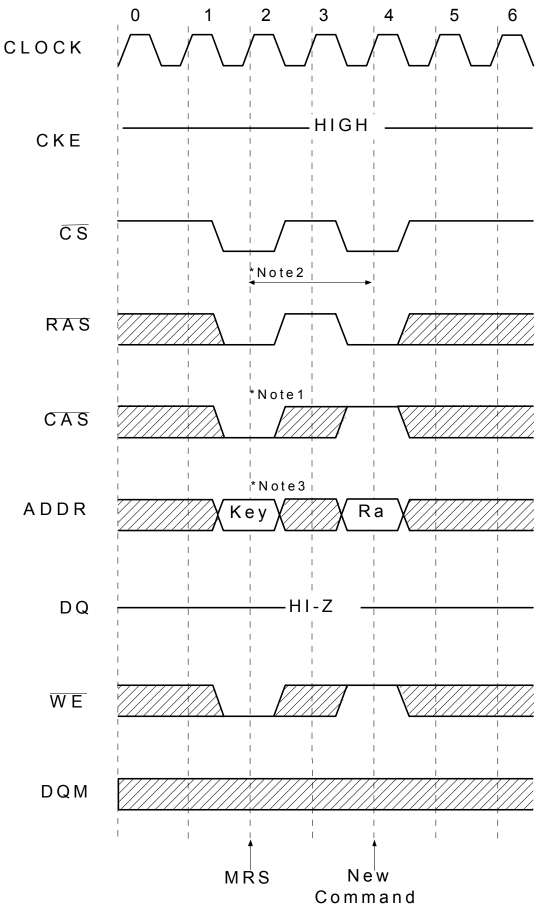
*Note: **TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

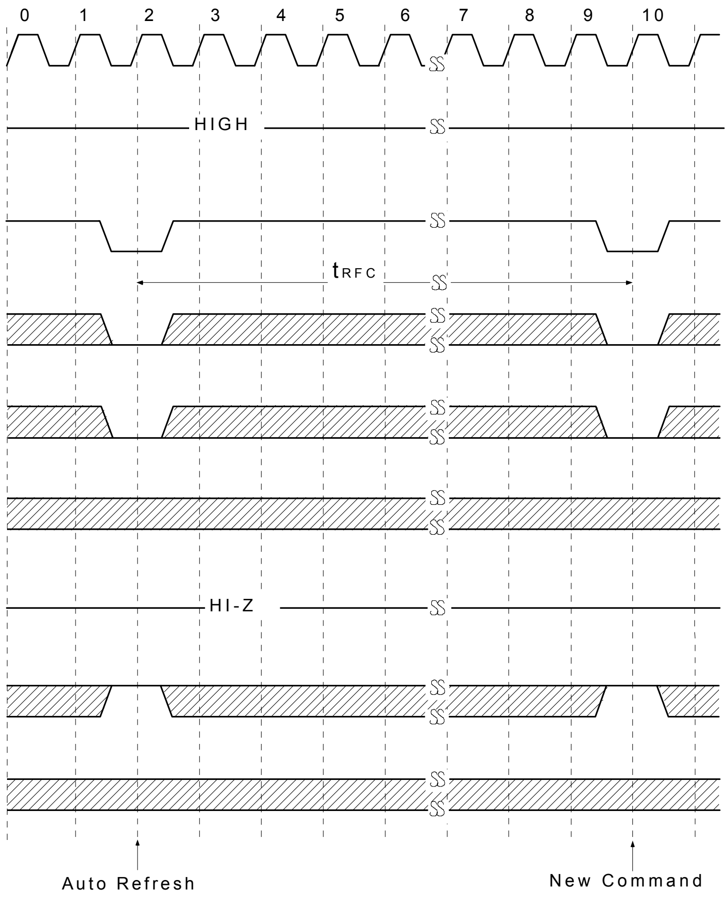
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RFC} is required after CKE going high to complete self refresh exit.
7. 4K cycles of burst auto refresh is required immediately before self refresh entry and immediately after self refresh exit.

Mode Register Set Cycle



Auto Refresh Cycle



▨ :Don't Care

All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

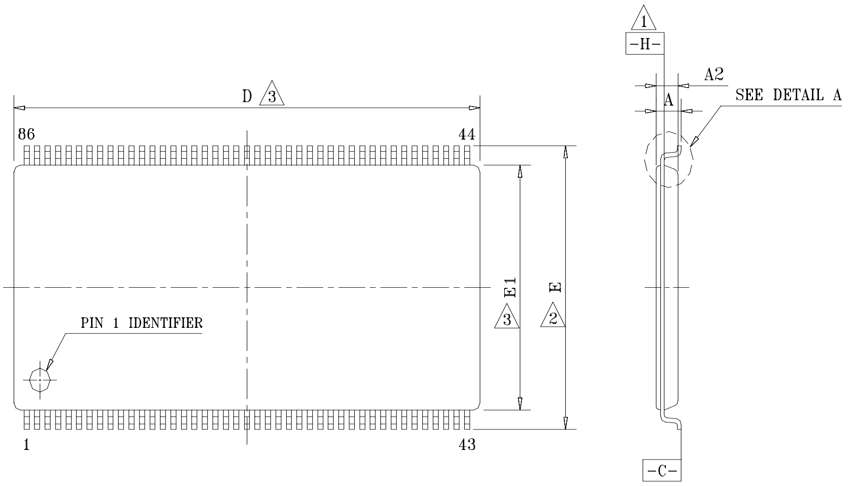
MODE REGISTER SET CYCLE

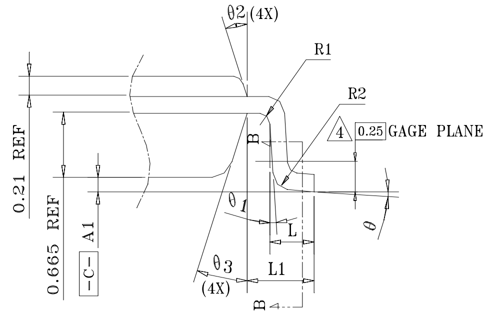
*Note: 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.

2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.

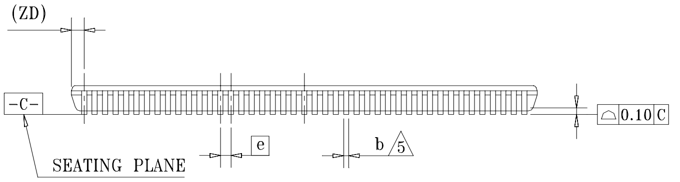
3. Please refer to Mode Register Set table.

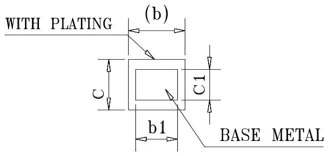
PACKING DIMENSIONS
86 - LEAD TSOP(II) DRAM(400mil)





DETAIL A



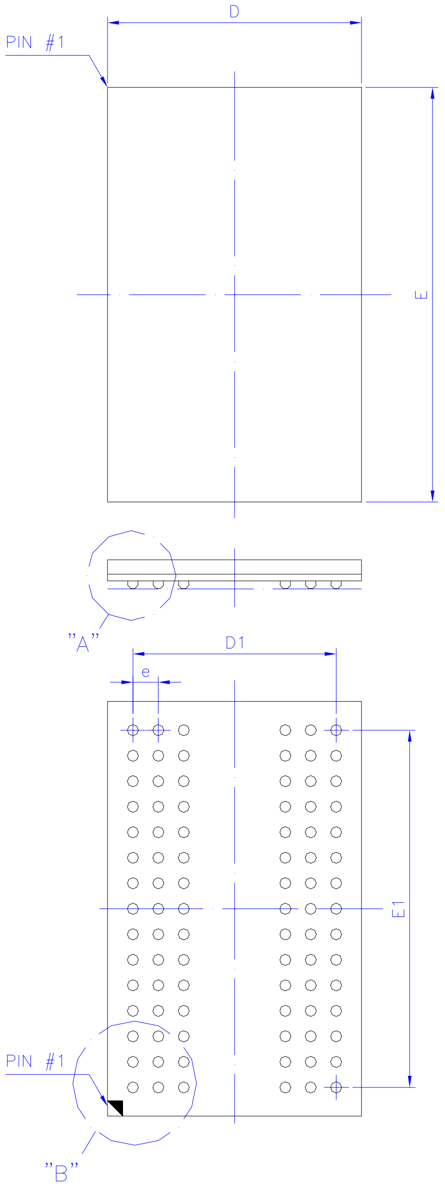


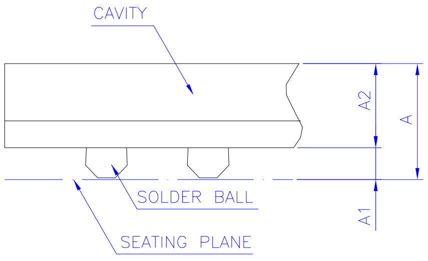
4 SECTION B-B

Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.20	—	—	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	—	0.27	0.007	—	0.018
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.12	—	0.21	0.005	—	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
ZD	0.61 REF			0.024 REF		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
e	0.50 BSC			0.020 BSC		
R1	0.12	—	—	0.005	—	—
R2	0.12	—	0.25	0.005	—	0.010
θ	0°	—	8°	0°	—	8°
θ 1	0°	—	—	0°	—	—
θ 2	10°	15°	20°	10°	15°	20°
θ 3	10°	15°	20°	10°	15°	20°

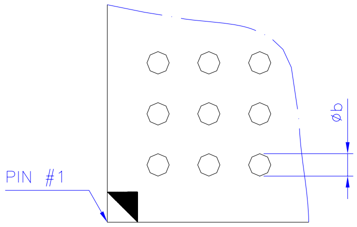
PACKING DIMENSIONS

90-BALL SDRAM (8x13 mm)





DETAIL : "A"



DETAIL : "B"

Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.00	—	—	0.039
A_1	0.30	0.35	0.40	0.012	0.014	0.016
A_2	—	0.586	—	—	0.023	—
$ø_b$	0.40	0.45	0.50	0.016	0.018	0.020
D	7.90	8.00	8.10	0.311	0.315	0.319
E	12.90	13.00	13.10	0.508	0.512	0.516
D_1	—	6.40	—	—	0.252	—
E_1	—	11.20	—	—	0.441	—
e	—	0.80	—	—	0.031	—

Controlling dimension : Millimeter.

Revision History

Revision	Date	Description
1.0	2016.02.05	Original

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