HT24LC256
CMOS 256K 2-Wire Serial EEPROM

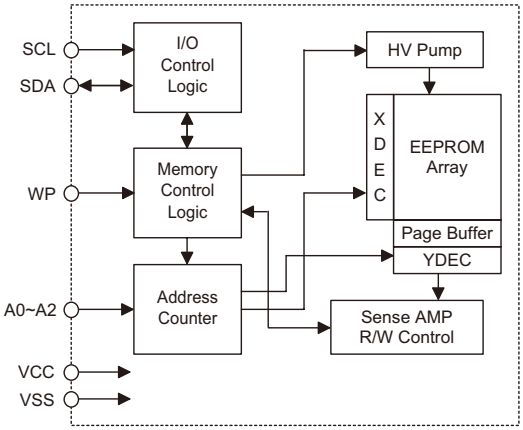
Features

- Operating voltage:
  2.2V~5.5V for Ta=-40˚C to +85˚C
- Memory Capacity: 256K (32K×8)
- 2-wire I^2C serial interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Partial page write allowed
- 64-byte Page write modes
- Write operation with built-in timer
- Hardware controlled write protection
- 40-year data retention
- 10^6 erase/write cycles per word
- 8-pin DIP/SOP/TSSOP package

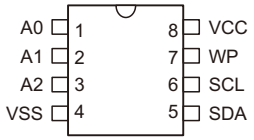
Description

The HT24LC256 device is a 256K-bit 2-wire serial read/write non-volatile memory device manufactured using a CMOS floating gate process. Its 256K bits of memory are organized into 32K words and each word is 8 bits. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. Up to eight HT24LC256 devices may be connected to the same two-wire bus. The HT24LC256 is guaranteed for 1M erase/write cycles and 40-year data retention.

Block Diagram



Pin Assignment



HT24LC256
8 DIP-A/SOP-A/TSSOP-A

Pin Description

Pin Name	Type	Description
A0~A2	I	Address inputs
SDA	I/O	Serial data
SCL	I	Serial clock input
WP	I	Write protect
VSS	PWR	Negative power supply, ground
VCC	PWR	Positive power supply

Absolute Maximum Ratings

Supply Voltage .....V_{SS}−0.3V to V_{SS}+3.0V
Input Voltage .....V_{SS}−0.3V to V_{CC}+0.3V
Storage Temperature .....-50°C to 125°C
Operating Temperature.....-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C Characteristics

Ta=-40ºC to 85ºC

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{CC}	Operating Voltage	—	—	2.2	—	5.5	V
I_{CC1}	Operating Current	5V	Read at 100kHz	—	—	2	mA
I_{CC2}	Operating Current	5V	Write at 100kHz	—	—	5	mA
V_{IL}	Input Low Voltage	—	—	-1	—	$0.3V_{CC}$	V
V_{IH}	Input High Voltage	—	—	$0.7V_{CC}$	—	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	2.4V	I_{OL}=2.1mA	—	—	0.4	V
I_{LI}	Input Leakage Current	5V	V_{IN}=0 or V_{CC}	—	0.1	2	μA
I_{LO}	Output Leakage Current	5V	V_{OUT}=0 or V_{CC}	—	0.1	1	μA
I_{STB1}	Standby Current	5V	V_{IN}=0 or V_{CC}	—	—	3	μA
I_{STB2}	Standby Current	2.2V	V_{IN}=0 or V_{CC}	—	—	2	μA
C_{IN}	Input Capacitance (See note)	—	f_{SK}=1MHz @ 25˚C	—	—	6	pF
C_{OUT}	Output Capacitance (See note)	—	f_{SK}=1MHz @ 25˚C	—	—	8	pF

Note: These parameters are periodically sampled but not 100% tested.

A.C Characteristics

Ta=-40ºC to 85ºC

Symbol	Parameter	Remark	V_{CC}=2.2~5.5V		V_{CC}=2.5~5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SK}	Clock Frequency	—	—	400	—	1000	kHz
t_{HIGH}	Clock High Time	—	600	—	400	—	ns
t_{LOW}	Clock Low Time	—	1200	—	600	—	ns
t_r	SDA and SCL Rise Time	Note	—	300	—	300	ns
t_f	SDA and SCL Fall Time	Note	—	300	—	300	ns
$t_{HD:STA}$	START Condition Hold Time	After this period the first clock pulse is generated	600	—	250	—	ns
$t_{SU:STA}$	START Condition Setup Time	Only relevant for repeated START condition	600	—	250	—	ns
$t_{HD:DAT}$	Data Input Hold Time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data Input Setup Time	—	150	—	100	—	ns
$t_{SU:STO}$	STOP Condition Setup Time	—	600	—	250	—	ns
t_{AA}	Output Valid from Clock	—	—	900	—	600	ns
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	1200	—	500	—	ns
t_{SP}	Input Filter Time (SDA and SCL Pins)	Noise suppression time	—	50	—	50	ns
t_{WR}	Write Cycle Time	—	—	5	—	5	ms
Endurance	25ºC, Page Mode	5.0V	1,000,000				Write Cycles

Note: These parameters are periodically sampled but not 100% tested. For relative timing, refer to timing diagrams.

Functional Description

Pin Function

- Serial clock – SCL
  The positive edge of the SCL input is used to clock data into the EEPROM device. The negative edge is used to clock data out of the device.
- Serial data – SDA
  The SDA pin is bidirectional for serial data transfer. The pin is open drain driven and may be wired-OR with any number of other open drain or open collector devices.
- Address Inputs – A0, A1, A2
  The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected. When the pins are hardwired, as many as eight 256K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). These inputs must be tied to VCC or VSS, to establish the device select code.
- Write protect – WP
  The device has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations connected to ground. When the write protect pin is connected to VCC, the write protection feature is enabled and operates as shown in the following table.

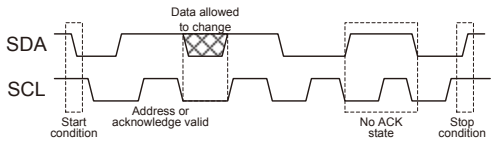
WP Pin Status	Protect Array
V_{CC}	Full Array – 256K
V_{SS} or floating	Normal Read/Write Operations

Memory Structure

The device is internally structured into 32K 8-bit words. A 15-bit data word address is required for word addressing.

Device Operation

- Clock and data transition
  Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a START or STOP condition.
- Start condition
  A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).
- Stop condition
  A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).
- Acknowledge
  All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.



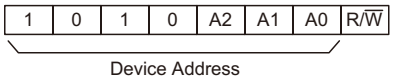
Start and Stop Definition Timing diagram

Device Addressing

The 256K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consists of a mandatory one, zero sequence for the first four most significant bits (refer to the diagram showing the Device Address). This is common to all the EEPROM devices.

The 256K EEPROM uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits are compared to their corresponding hardwired input pins.

The 8th bit device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. If the comparison of the device address is successful, the EEPROM will output a zero ACK bit. If not, the device will return to the standby state.



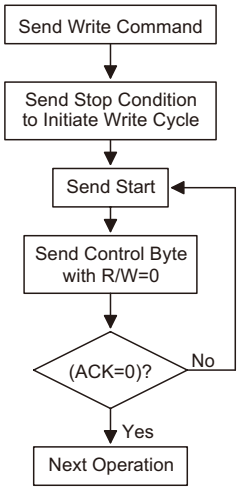
Device Adress

Write Operations

- Byte write
  A write operation requires two data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. After receiving the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM will execute an internally-timed write cycle to the non-volatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write operation is completed (refer to Byte write timing).

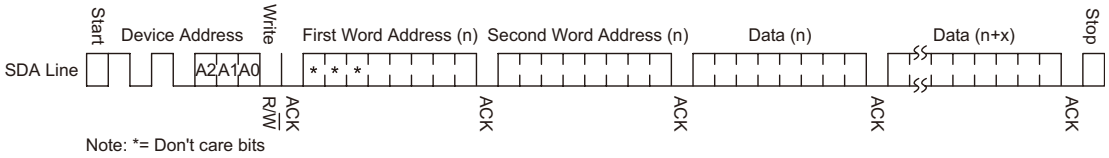
- Page write
  The 256K EEPROM is capable of a 64-byte page write. A page write is initiated in the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges the receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Page write timing). The data word address lower 6 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

- Acknowledge polling
  To maximize bus throughput, one technique is to allow the master to poll for an acknowledge signal after the start condition and the control byte for a write command has been sent. If the device is still busy implementing its write cycle, then no ACK will be returned. The master can send the next read/write command when the ACK signal has finally been received.



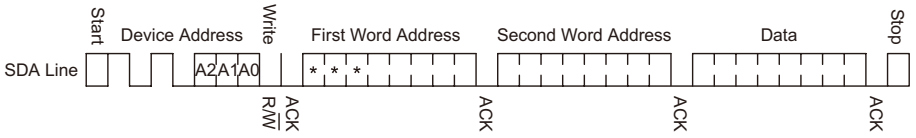
Acknowledge Polling Timing

- Write protect
  The HT24LC256 device has a write-protect function. Programming will be inhibited when the WP pin is connected to VCC. In this mode, the HT24LC256 device can be used as a serial ROM.



Note: *= Don't care bits

Page Write Timing

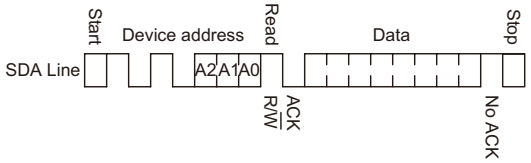


Byte Write Timing

Read Operations

The HT24LC256 device supports three read operations, namely, current address read, random address read and sequential read. During read operation execution, the read/write select bit should be set to "1".

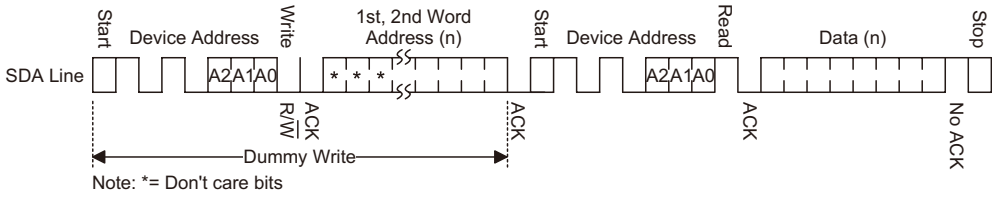
- Current address read
  The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address remains valid between operations as long as the chip power is maintained. The address will roll over during a read from the last byte of the last memory page to the first byte of the first page. The address will roll over during a write from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but generates a following stop condition (refer to Current read timing).



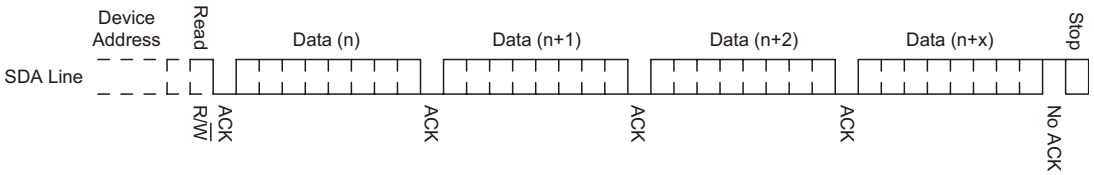
Current Address Read Timing

- Random read
  A random read requires a dummy byte write sequence to load in the data word address which is then clocked in and acknowledged by the EEPROM. The microcontroller must then generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller should respond with a "no ACK" signal (high) followed by a stop condition (refer to Random read timing).

- Sequential read
  Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgment. As long as the EEPROM receives an acknowledgment, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read continues. The sequential read operation is terminated when the microcontroller does not respond with a zero but generates a following stop condition.

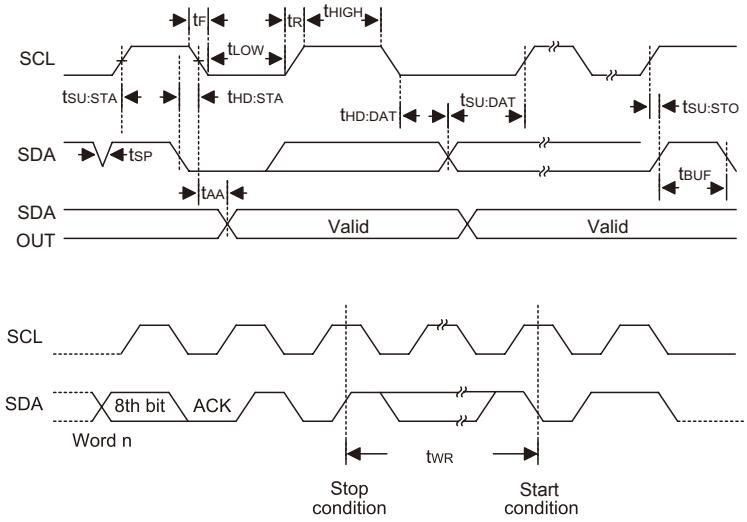


Random Read Timing



Sequential Read Timing

Timing Diagrams

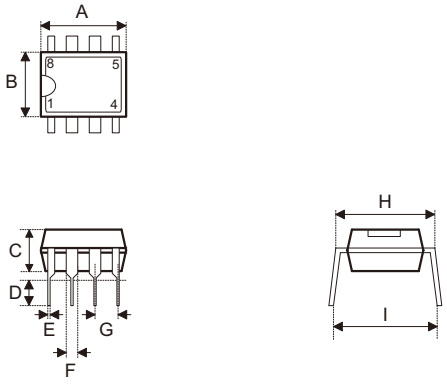


Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the valid start condition of sequential command.

Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website (http://www.holtek.com.tw/english/literature/package.pdf) for the latest version of the package information.

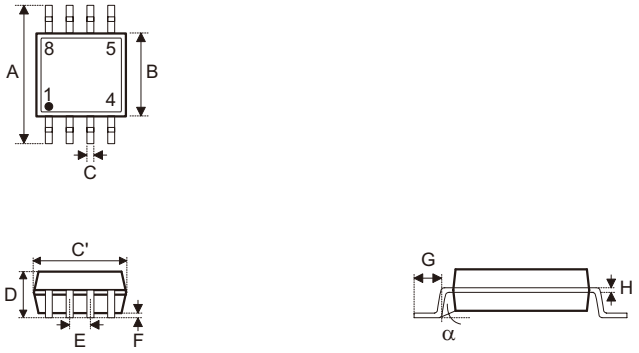
8-pin DIP (300mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.355	—	0.375
B	0.240	—	0.260
C	0.125	—	0.135
D	0.125	—	0.145
E	0.016	—	0.020
F	0.050	—	0.070
G	—	0.100	—
H	0.295	—	0.315
I	—	0.375	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.02	—	9.53
B	6.10	—	6.60
C	3.18	—	3.43
D	3.18	—	3.68
E	0.41	—	0.51
F	1.27	—	1.78
G	—	2.54	—
H	7.49	—	8.00
I	—	9.53	—

8-pin SOP (150mil) Outline Dimensions

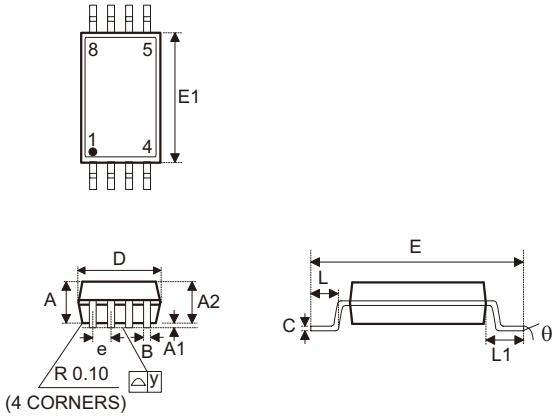


MS-012

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.012	—	0.020
C'	0.188	—	0.197
D	—	—	0.069
E	—	0.050	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.30	—	0.51
C'	4.78	—	5.00
D	—	—	1.75
E	—	1.27	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.18	—	0.25
α	0°	—	8°

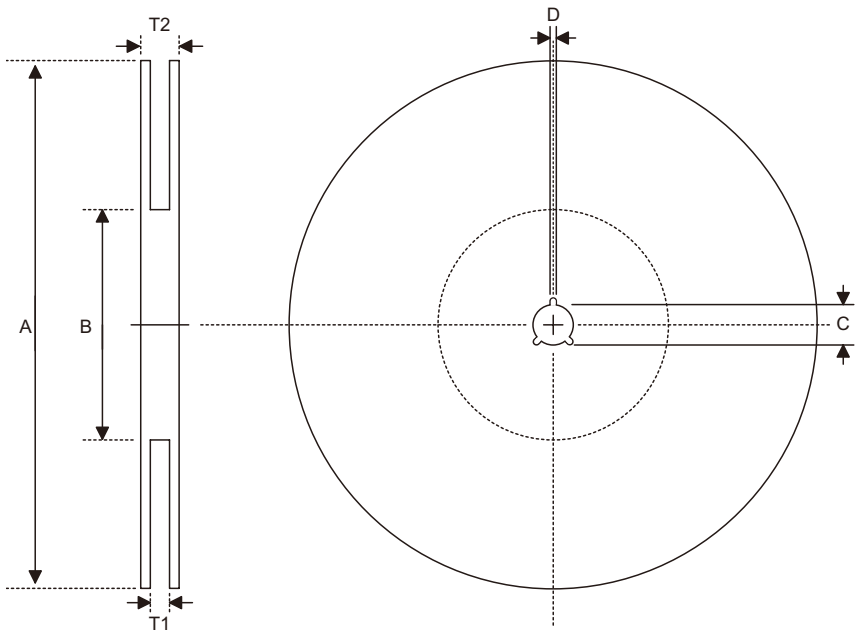
8-pin TSSOP Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.041	—	0.047
A1	0.002	—	0.006
A2	0.031	—	0.041
B	—	0.010	—
C	0.004	—	0.006
D	0.114	—	0.122
E	0.244	—	0.260
E1	0.169	—	0.177
e	—	0.026	—
L	0.020	—	0.028
L1	0.035	—	0.043
y	—	—	0.004
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	1.05	—	1.20
A1	0.05	—	0.15
A2	0.80	—	1.05
B	—	0.25	—
C	0.11	—	0.15
D	2.90	—	3.10
E	6.20	—	6.60
E1	4.30	—	4.50
e	—	0.65	—
L	0.50	—	0.70
L1	0.90	—	1.10
y	—	—	0.10
θ	0°	—	8°

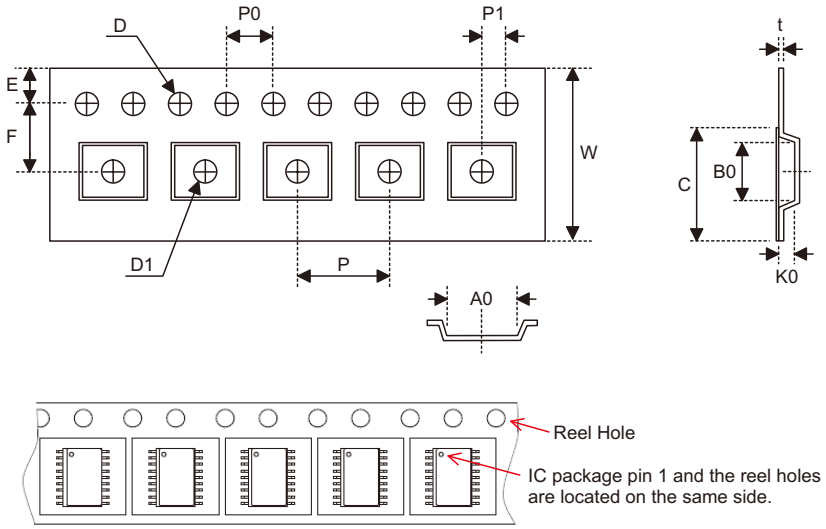
Reel Dimensions



SOP 8N, TSSOP 8L

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	$13.0^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	$12.8^{+0.3/-0.2}$
T2	Reel Thickness	18.2±0.2

Carrier Tape Dimensions



SOP 8N (150mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	$12.0^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	$1.50^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.2±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	9.3±0.1

TSSOP 8L

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	$12.0^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	5.5±0.5
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.5^{+0.1/-0.0}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	7.0±0.1
B0	Cavity Width	3.6±0.1
K0	Cavity Depth	1.6±0.1
t	Carrier Tape Thickness	0.300±0.013
C	Cover Tape Width	9.3±0.1

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