EMD12164PHW-xxx
8Mb x 16 bits x 4 Banks Mobile DDR SDRAM

GENERAL DESCRIPTION

The EMD51164P is 536,870,912 bits of double data rate synchronous DRAM organized as 4 banks of 8,388,608 words by 16 bits. The synchronous operation with Data Strobe allows extremely high performance. EMLSI is applied to reduce leakage and refresh currents while achieving very high speed. I/O transactions are possible on both edges of the clock. The ranges of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

FEATURES

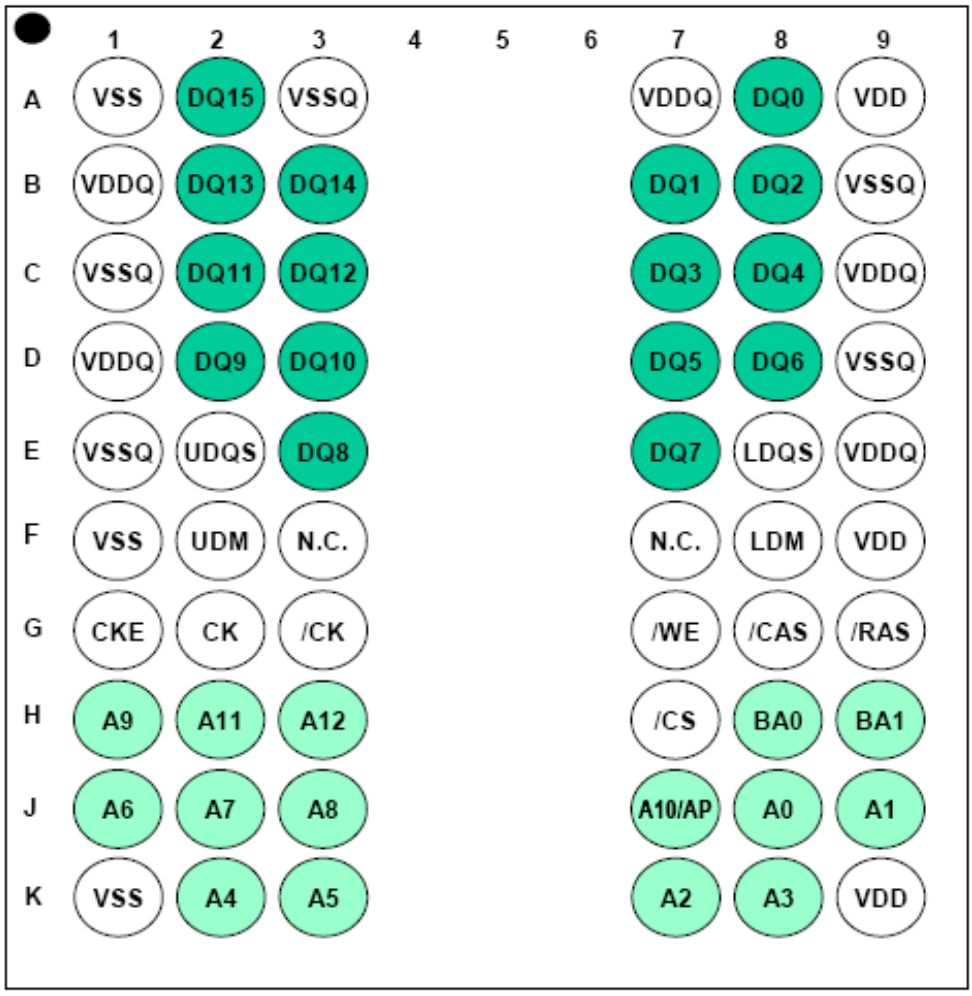
• EMLSI for low power at high speed
• JEDEC standard 1.8V power supply
• Double Data Rate architecture; two data transfers per clock cycle
• Bidirectional data strobe (DQS)
• Auto Refresh and Self Refresh
• Differential clock inputs (CK and /CK)
• All device pins are compatible with an LVCMOS interface
• 8K refresh cycles / 64ms
• Packages
- 60-Balls FpBGA
• Programmable Burst Length and Burst Type
- Burst Length : 2, 4, 8, or 16
- Burst Type : Sequential & Interleaved
• Programmable /CAS Latency : 3 clocks
• All inputs except data & DM are sampled at the positive going edge of the system clock (CK)
• Data I/O transactions on both edges of data strobe, DM for masking
• Edge-aligned data outputs, center-aligned data inputs
• Four-banks operation
• Special functions supported to reduce power
- PASR (Partial Array Self Refresh)
- Auto TCSR (Temperature Compensated Self Refresh)
- DS (Driver Strength)
• Deep Power Down mode
• No DLL (Delay Lock Loop), to reduce power; CK to DQS is not
synchronized.
• Operating temperature range
- Extended (-25 C to +85 C)

ORDERING INFORMATION

Part No.	Clock Freq.	Vdd/Vddq	Organization	Package
EMD12164PHW-60	DDR333 166MHz	1.8V/1.8V	8M x 16 Bits x 4 Banks	60-FpBGA

PIN CONFIGURATION

Top View

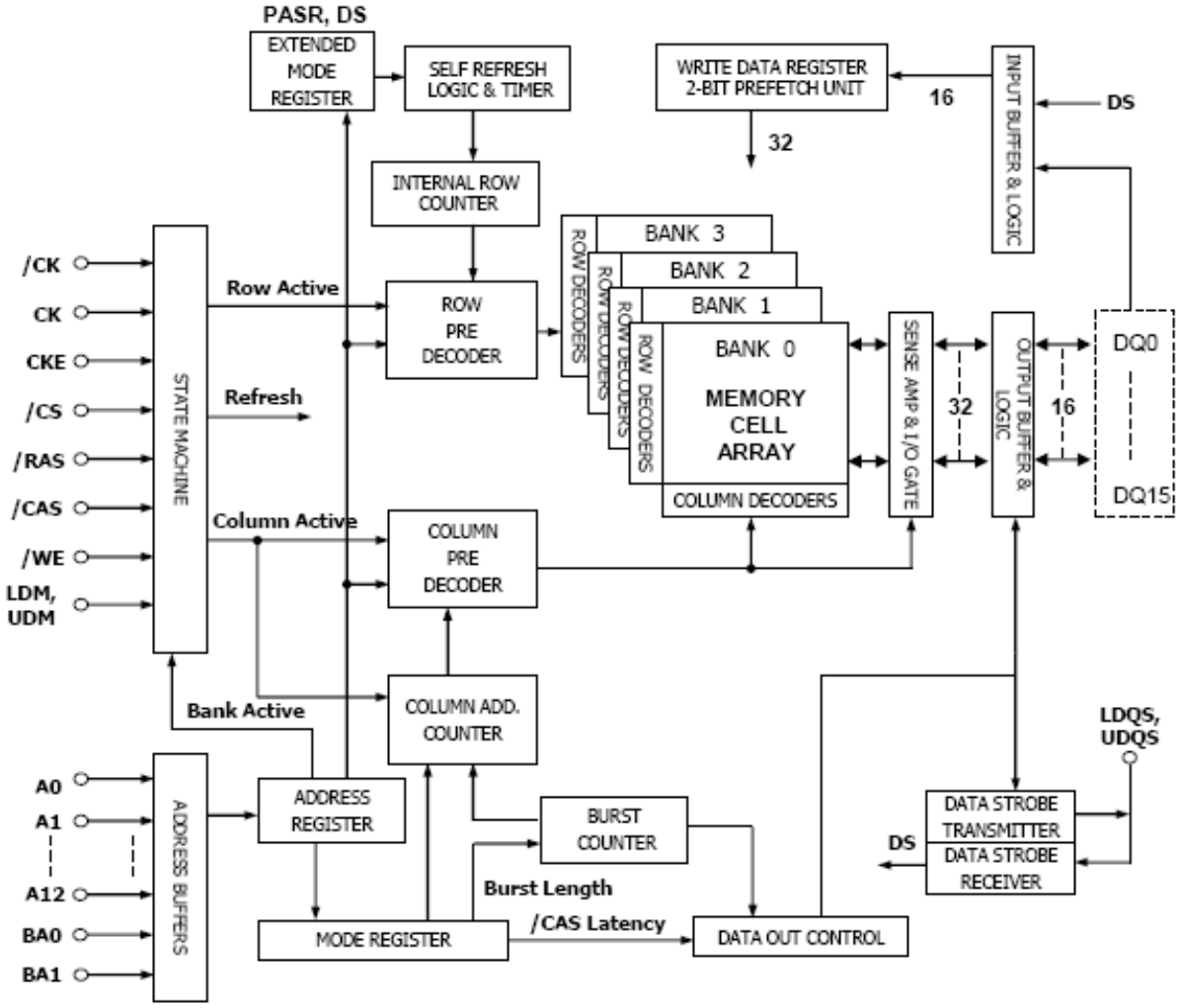


60-Ball FBGA

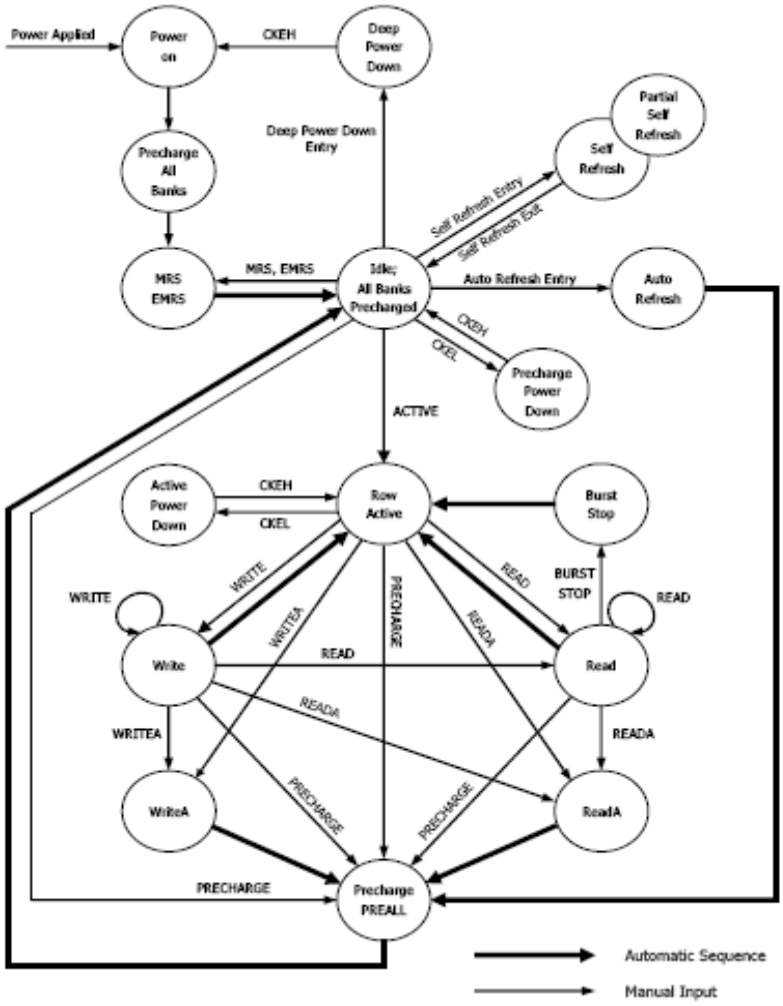
INPUT / OUTPUT FUNCTION DESCRIPTIONS

Pin	Pin Name	Description
CK, /CK	System Differential Clock	CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Input and output data is referenced to the crossing of CK and /CK (both directions of the crossing)
CKE	Clock Enable	CKE High activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self Refresh operation (all banks idle) or Active Power Down (Row Active in any bank). CKE is synchronous for all functions except for disabling outputs, which is asynchronous. Input buffers, excluding CK, /CK, and CKE, are disabled during Power Down and Self Refresh modes to reduce standby power consumption.
/CS	Chip Select	/CS enables (registered Low) and disables (registered High) the command decoder. All commands are masked when /CS is registered High. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
BA0, BA1	Bank Address	BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determine which mode register (MRS or EMRS) is loaded during a Mode Register Set command.
A0 ~ A12	Address	The address inputs provide the row address for Active commands and the column address and auto precharge bit (A10) for Read or Write commands, selecting one location out of the memory array in the respective bank. A10 sampled during a Precharge command determines whether the precharge applies to one bank (A10 Low) or all banks (A10 High). If only one bank is to be precharged, the bank is selected by BA0 and BA1. The address inputs also provide the Op Code during a Mode Register Set command. BA0 and BA1 determine which mode register (Mode Register or Extended Mode Register) is loaded during the Mode Register Set command.
/RAS, /CAS, /WE	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE (along with /CS) define the command being entered. Refer to the Function Truth Table for details.
LDM, UDM	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled High along with input data during a Write access. DM is sampled on both edges of DQS. DM pins include dummy parasitic loading internally to match the DQ and DQS loading. For x16, LDM is DM for DQ0-DQ7 and UDM is DM for DQ8-DQ15.
LDQS, UDQS	Data Strobe	DQS is an output with read data and an input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. For x16, LDQS is DQS for DQ0-DQ7 and UDQS is DQS for DQ8-DQ15.
DQ0 ~ DQ15	Data Input / Output	Multiplexed data input / output pins.
VDD / VSS	Power Supply / Ground	Power Supply and Ground for internal circuits and input buffers.
VDDQ / VSSQ	Data Output Power / Ground	Power Supply and Ground for output buffers.
NC	No Connection	No connection.

FUNCTIONAL BLOCK DIAGRAM



SIMPLIFIED STATE DIAGRAM



CKEH : Clock Enable Low-to-High Transition
CKEL : Clock Enable High-to-Low Transition
EMRS : Extended Mode Register Set
MRS : Mode Register Set

PREALL : Precharge All Banks
READA : Read with Auto Precharge
WRITEA : Write with Auto Precharge

Note: Use caution with this diagram. It is intended to provide an overview of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not captured in full detail.

BASIC FUNCTION DESCRIPTION

This 512Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the 134,217,728-bit banks is organized as 8,192 rows by 1024 columns by 16 bits. The 512Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high speed operation. EMLSI is applied to reduce leakage and refresh currents while achieving very high speed. The double data rate architecture is essentially a 2n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. Single read or write access for the 512Mb Mobile DDR SDRAM consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A12 select the row). The address bits (BA0, BA1 select the bank, A0-A9 select the column) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Note that the DLL (Delay Lock Loop) circuitry used on standard DDR devices is not included in the Mobile DDR SDRAM. It has been omitted to save power.
Prior to normal operation, the Mobile DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation

Power Up and Initialization

Mobile DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. To properly initialize the Mobile DDR SDRAM, this sequence must be followed:
1. To prevent device latch-up, it is recommended that core power (VDD) and I/O power (VDDQ) be from the same power source and be brought up simultaneously. If separate power sources are used, VDD must lead VDDQ.
2. Once power supply voltages are stable and CKE has been driven High, it is safe to apply the clock.
3. Once the clock is stable, a 200us (minimum) delay is required by the Mobile DDR SDRAM prior to applying an executable command.
During this time, NOP or Deselect commands must be issued on the command bus.
4. Issue a Precharge All command.
5. Issue NOP or Deselect commands for at least tRP time.
6. Issue an Auto Refresh command followed by NOP or Deselect commands for at least tRFC time. Issue a second Auto Refresh command followed by NOP or Deselect commands for at least tRFC time. As part of the individualization sequence, two Auto Refresh commands must be issued. Typically, both of these commands are issued at this stage as described above.
Alternately, the second Auto Refresh command and NOP or Deselect sequence can be issued between steps 10 and 11.
7. Using the Mode Register Set command, load the standard Mode Register as desired.
8. Issue NOP or Deselect commands for at least tMRD time.
9. Using the Mode Register Set command, load the Extended Mode Register to the desired operating modes.
Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or Deselect commands for at least tMRD time.
11. The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

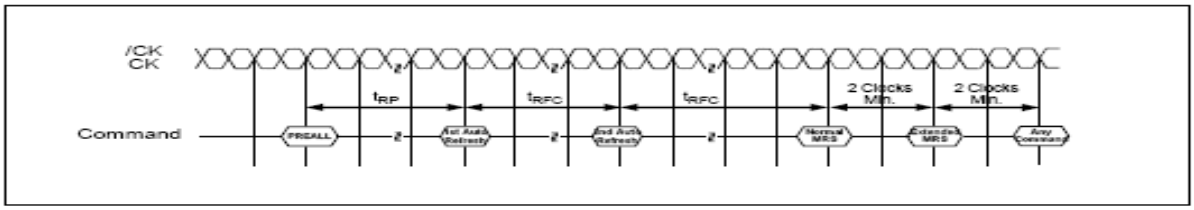


Figure.1 Power Up & Initialization Sequence

Mode Register Set(MRS)

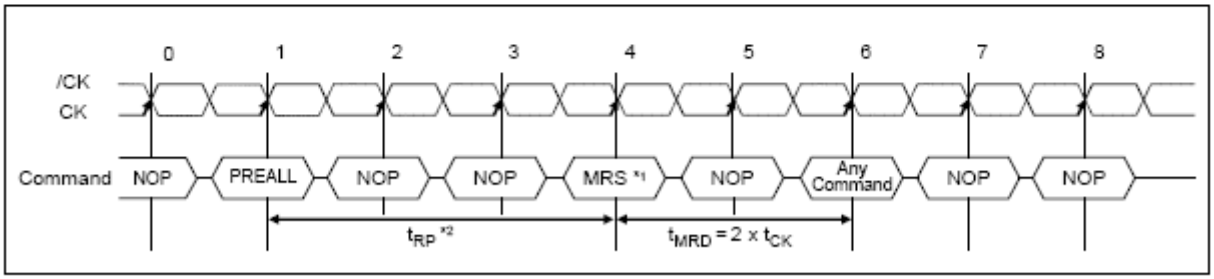
The Mode Register stores the data for controlling various operating modes of a DDR SDRAM. It programs /CAS Latency, Burst Type, and Burst Length to make the Mobile DDR SDRAM useful for a variety of applications. The default value of the Mode Register is not defined; therefore the Mode Register must be written by the user. Values stored in the register will be retained until the register is reprogrammed, the device enters Deep Power Down mode, or power is removed from the device. The Mode Register is written by asserting Low on /CS, /RAS, /CAS, /WE, BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of address pins A0~A12 and BA0, BA1 in the same cycle in which /CS, /RAS, /CAS and /WE are asserted Low is written into the Mode Register. A minimum of two clock cycles, tMRD, are required to complete the write operation in the Mode Register. The Mode Register is divided into various fields depending on functionality. The Burst Length uses A0~A2, Burst Type uses A3, and /CAS Latency (read latency from column address) uses A4~A6. A logic 0 should be programmed to all the undefined addresses to ensure future compatibility. Reserved states should not be used to avoid unknown device operation or incompatibility with future versions. Refer to the table for specific codes for various burst lengths, burst types and /CAS latencies.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	/CAS Latency			BT	Burst Length		

A3	Burst Type
0	Sequential
1	Interleaved

A6	A5	A4	/CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Length	
			A3 = 0	A3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	16	16
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved



* 1 : MRS can be issued only with all banks in the idle state.
* 2 : A minimum delay of t_{RP} is required before issuing an MRS command.

Figure.2 Mode Register Set Cycle

Extended Mode Register Set(EMRS)

The Extended Mode Register is designed to support Partial Array Self Refresh and Driver Strength. The EMRS cycle is not mandatory, and the EMRS command needs to be issued only when either PASR or DS is used. The Extended Mode Register is written by asserting Low on /CS, /RAS, /CAS, /WE, and BA0 and High on BA1 (the device should have all banks idle with no bursts in progress prior to writing into the Extended Mode Register, and CKE should be High). Values stored in the register will be retained until the register is reprogrammed, the device enters Deep Power Down mode, or power is removed from the device. The state of address pins A0~A12 and BA0, BA1 in the same cycle in which /CS, /RAS, /CAS and /WE are asserted Low is written into the Extended Mode Register. Two clock cycles, tMRD, are required to complete the write operation in the Extended Mode Register. A0~A2 are used for Partial Array Self Refresh and A5~A6 are used for Driver Strength. An automatic Temperature Compensated Self Refresh function is included with a temperature sensor embedded into this device. A3~A4 are no longer used to control this function; any inputs applied to A3~A4 during EMRS are ignored. All the other address pins, A7~A12 and BA0, must be set to Low for proper EMRS operation. Refer to the tables below for specific codes. If the user does not write values to the Extended Mode Register, DS defaults to Full Strength; and PASR defaults to the Full Array.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	DS		0	0	PASR		

A6	A5	Driver Strength
0	0	Full Strength
0	1	1/2 Strength
1	0	1/4 Strength
1	1	1/8 Strength

A2	A1	A0	Partial Array Self Refresh Coverage
0	0	0	Full Array (All Banks)
0	0	1	Half of Full Array (BA1 = 0)
0	1	0	Quarter of Full Array (BA1 = BA0 = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Mode Operation

Burst Mode operation is used to provide a constant flow of data to memory locations (write cycle) or from memory locations (read cycle). There are two parameters that define how the Burst Mode operates. These parameters include Burst Type and Burst Length and are programmed by addresses A0~A3 during the Mode Register Set command. Burst Type is used to define the sequence in which the burst data will be delivered from or stored to the DDR SDRAM. Two types of burst sequences are supported, Sequential and Interleaved. See the table below. The Burst Length controls the number of bits that will be output after a read command, or the number of bits to be input after a write command. The Burst Length can be programmed to have a value of 2, 4, 8, or 16.

Burst Length Sequence

Burst Length	Starting Addr. A3,A2,A1,a0	Sequential Mode	Interleaved Mode
2	XXX0	0-1	0-1
	XXX1	1-0	1-0
4	XX00	0-1-2-3	0-1-2-3
	XX01	1-2-3-0	1-0-3-2
	XX10	2-3-0-1	2-3-0-1
	XX11	3-0-1-2	3-2-1-0
8	X000	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	X001	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	X010	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	X011	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	X100	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	X101	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	X110	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	X111	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
16	0000	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15
	0001	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-0-3-2-5-4-7-6-9-8-11-10-13-12-15-14
	0010	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-0-1-6-7-4-5-10-11-8-9-14-15-12-13
	0011	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-2-1-0-7-6-5-4-11-10-9-8-15-14-13-12
	0100	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-0-1-2-3-12-13-14-15-8-9-10-11
	0101	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-4-7-6-1-0-3-2-13-12-15-14-9-8-11-10
	0110	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-4-5-2-3-0-1-14-15-12-13-10-11-8-9
	0111	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-15-14-13-12-11-10-9-8
	1000	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7
	1001	9-10-11-12-13-14-15-0-1-2-3-4-5-6-7-8	9-8-11-10-13-12-15-14-1-0-3-2-5-4-7-6
	1010	10-11-12-13-14-15-0-1-2-3-4-5-6-7-8-9	10-11-8-9-14-15-12-13-2-3-0-1-6-7-4-5
	1011	11-12-13-14-15-0-1-2-3-4-5-6-7-8-9-10	11-10-9-8-15-14-13-12-3-2-1-0-7-6-5-4
	1100	12-13-14-15-0-1-2-3-4-5-6-7-8-9-10-11	12-13-14-15-8-9-10-11-4-5-6-7-0-1-2-3
	1101	13-14-15-0-1-2-3-4-5-6-7-8-9-10-11-12	13-12-15-14-9-8-11-10-5-4-7-6-1-0-3-2
	1110	14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-12-13-10-11-8-9-6-7-4-5-2-3-0-1
	1111	15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-14-13-12-11-10-9-8-7-6-5-4-3-2-1-0

Bank Activation / Row Address Command

The Bank Activation / Row Address command, also called the Active command, is issued by holding /CAS and /WE High with /CS and /RAS Low at the rising edge of the clock (CK). The DDR SDRAM has four independent banks, so two Bank Select Addresses (BA0, BA1) are required. The Active command must be applied before any read or write operation is executed. The delay from the Active command to the first Read or Write command must meet or exceed the minimum of /RAS to /CAS delay time tRCDmin). Once a bank has been activated, it must be precharged before another Active command can be applied to the same bank. The minimum time interval between interspersed Active commands (Bank 0 to Bank 3, for example) is the bank to bank delay time (tRRD min).

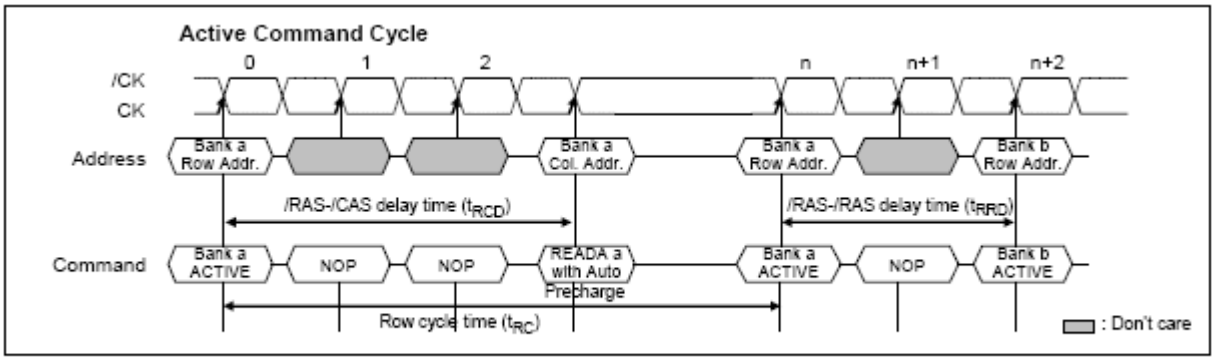


Figure.3 Bank Activation / Row Address (Active) command cycle timing

Burst Read Operation

Burst Read operation in a DDR SDRAM is initiated by asserting /CS and /CAS Low while holding /RAS and /WE High at the rising edge of the clock (CK) after tRCD from the Active command. The address inputs (A0~A9) determine the starting address for the Burst. The Mode Register sets the type of burst (Sequential or Interleaved) and the burst length (2, 4, 8, or 16). The first output data is available after the /CAS Latency from the Read command, and the consecutive data bits are presented on the falling and rising edges of Data Strobe (DQS) as supplied by the DDR SDRAM until the burst is completed.

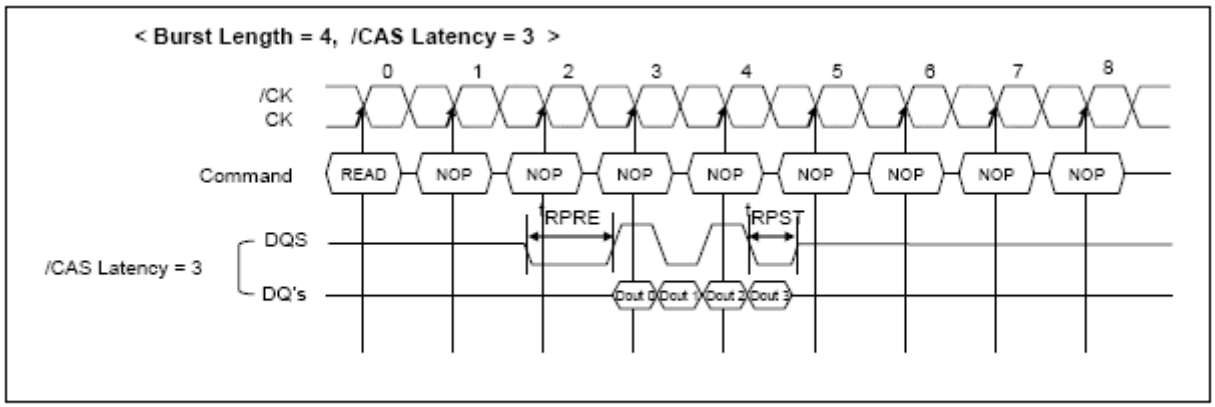


Figure.4 Burst Read Operation timing

Burst Write Operation

The Burst Write command is issued by having /CS, /CAS and /WE Low while holding /RAS High at the rising edge of the clock (CK). The address inputs determine the starting column address. There is no write latency relative to DQS required for the Burst Write cycle. The first data for a Burst Write cycle must be applied at the first rising edge of the data strobe enabled after tDQSS from the rising edge of the clock when the Write command was issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. After the burst has finished, any additional data supplied to the DQ pins will be ignored.

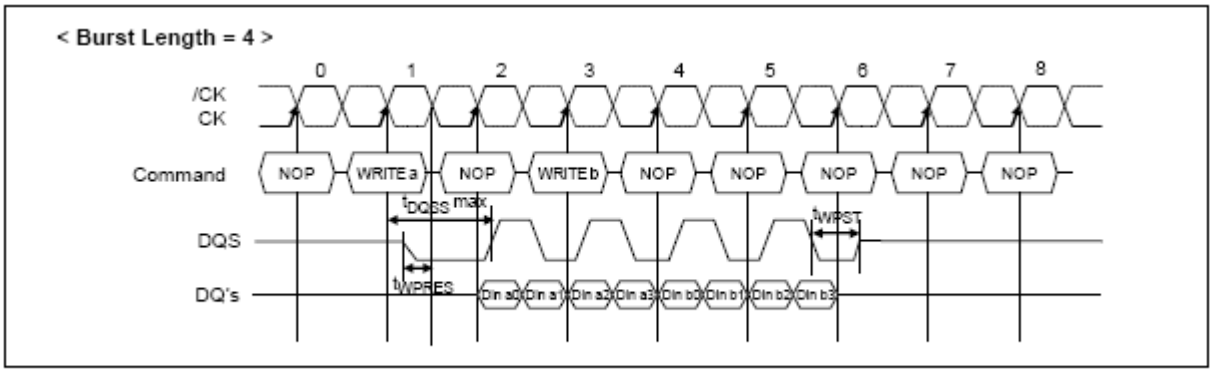


Figure.5 Burst Write operation timing

Burst Interruption

Read Interrupted by Read

Burst Read can be interrupted before completion of the burst by a new Read command to any bank. When the previous burst is interrupted, data bits from the remaining addresses are overridden by data from the new addresses with the full burst length. The data from the previous Read command continues to appear on the outputs until the /CAS latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. The Read to Read interval is a minimum of 1 clock.

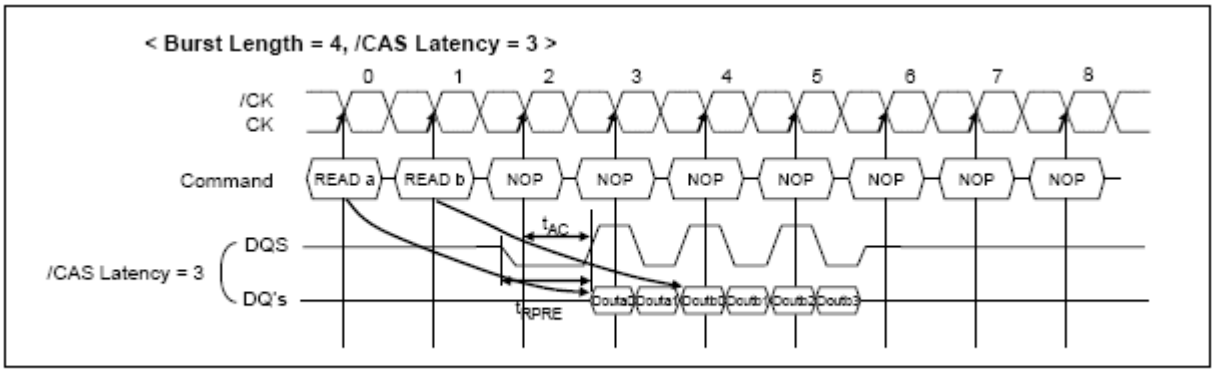


Figure.6 Read Interrupted by Read timing

Read Interrupted by Burst Stop & Write

To interrupt Burst Read with a write command, the Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's (output drivers) in a high impedance state. To ensure the DQ's are tri-stated one cycle before the beginning of the write operation, the Burst Stop command must be applied at least 2 clock cycles for CL = 2 and at least 3 clock cycles for CL = 3 before the Write command.

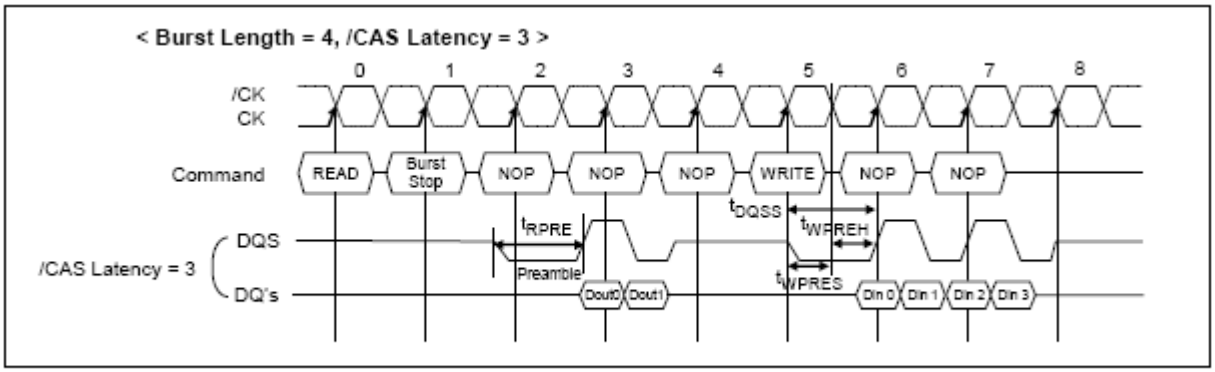


Figure.7 Read Interrupted by Burst Stop and Write timing

Read Interrupted by Precharge

Burst Read can be interrupted by a precharge of the same bank. A minimum of 1 clock cycle is required for the read precharge interval. A Precharge command to output disable latency is equivalent to the /CAS latency.

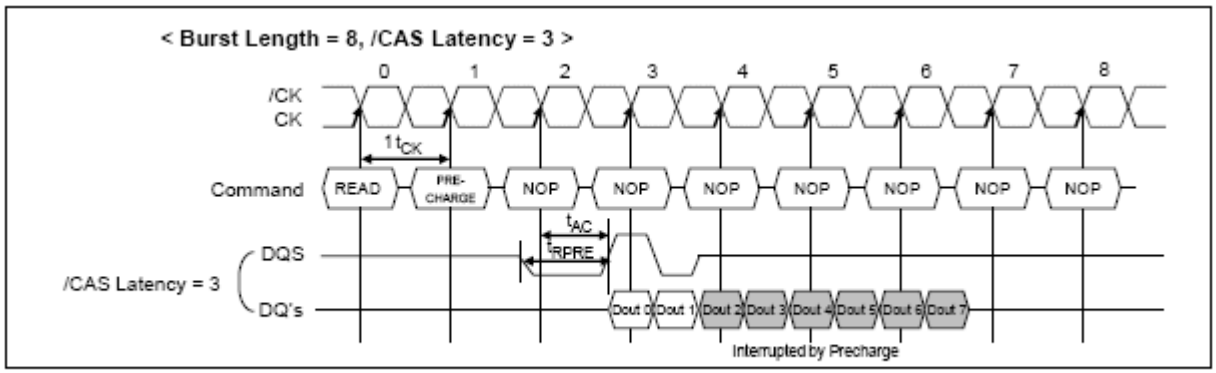


Figure. 8 Read Interrupted by Precharge timing

Write Interrupted by Write

A Burst Write can be interrupted by the new Write command before completion of the previous Burst Write, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new addresses and the new data will be written into the device until the programmed Burst Length is satisfied.

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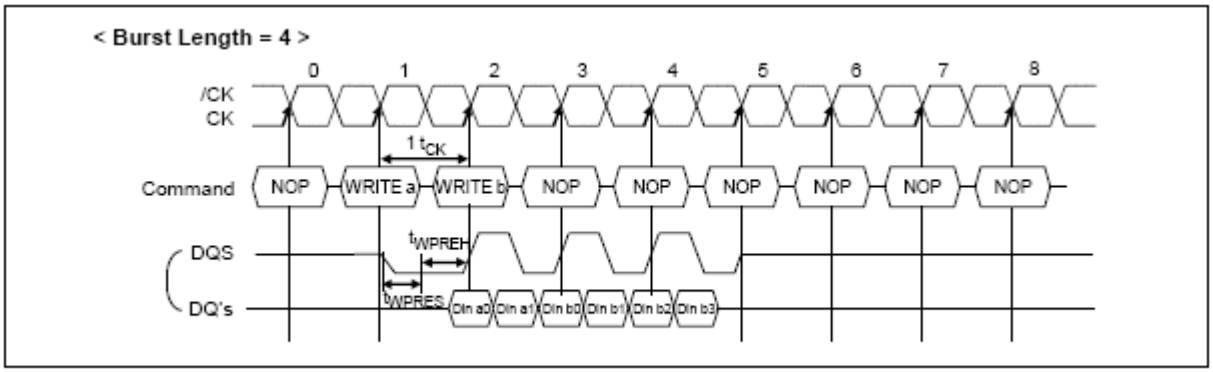


Figure.9 Write Interrupted by Write timing

Write Interrupted by Read & DM

A Burst Write can be interrupted by a Read command to any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appears on the outputs to avoid data contention. When the Read command is to be asserted, any residual data from the Burst Write sequence must be masked by DM. The delay from the last data to the Read command (tWTR) is required to avoid data contention inside the DRAM. Data presented on the DQ pins before the Read command is initiated will actually be written to the memory. A Read command interrupting a write sequence can not be issued at the next clock edge following the Write command.

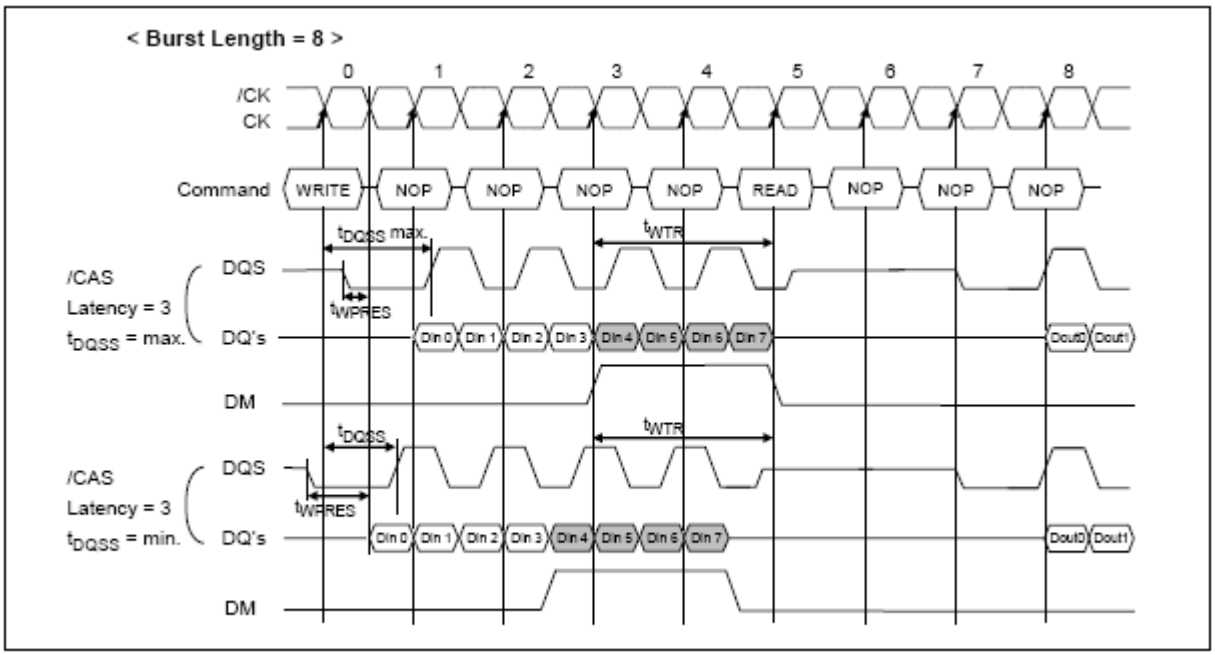


Figure.10 Write Interrupted by Read and DM timing

Write Interrupted by Precharge & DM

A Burst Write can be interrupted by a Precharge of the same bank before completion of the previous burst. A write recovery time (tWR) is required from the last data to the Precharge command. When the Precharge command is asserted, any residual data from the Burst Write cycle must be masked by DM.

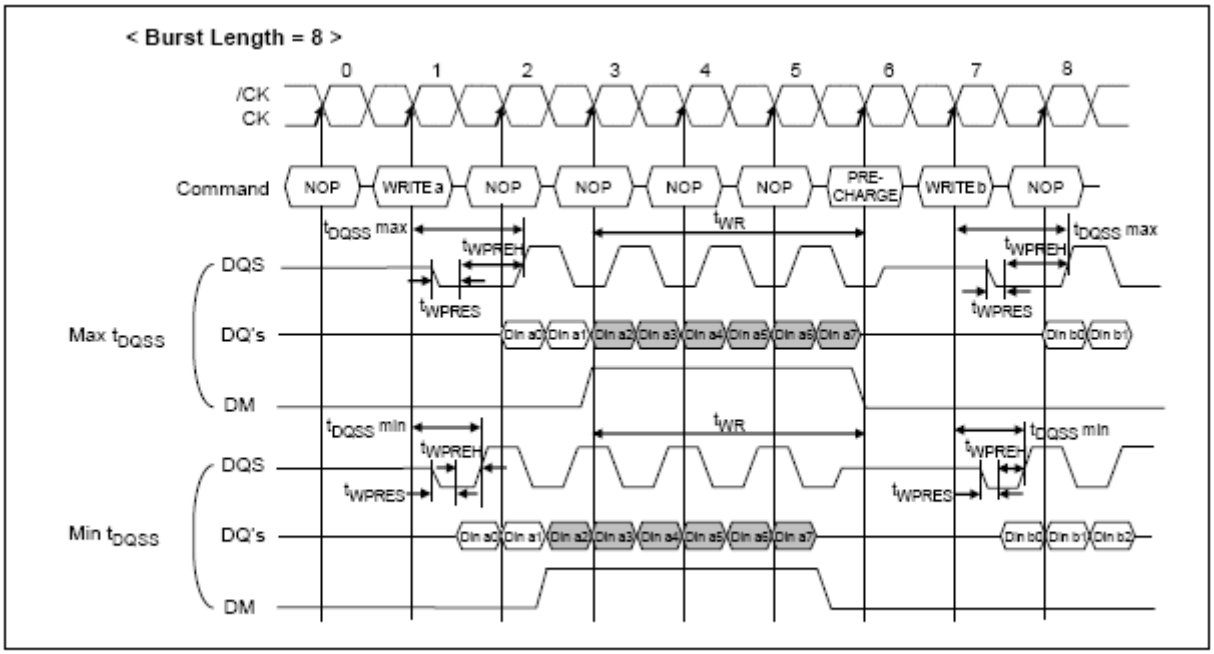


Figure.11 Write Interrupted by Precharge and DM timing

Burst Stop Command

The Burst Stop command is initiated by having /RAS and /CAS High with /CS and /WE Low at the rising edge of the clock only. The Burst Stop command has the fewest restrictions, making it the easiest method to use when terminating a burst operation before it has been completed. When the Burst Stop command is issued during a Burst Read cycle, both the data and DQS (Data Strobe) go to a high impedance state after a delay which is equal to the /CAS latency set in the Mode Register. The Burst Stop command, however, is not supported during a Burst Write operation.

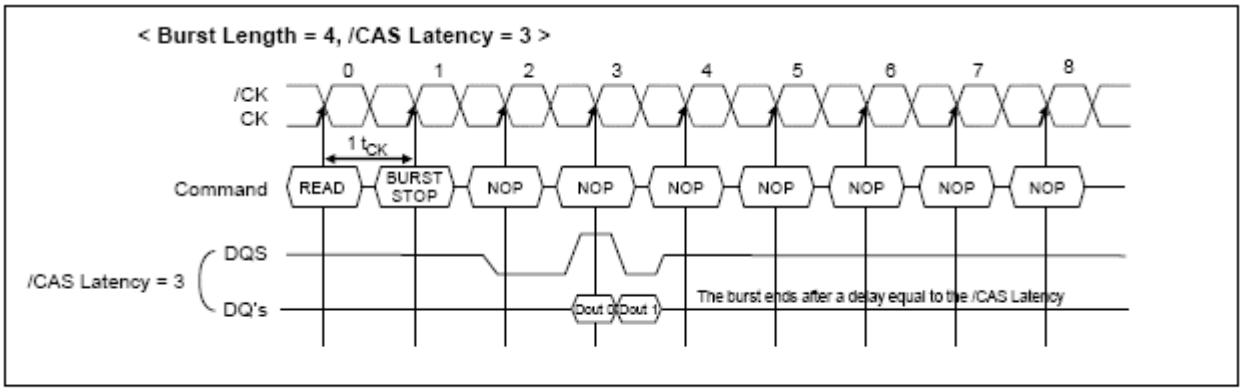


Figure.12 Burst Stop timing

DM Masking Function

The DDR SDRAM has a Data Mask function that can be used in conjunction with the data write cycle only, not the read cycle. When the Data Mask is activated (DM High) during a write operation, the write data is masked immediately (DM to Data Mask latency is zero). DM must be issued at the rising edge or the falling edge of Data Strobe instead of at a clock edge.

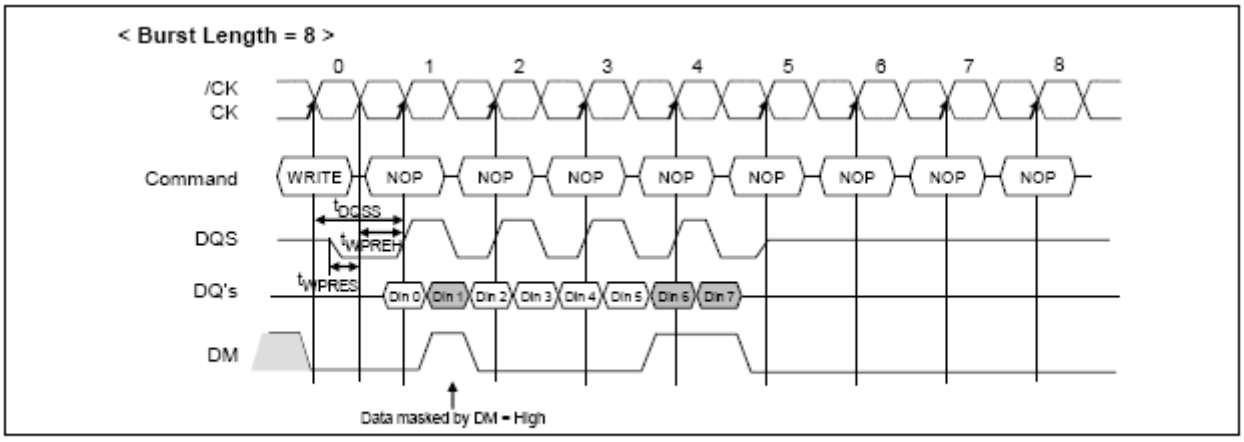


Figure.13 DM Masking timing

Auto Precharge Operation

The Auto Precharge command can be issued by having column address A10 High when a Read or a Write command is asserted to the DDR SDRAM. If A10 is Low when a Read or Write command is issued, normal Read or Write Burst operation is asserted and the bank remains active after the completion of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during a read or write cycle after tRAS (min) is satisfied.

Read with Auto Precharge

After a Read with Auto Precharge command is asserted, the DDR SDRAM automatically begins the precharge operation (Burst Length) ÷ 2 clock cycles later if tRAS (min) has also been satisfied at that point. If tRAS (min) has not been satisfied, the internal precharge operation will be delayed automatically until tRAS (min) is satisfied. Once the precharge operation has started, the bank cannot be reactivated or a new command asserted to that bank until the precharge time (tRP) has been satisfied.

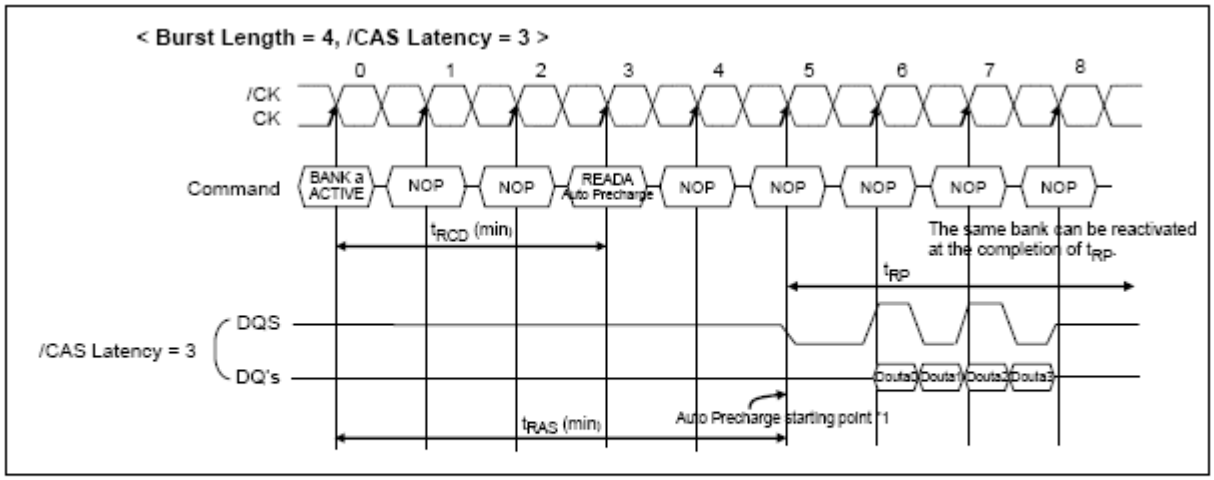


Figure.14 Read with Auto Precharge timing

Note : 1. An Active command to this bank being precharged can be issued after t_{RP} from this point.
A new Read or Write command to another activated bank can be issued from this point.

Write with Auto Precharge

If A10 is High when a Write command is issued, the Write with Auto Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after satisfying tWR (min).

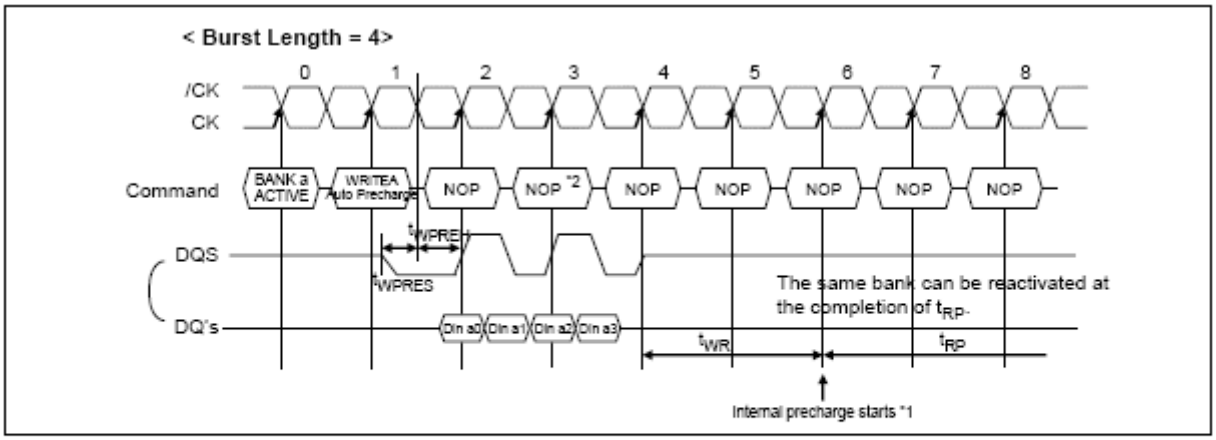


Figure.15 Write with Auto Precharge timing

Note : 1. An Active command to this bank being precharged can be issued after t_{RP} from this point.
2. A new Read or Write command to another activated bank can be issued from this point.

Precharge Command

The Precharge command is issued when /CS, /RAS, and /WE are Low and /CAS is High at the rising edge of the clock (CK). The Precharge command can be used to precharge any bank individually or all banks simultaneously. The Bank Select addresses (BA0, BA1) are used to define which bank is precharged when the command is initiated. For a write cycle, tWR (min) must be satisfied from the start of the last Burst Write cycle until the Precharge command can be issued. After tRP from the precharge, an Active command to the same bank can be initiated.

< Bank Selection for Precharge by Bank Address bits >

A10/AP	BA1	BA0	Precharge
0	0	0	Bank 0 only
0	0	1	Bank 1 only
0	1	0	Bank 2 only
0	1	1	Bank 3 only
1	X	X	All Banks

Auto Refresh

An Auto Refresh command is issued by having /CS, /RAS, and /CAS held Low with CKE and /WE High at the rising edge of the clock(CK). All banks must be precharged and idle for a tRP (min) before the Auto Refresh command is applied. The refresh addressing is generated by the internal refresh address counter. This makes the address bits “Don’t Care” during an Auto Refresh command. When the refresh cycle is complete, all banks will be in the idle state. A delay between the Auto Refresh command and the next Active command or subsequent Auto Refresh command must be greater than or equal to the tRFC (min).

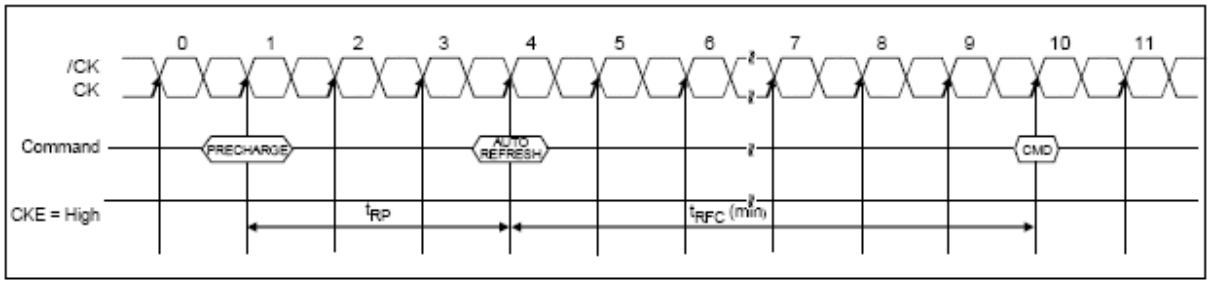


Figure.16 Auto Refresh timing

Self Refresh

A Self Refresh command is defined by having /CS, /RAS, /CAS and CKE Low with /WE High at the rising edge of the clock (CK). Once the Self Refresh command has been initiated, CKE must be held Low to keep the device in Self Refresh mode. During the Self Refresh operation, all inputs except CKE are ignored. The clock is internally disabled during Self Refresh operation to reduce power consumption. To exit the Self Refresh mode, supply a stable clock input before returning CKE high, assert Deselect or a NOP command and then assert CKE high.

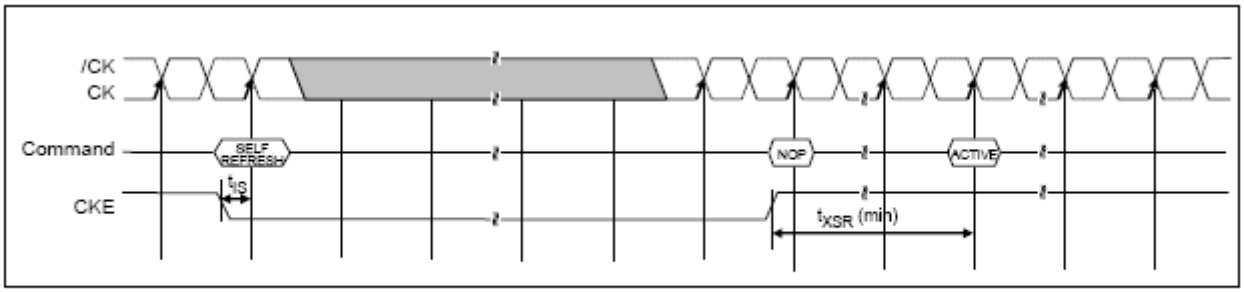


Figure.17 Self Refresh timing

Power Down Mode

The device enters Power Down mode when CKE is brought Low, and it exits when CKE returns High. Once the Power Down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. All banks should be in an idle state prior to entering the Precharge Power Down mode and CKE should be set high at least tXP prior to an Active command. During Power Down mode, refresh operations cannot be performed; therefore the device must remain in Power Down mode for a shorter time than the refresh period (tREF) of the device.

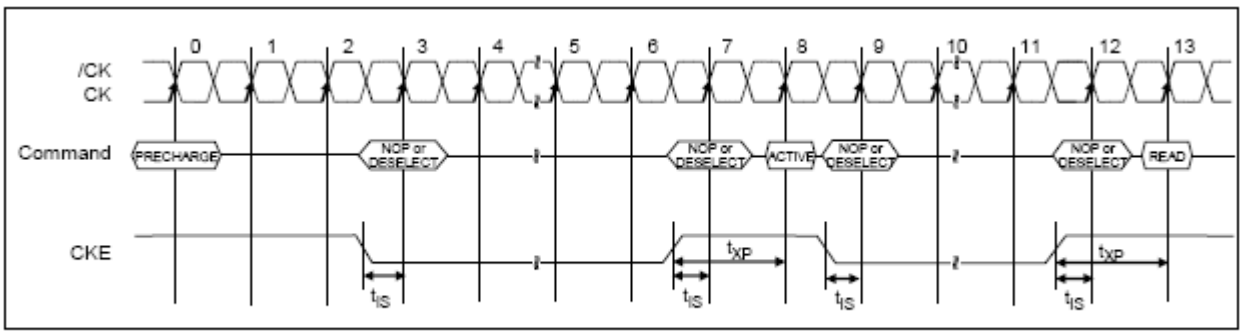


Figure.18 Power Down entry and exit timing

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DM	BA0, 1	A10/AP	A0~A9, A11, A12	Note
Register	Extended Mode Register		H	X	L	L	L	L	X	OP CODE			1, 2
	Mode Register Set		H	X	L	L	L	L	X	OP CODE			
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Active (Bank Activation & Row Address)			H	X	L	L	H	H	X	V	Row Address (A0~A12)		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 6
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		5
Burst Stop			H	X	L	H	H	L	X	X			7
Deep Power Down		Entry	H	L	L	H	H	L	X	X			
		Exit	L	H	H	X	X	X	X				
Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
DM			H	X					V	X			8
Deselect			H	X	H	X	X	X	X	X			9
No Operation Command (NOP)			H	X	L	H	H	H	X	X			

(V = Valid, X = Don't care, H = Logic High, L = Logic Low)

Note :
1. OP CODE : Operand Code.
   A0 ~ A12 & BA0 ~ BA1 : programmable inputs for the two Mode Registers.
2. EMRS / MRS can be issued only when all banks are in the precharge state
   A new command can be issued 2 clock cycles following either MRS or EMRS.
3. The Auto Refresh functions are the same as CBR (/CAS-Before-/RAS) refresh of standard DRAM.
   The automatic precharge without a Row Precharge command is meant by "Auto".
   Auto / Self Refresh can be issued only when all banks are in a precharge state.
4. BA0 ~ BA1 : Bank Select addresses.
   If both BA0 and BA1 are Low at Read, Write, Active or Precharge, bank 0 is selected.
   If BA0 is High and BA1 is Low at Read, Write, Active or Precharge, bank 1 is selected.
   If BA0 is Low and BA1 is High at Read, Write, Active or Precharge, bank 2 is selected.
   If both BA0 and BA1 are High at Read, Write, Active or Precharge, bank 3 is selected.
5. If A10/AP is High at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During Burst Read or Burst Write with Auto Precharge, a new Read or Write command cannot be issued.
   Another bank Read or Write command can be issued after the end of the burst.
   A new Active command to the associated bank can be issued after t_{RP} has been satisfied.
7. The Burst Stop command is valid for every Burst Length.
8. The DM inputs are sampled at both the rising and the falling edges of DQS (Write DM latency is 0).
9. The Deselect command is functionally equivalent to a NOP.

FUNCTION TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
Precharge Standby	L	H	H	L	X	BURST STOP	Illegal *2
	L	H	L	X	BA, CA, A10/AP	READ / WRITE	Illegal *2
	L	L	H	H	BA, RA	ACTIVE	Activate bank, latch RA
	L	L	H	L	BA, A10/AP	PRE / PREALL	Illegal *4
	L	L	L	H	X	REFRESH	Auto Refresh *5
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Mode Register Set *5
Active Standby	L	H	H	L	X	BURST STOP	NOP
	L	H	L	H	BA, CA, A10/AP	READ / READA	Begin Read, latch CA, determine Auto Precharge action
	L	H	L	L	BA, CA, A10/AP	WRITE / WRITEA	Begin Write, Latch CA, determine Auto Precharge action
	L	L	H	H	BA, RA	ACTIVE	Activate bank / Illegal *2
	L	L	H	L	BA, A10/AP	PRE / PREALL	Precharge / Precharge All
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal
Read	L	H	H	L	X	BURST STOP	Terminate burst
	L	H	L	H	BA, CA, A10/AP	READ / READA	Terminate burst, latch CA, begin new Read, determine Auto Precharge action *3
	L	H	L	L	BA, CA, A10/AP	WRITE / WRITEA	Illegal
	L	L	H	H	BA, RA	ACTIVE	Activate bank / Illegal *2
	L	L	H	L	BA, A10/AP	PRE / PREALL	Terminate burst, precharge
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal
Write	L	H	H	L	X	BURST STOP	Illegal
	L	H	L	H	BA, CA, A10/AP	READ / READA	Terminate burst with DM = High, latch CA, begin Read, determine Auto Precharge action *3
	L	H	L	L	BA, CA, A10/AP	WRITE / WRITEA	Terminate burst, latch CA, begin new Write, determine precharge action *3
	L	L	H	H	BA, RA	ACTIVE	Activate bank / Illegal *2
	L	L	H	L	BA, A10/AP	PRE / PREALL	Terminate burst with DM = High, precharge
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal
Read with Auto Precharge	L	H	H	L	X	BURST STOP	Illegal
	L	H	L	X	BA, CA, A10/AP	READ / WRITE	Illegal *2
	L	L	H	H	BA, RA	ACTIVE	Illegal *2
	L	L	H	L	BA, A10/AP	PRE / PREALL	Illegal *2
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal
Write with Auto Precharge	L	H	H	L	X	BURST STOP	Illegal
	L	H	L	X	BA, CA, A10/AP	READ / WRITE	Illegal *2
	L	L	H	H	BA, RA	ACTIVE	Illegal *2
	L	L	H	L	BA, A10/AP	PRE / PREALL	Illegal *2
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
Precharging	L	H	H	L	X	BURST STOP	Illegal *2
	L	H	L	X	BA, CA, A10/AP	READ / WRITE	Illegal *2
	L	L	H	H	BA, RA	ACTIVE	Illegal *2
	L	L	H	L	BA, A10/AP	PRE / PREALL	NOP *4 (idle after t_{RP})
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal
Row Activating	L	H	H	L	X	BURST STOP	Illegal *2
	L	H	L	X	BA, CA, A10/AP	READ / WRITE	Illegal *2
	L	L	H	H	BA, RA	ACTIVE	Illegal *2
	L	L	H	L	BA, A10/AP	PRE / PREALL	Illegal *2
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal
Write Recovering	L	H	H	L	X	BURST STOP	Illegal *2
	L	H	L	H	BA, CA, A10/AP	READ	Illegal *2
	L	H	L	L	BA, CA, A10/AP	WRITE / WRITEA	New Write, determ. Auto Pre. action
	L	L	H	H	BA, RA	ACTIVE	Illegal *2
	L	L	H	L	BA, A10/AP	PRE / PREALL	Illegal *2
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal
Refreshing	L	H	H	L	X	BURST STOP	Illegal
	L	H	L	X	BA, CA, A10/AP	READ / WRITE	Illegal
	L	L	H	H	BA, RA	ACTIVE	Illegal
	L	L	H	L	BA, A10/AP	PRE / PREALL	Illegal
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal
Mode Register Setting	L	H	H	L	X	BURST STOP	Illegal
	L	H	L	X	BA, CA, A10/AP	READ / WRITE	Illegal
	L	L	H	H	BA, RA	ACTIVE	Illegal
	L	L	H	L	BA, A10/AP	PRE / PREALL	Illegal
	L	L	L	H	X	REFRESH	Illegal
	L	L	L	L	Op Code, Mode Reg. inputs	MRS	Illegal

ABBREVIATIONS :

H = High Level, L = Low Level, V = Valid, X = Don't care

BA = Bank Address, RA = Row Address, CA = Column Address, NOP = No Operation

PRE = Precharge, PREALL = Precharge All, MRS = Mode Register Set

READA = Read with Auto Precharge, WRITEA = Write with Auto Precharge

Note :

1. All entries assume that CKE was High during the preceding clock cycle and remains High in the current clock cycle.
2. Illegal for the bank in the specified state; the function may be legal in another bank specified by BA, depending on the state of that bank.
3. The timing must satisfy bus contention, bus turn-around, and write recovery requirements.
4. This command functions as a NOP to a bank precharging or in the idle state, but the system may precharge another bank indicated by BA.
5. Illegal if any bank is not idle.
6. The same bank's previous Auto Precharge will not be performed. But if the bank is different, the previous Auto Precharge will be performed.

Illegal = Device operation and/or data integrity are not guaranteed.

FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Address	Action
Self-Refreshing	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Self Refresh *1
	L	H	L	H	H	H	X	Exit Self Refresh *1
	L	H	L	H	H	L	X	Illegal
	L	H	L	H	L	X	X	Illegal
	L	H	L	L	X	X	X	Illegal
	L	L	X	X	X	X	X	NOP (maintain Self Refresh)
Power Down	H	X	X	X	X	X	X	Invalid
	L	H	X	X	X	X	X	Exit Power Down *2
	L	L	X	X	X	X	X	NOP (maintain Power Down)
Deep Power Down	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Deep Power Down *5
	L	L	X	X	X	X	X	NOP (maintain Deep Power Down)
All Banks Idle	H	H	X	X	X	X	X	Refer to the previous Function Truth Table
	H	L	H	X	X	X	X	Enter Power Down *3
	H	L	L	H	H	H	X	Enter Power Down *3
	H	L	L	H	H	L	X	Enter Deep Power Down
	H	L	L	H	L	X	X	Illegal
	H	L	L	L	H	H	BA, RA	Activate a bank and latch the row address
	H	L	L	L	L	H	X	Enter Self Refresh *4
	H	L	L	L	L	L	OP Code	Access the Mode Register
	L	X	X	X	X	X	X	Refer above to Current State = Power Down
Any State other than those listed above	H	H	X	X	X	X	X	Refer to the previous Function Truth Table

ABBREVIATIONS :

H = High Level, L = Low Level, V = Valid, X = Don't care

NOP = No Operation, OP = Operation; the OP Code is the set of Mode Register inputs

Note :

1. After CKE makes a Low to High transition to exit Self Refresh mode. Additionally, a time of t_{RC} (min) must elapse after CKE makes a Low to High transition before issuing a new command.
2. The CKE Low to High transition is asynchronous; this transition restarts the internal clock. A minimum setup time of t_{XP} must be satisfied before any command other than the exit from Power Down.
3. Precharge Power Down can be entered only when all banks are idle. If at least one bank is active, the power down state will be Active Power Down.
4. Self Refresh can be entered only when all banks are idle.
5. The CKE Low to High transition is asynchronous. The clock must be stable before this CKE transition. NOP commands must be maintained for at least 200us followed by steps 4 through 11 of the Power Up and Initialization sequence.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 ~ 2.3	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 ~ 2.3	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.3	V
Storage temperature	T_{STG}	-55 to +125	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

Note :

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
2. Functional operation should be restricted to Recommended Operating Conditions.
3. Exposure to higher than the recommended voltages for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS

Recommended Operating Conditions (voltages referenced to VSS = 0V, TA = -25°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device supply voltage	V_{DD}	1.70	1.80	1.90	V	
Output supply voltage	V_{DDQ}	1.70	1.80	1.90	V	
Input logic high voltage	V_{IH}	0.8 x V_{DDQ}	-	V_{DDQ} + 0.30	V	1
Input logic low voltage	V_{IL}	-0.30	-	0.3x V_{DDQ}	V	1
Output logic high voltage	V_{OH}	0.9 x V_{DDQ}	-	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL}	-	-	0.1 x V_{DDQ}	V	I_{OL} = +0.1mA
Input leakage current	I_{IL}	-2	-	2	uA	
Output leakage current	I_{OL}	-5	-	5	uA	

Note :

1. This parameter should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.

DC Characteristics 1 (TJ = –25°C to +85°C, VDD and VDDQ = 1.7V to 1.9V, VSS and VSSQ = 0V)

Parameter	Symbol	Speed	×16 max.	×32 max.	Unit	Test condition	Notes
Operating current	IDD1	166MHz 133MHz	70 60	80 70	mA	Burst length = 2 tRC ≥ tRC (min.), IO = 0mA, One bank active	1
Standby current in power-down	IDD2P		0.8	0.8	mA	CKE ≤ VIL (max.), tCK = tCK (min.)	
Standby current in power-down (input signal stable)	IDD2PS		0.6	0.6	mA	CKE ≤ VIL (max.), tCK = ∞	
Standby current in non power-down	IDD2N	166MHz 133MHz	5.0 4.0	5.0 4.0	mA	CKE ≥ VIH (min.), tCK = tCK (min.), /CS ≥ VIH (min.), Input signals are changed one time during 2tCK.	
Standby current in non power-down (input signal stable)	IDD2NS		2.0	2.0	mA	CKE ≥ VIH (min.), tCK = ∞, Input signals are stable.	
Active standby current in power-down	IDD3P		3.0	3.0	mA	CKE ≤ VIL (max.), tCK = tCK (min.)	
Active standby current in power-down (input signal stable)	IDD3PS		2.0	2.0	mA	CKE ≤ VIL (max.), tCK = ∞	
Active standby current in non power-down	IDD3N		10	10	mA	CKE ≥ VIH (min.), tCK = tCK (min.), /CS ≥ VIH (min.), Input signals are changed one time during 2tCK.	
Active standby current in non power-down (input signal stable)	IDD3NS		7.0	7.0	mA	CKE ≥ VIH (min.), tCK = ∞, Input signals are stable.	
Burst operating current	IDD4	166MHz 133MHz	120 90	150 120	mA	Burst length = 4 tCK ≥ tCK (min.), IOUT = 0mA, All banks active	2
Refresh current	IDD5		90	90	mA	tRFC ≥ tRFC (min.)	3
Standby current in deep power-down mode	IDD7		10	10	µA	CKE ≤ 0.2V	

Advanced Data Retention Current (TJ = –25°C to +85°C, VDD and VDDQ = 1.7V to 1.9V, VSS and VSSQ = 0V)

Parameter	Symbol	Grade	typ.	max.	Unit	Condition	Notes
Advanced data retention current (Self-refresh current) PASR="000" (Full)	IDD6		—	250	µA	–25°C ≤ TJ ≤ +40°C CKE ≤ 0.2V	
PASR="001" (2BK)			—	220	µA		
PASR="010" (1BK)			—	200	µA		
PASR="000" (Full)	IDD6		—	480	µA	+40°C < TJ ≤ +70°C	
PASR="001" (2BK)			—	350	µA	CKE ≤ 0.2V	
PASR="010" (1BK)			—	280	µA		
PASR="000" (Full)	IDD6		—	600	µA	+70°C < TJ ≤ +85°C	
PASR="001" (2BK)			—	400	µA	CKE ≤ 0.2V	
PASR="010" (1BK)			—	300	µA		

Notes: 1. IDD1 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, IDD1 is measured on condition that addresses are changed only one time during tCK (min.).
2. IDD4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, IDD4 is measured on condition that addresses are changed only one time during tCK (min.).
3. IDD5 is measured on condition that addresses are changed only one time during tCK (min.).

DC Characteristics 2 (TJ = –25°C to +85°C, VDD and VDDQ = 1.7V to 1.9V, VSS and VSSQ = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–2.0	2.0	µA	0 ≤ VIN ≤ VDDQ	
Output leakage current	ILO	–1.5	1.5	µA	0 ≤ VOUT ≤ VDDQ, DQ = disable	
Output high voltage	VOH	0.9 × VDDQ	—	V	IOH = – 0.1mA	
Output low voltage	VOL	—	0.1 × VDDQ	V	IOL = 0.1 mA	

Pin Capacitance (TA = +25°C, VDD and VDDQ = 1.7V to 1.9V)

Parameter	Symbol	Pins	min.	typ.	max.	Unit	Notes
Input capacitance	CI1	CK, /CK	1.5	—	3.5	pF	1
	CI2	All other input-only pins	1.5	—	3.0	pF	1
Delta input capacitance	Cdi1	CK, /CK	—	—	0.25	pF	1
	Cdi2	All other input-only pins	—	—	0.5	pF	1
Data input/output capacitance	CI/O	DQ, DM, DQS	2.0	—	4.5	pF	1, 2,
Delta input/output capacitance	Cdio	DQ, DM, DQS	—	—	0.5	pF	1

Notes: 1. These parameters are measured on conditions: f = 100MHz, VOUT = VDDQ/2, ΔVOUT = 0.2V, TA = +25°C.
2. DOUT circuits are disabled.

AC INPUT OPERATING CONDITIONS

Recommended Operating Conditions (voltages referenced to VSS = 0V, TA = -25°C to +85°C)

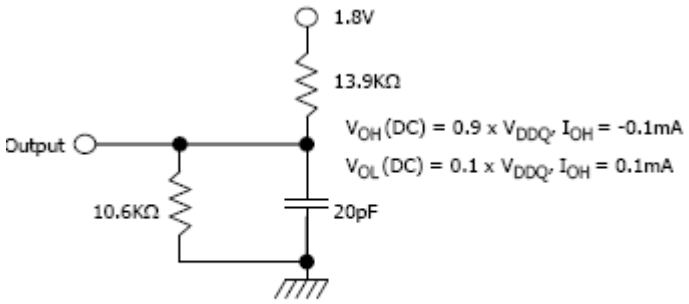
Parameter	Symbol	Min	Typ	Max	Unit	Note
Input high (logic 1) voltage: DQ	V_{IH}	0.8 x V_{DDQ}	-	V_{DDQ} + 0.3	V	1
Input low (logic 0) voltage: DQ	V_{IL}	-0.3	-	0.2 x V_{DDQ}	V	1
Clock input crossing point voltage: CK and /CK	V_{IX}	0.4 x V_{DDQ}	-	0.6 x V_{DDQ}	V	2

Note :
1. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
2. The value of V_{IX} is expected to equal 0.5 x V_{DDQ} of the transmitting device and must track variation in the DC level of the same.

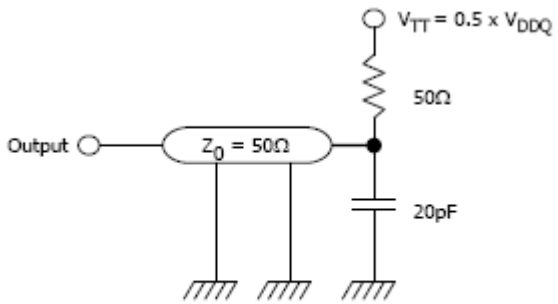
AC OPERATING TEST CONDITIONS

(VDD = 1.70V to 1.95V, TA = -25°C to +85°C)

Parameter	Symbol	Value	Unit
AC input high / low level voltage	V_{IH} / V_{IL}	0.8 x V_{DDQ} / 0.2 x V_{DDQ}	V
Input timing measurement reference level voltage	V_{TRIP}	0.5 x V_{DDQ}	V
Input rise / fall time	t_R / t_F	1 / 1	ns
Output timing measurement reference level voltage	V_{OUTREF}	0.5 x V_{DDQ}	V
Output load capacitance for access time measurement		See F2	



F1. DC Output Load Circuit



F2. AC Output Load Circuit

CAPACITANCE (VDD = 1.8V, VDDQ = 1.8V, TA = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (CK, /CK)	C_{CK}	1.5	3.5	pF
Input capacitance delta (CK, /CK)	C_{DCK}		0.25	pF
Input capacitance (all other input-only pins)	C_I	1.5	3.0	pF
Input capacitance delta (all other input-only pins)	C_{DI}		0.5	pF
Input / output capacitance (DQ, DQS, DM)	C_{IO}	2.0	4.5	pF
Input / output capacitance delta (DQ, DQS, DM)	C_{DIO}		0.5	pF

Notes : 1. These values are guaranteed by design and are tested on a sample basis only.
2. These capacitance values are for single monolithic devices only. Multiple die packages will have parallel capacitive loads.
3. Input capacitance is measured with V_{SS}, V_{SSQ}, V_{DD}, and V_{DDQ} applied and all other pins (except the pin under test) floating. DQ's should be in a high impedance state. This may be achieved by pulling CKE to low level.
4. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS, and DM in the system.

AC CHARACTERISTICS

Parameter		Symbol	-60 (DDR333)		-75 (DDR266)		Unit	Note
			Min	Max	Min	Max		
CK cycle time	CL = 3	t_{CK}	6.0	100	7.5	100	ns	1
CK High level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
CK Low level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
DQS out access time from CK		t_{DQSCK}	2.0	5.0	2.0	5.5	ns	
Output access time from CK		t_{AC}	2.0	5.0	2.0	5.5	ns	3
Data strobe edge to Dout edge		t_{DQSQ}	-	0.5	-	0.6	ns	
Read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	
Read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}	
CK to valid DQS-In		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	
DQS-In setup time		t_{WPRES}	0	-	0	-	ns	4
DQS-In hold time		t_{WPREH}	0.25	-	0.25	-	t_{CK}	
DQS write postamble time		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}	
DQS-In High level width		t_{DQSH}	0.35	-	0.35	-	t_{CK}	
DQS-In Low level width		t_{DQSL}	0.35	-	0.35	-	t_{CK}	
Address and Control Input setup time		t_{IS}	1.1	-	1.3	-	ns	1
Address and Control Input hold time		t_{IH}	1.1	-	1.3	-	ns	1
DQ and DM setup time to DQS		t_{DS}	0.6	-	0.8	-	ns	5, 6
DQ and DM hold time to DQS		t_{DH}	0.6	-	0.8	-	ns	5, 6
Clock half period		t_{HP}	t_{CL} (min) or t_{CH} (min)	-	t_{CL} (min) or t_{CH} (min)	-	ns	
Data hold time from DQS to earliest DQ edge		t_{QH}	t_{HP} -0.65	-	t_{HP} -0.75	-	ns	
Row cycle time		t_{RC}	60	-	67.5	-	ns	
Auto Refresh cycle time		t_{RFC}	108	-	110	-	ns	
Row Active time		t_{RAS}	42	120000	45	120000	ns	
/RAS to /CAS delay for Read or Write		t_{RCD}	22.5	-	22.5	-	ns	
Row precharge time		t_{RP}	18	-	22.5	-	ns	
Row Active to Row Active delay		t_{RRD}	12	-	15	-	ns	
Write recovery time		t_{WR}	15	-	15	-	ns	9
Last Din (Data Input) to Active delay		t_{DAL}	Note 2	-	Note 2	-	t_{CK}	2
Internal Write to Read command delay		t_{WTR}	2	-	1	-	t_{CK}	8
Col. address to col. Address delay		t_{CCD}	1	-	1	-	t_{CK}	
Mode register set cycle time		t_{MRD}	2	-	2	-	t_{CK}	
Exit Self Refresh to next valid command		t_{XSR}	120	-	120	-	ns	
Exit Power Down mode to first valid command		t_{XP}	25	-	25	-	ns	7
Refresh Interval time		t_{REF}	64	-	64	-	ms	10

Note :

1. Input Setup / Hold Slew Rate Derating

Input Setup / Hold Slew Rate (V/ns)	Δt_{IS} (ps)	Δt_{IH} (ps)
1.0	0	0
0.8	+ 50	+ 50
0.6	+ 100	+ 100

This derating table is used to increase t_{IS} / t_{IH} in the case where the input slew rate is below 1.0V/ns.

2. t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK}). For each of these terms, if the ratio is not already an integer, round up to the next integer.

3. Driver Strength should be selected based on actual system loading conditions. Figure 2, the AC Output Load Circuit, represents the reference load used in defining the relevant timing parameters of this device. The 20pF load capacitance is not expected to be a precise representation of either a typical system load or the production test environment but is appropriate for Full Driver Strength. Setting the output drivers to 1/2 Driver Strength, for a further example, is appropriate for a 10pF load.

4. The specific requirement is that DQS be Valid (High or Low) on or before this CK edge. The case shown (DQS going from High-Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS}.

5. I/O Setup / Hold Slew Rate Derating

I/O Setup / Hold Slew Rate (V/ns)	Δt_{DS} (ps)	Δt_{DH} (ps)
1.0	0	0
0.8	+ 75	+ 75
0.6	+ 150	+ 150

This derating table is used to increase t_{DS} / t_{DH} in the case where the I/O slew rate is below 1.0V/ns.

6. I/O Delta Rise/Fall Rate (1/slew rate) Derating

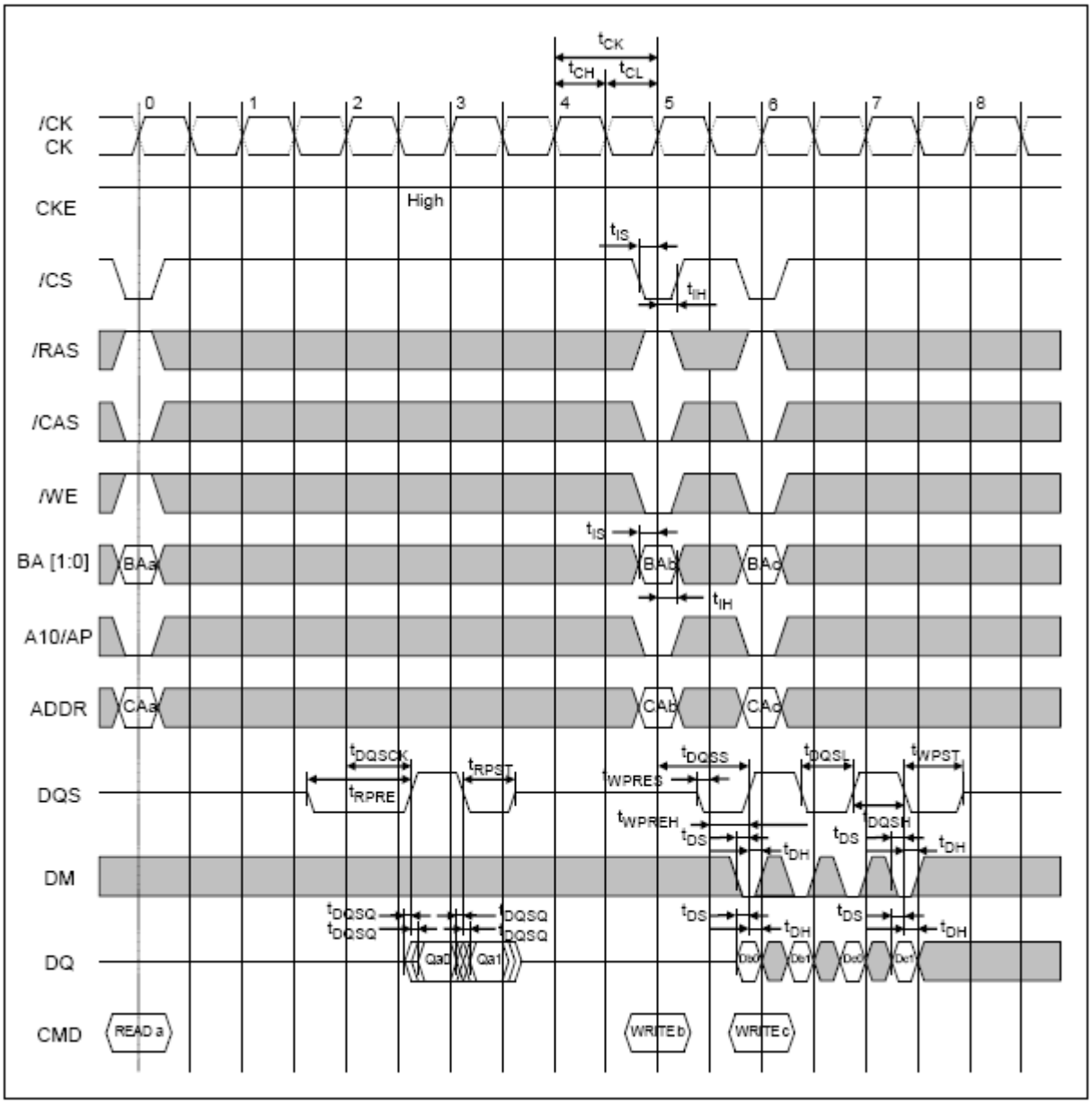
I/O Delta Rise / Fall Rate (ns/V)	Δt_{DS} (ps)	Δt_{DH} (ps)
1.0	0	0
± 0.25	+ 50	+ 50
± 0.50	+ 100	+ 100

This derating table is used to increase t_{DS} / t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise / Fall Rate is calculated as 1/SlewRate1 - 1/SlewRate2. For example, if SlewRate1 = 1.0V/ns and SlewRate2 = 0.8V/ns, then the Delta Rise / Fall Rate = -0.25ns/V.

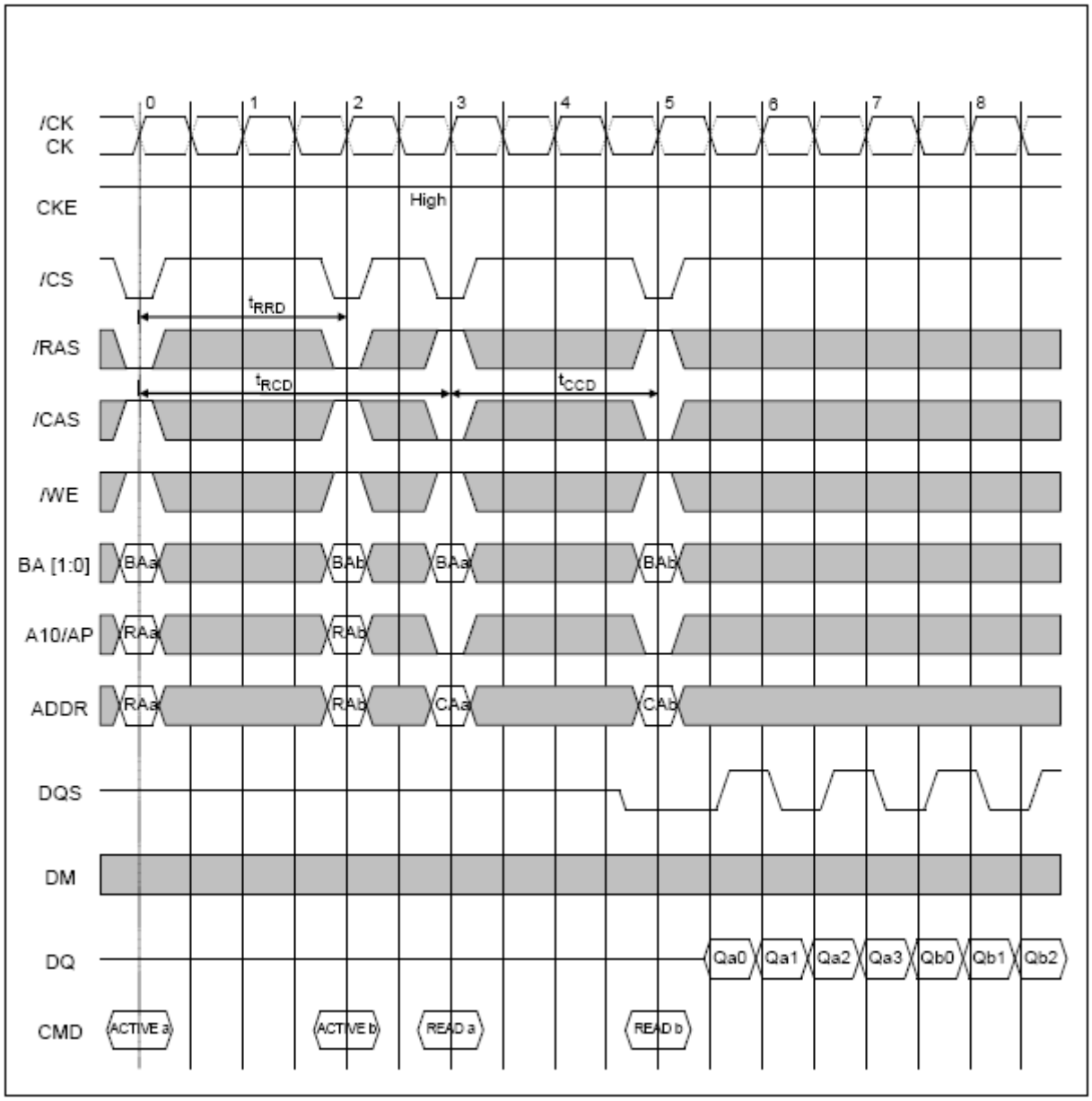
7. There must be at least one clock (CK) pulse during the t_{XP} period.
8. t_{WTR} is referenced from the positive clock edge after the last Data In pair.
9. t_{WR} is referenced from the positive clock edge after the last desired Data In pair.
10. Each of the 8192 row locations in each of the four banks must be activated or refreshed in any rolling 64ms period. If Auto Refresh cycles to all four banks simultaneously are used for this purpose, the average refresh interval for distributed refresh is 64ms ÷ 8192 = 7.8125us.

Timing

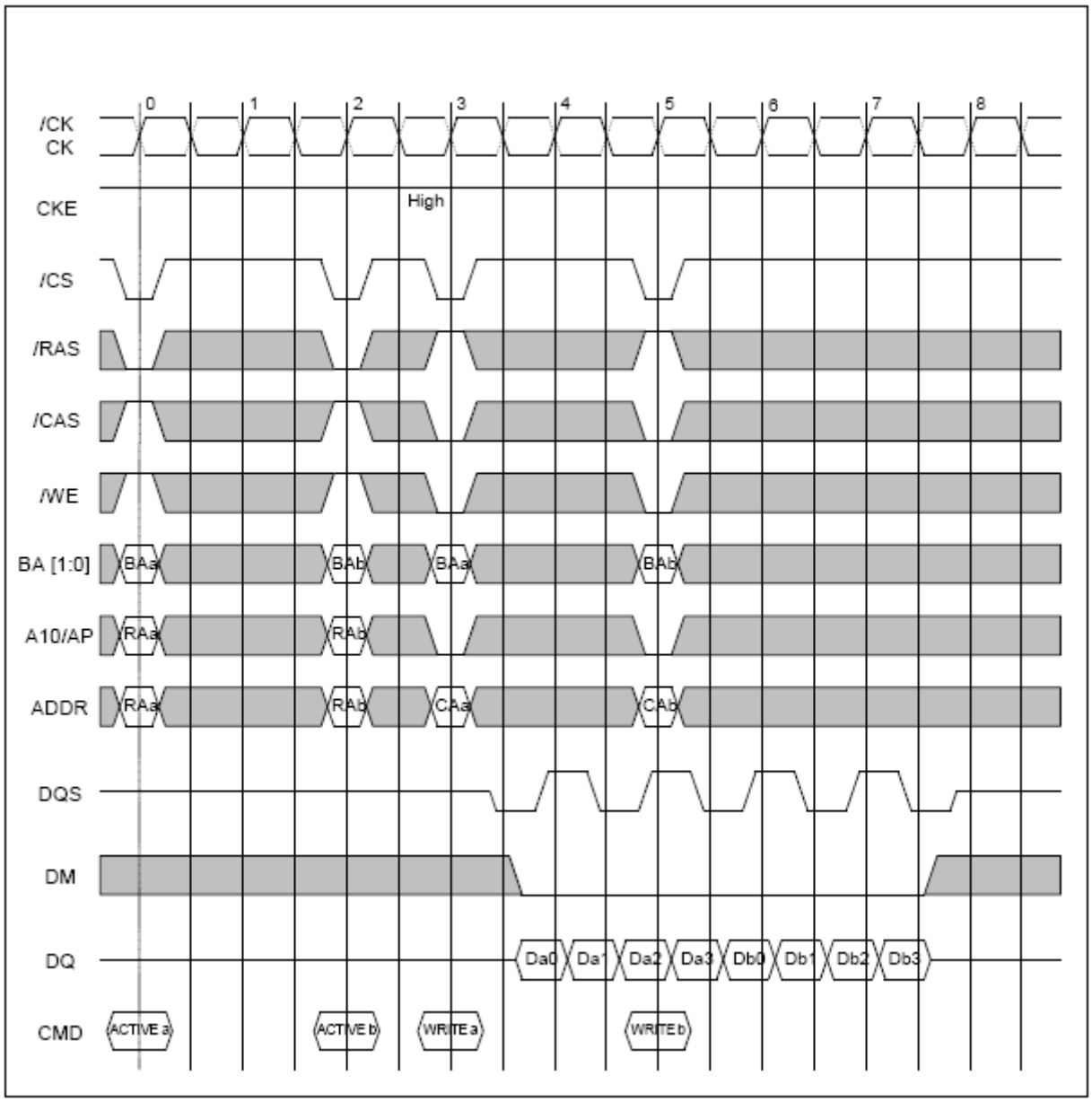
Basic Timing (Setup, Hold and Access Time @BL = 2, CL = 3)



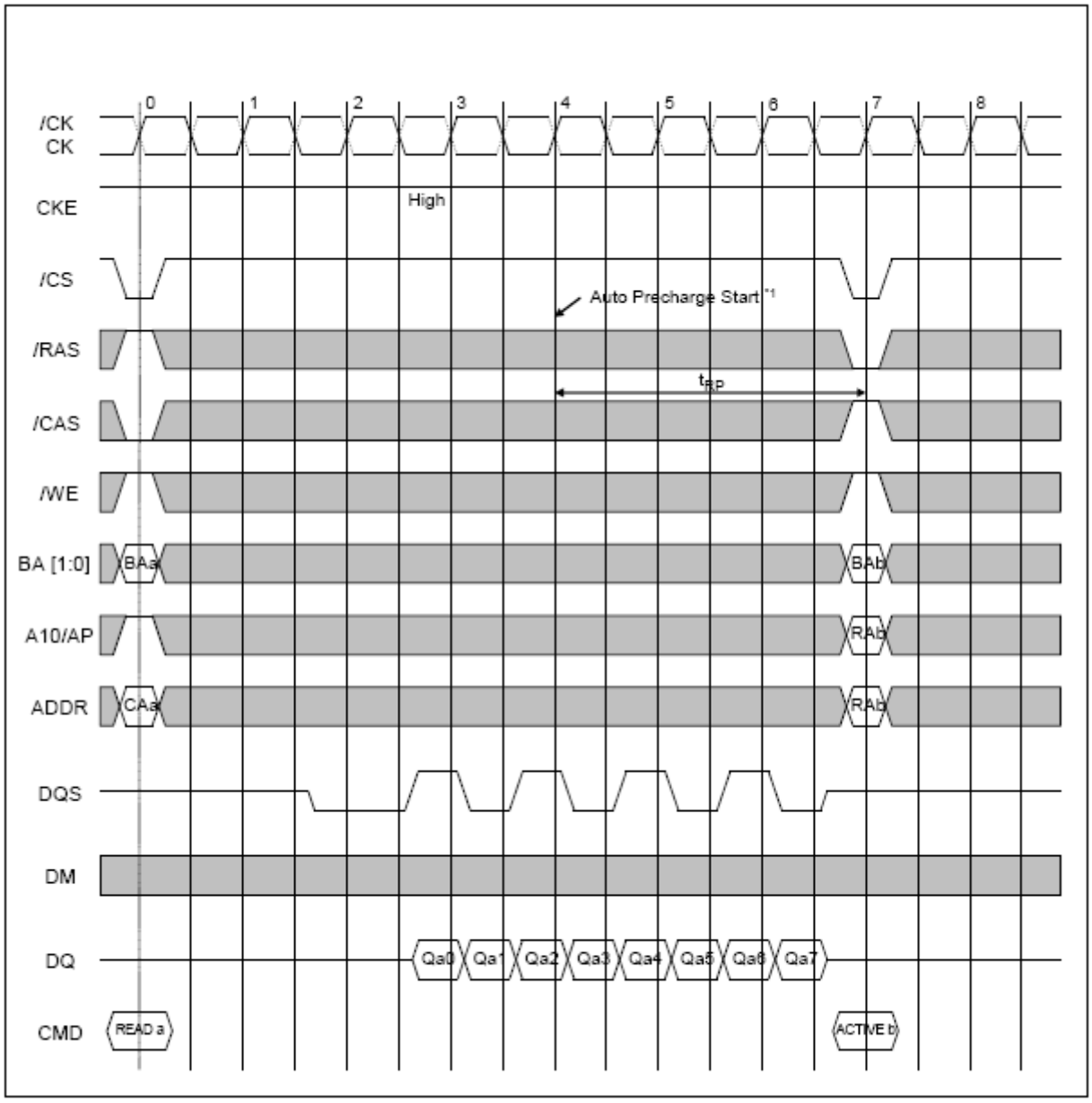
Multi Bank Interleaving READ (@BL = 4, CL = 3)



Multi Bank Interleaving Write (@BL = 4)

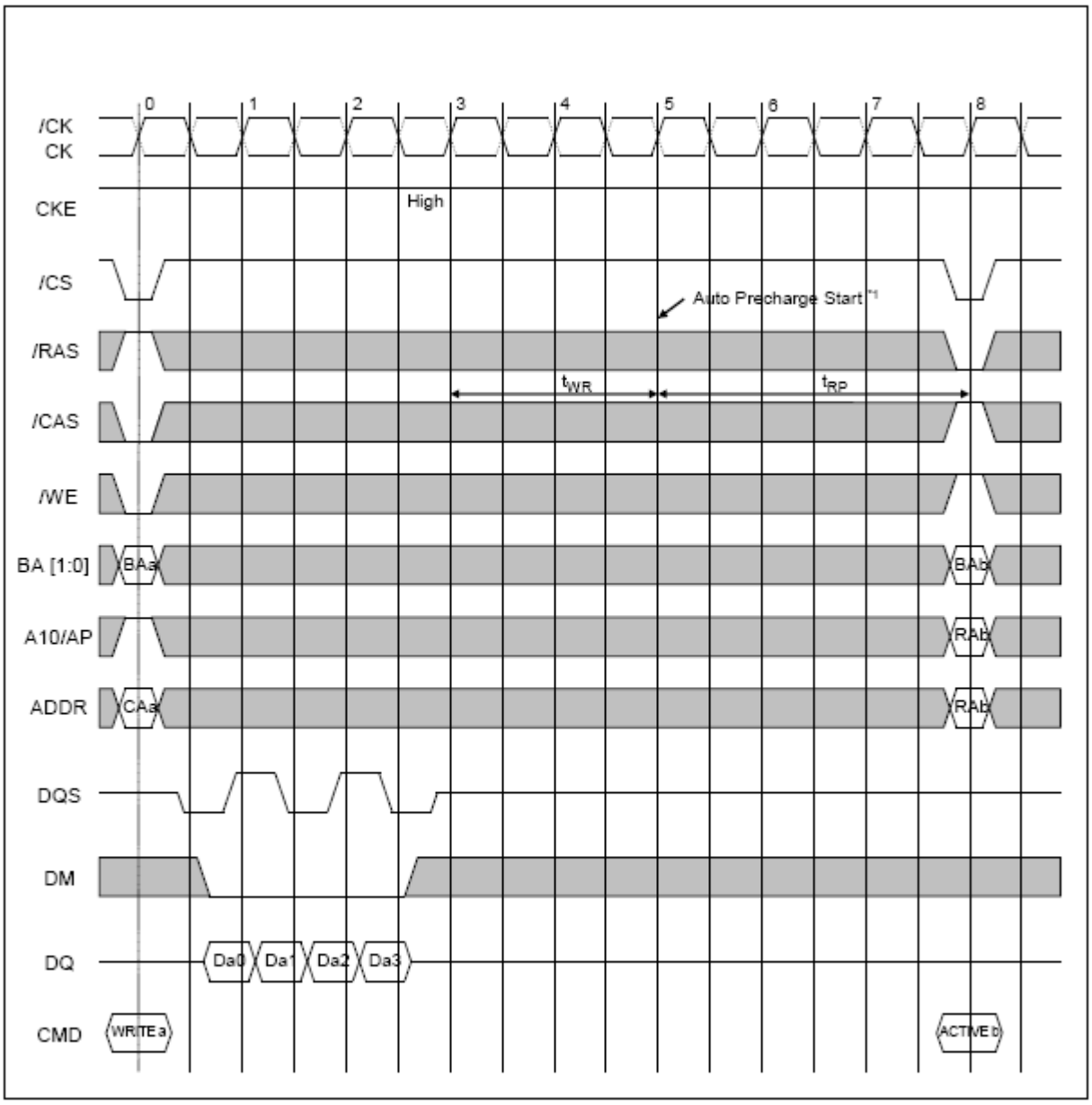


Read with Auto Precharge (@BL = 8, CL = 3)



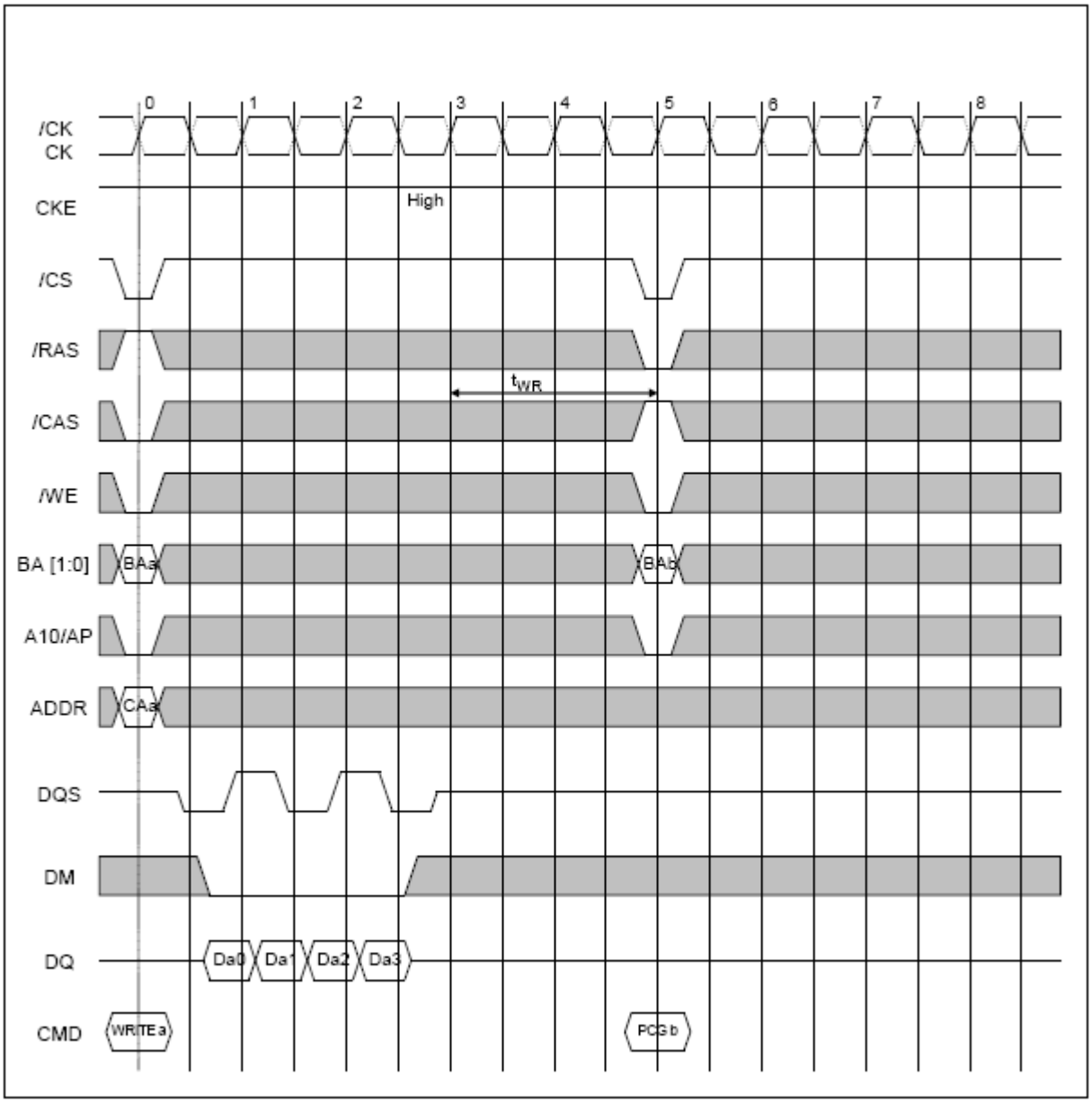
*1 The Active command of the precharged bank can be issued after t_{RP} from this point.

Write with Auto Precharge (@BL = 4)



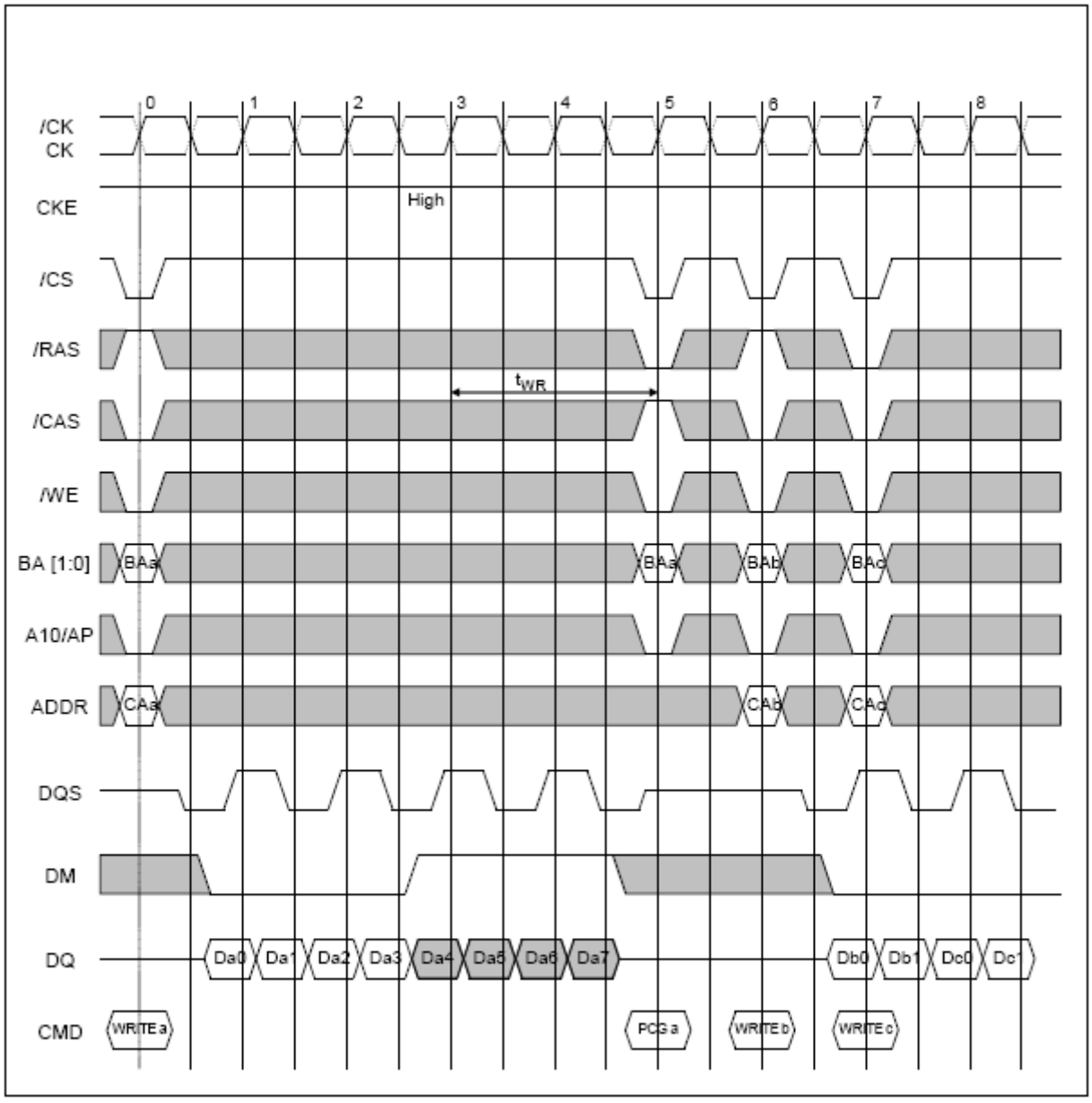
*1 The Active command of the precharged bank can be issued after t_{RP} from this point.

Write Followed by Precharge (@BL = 4)



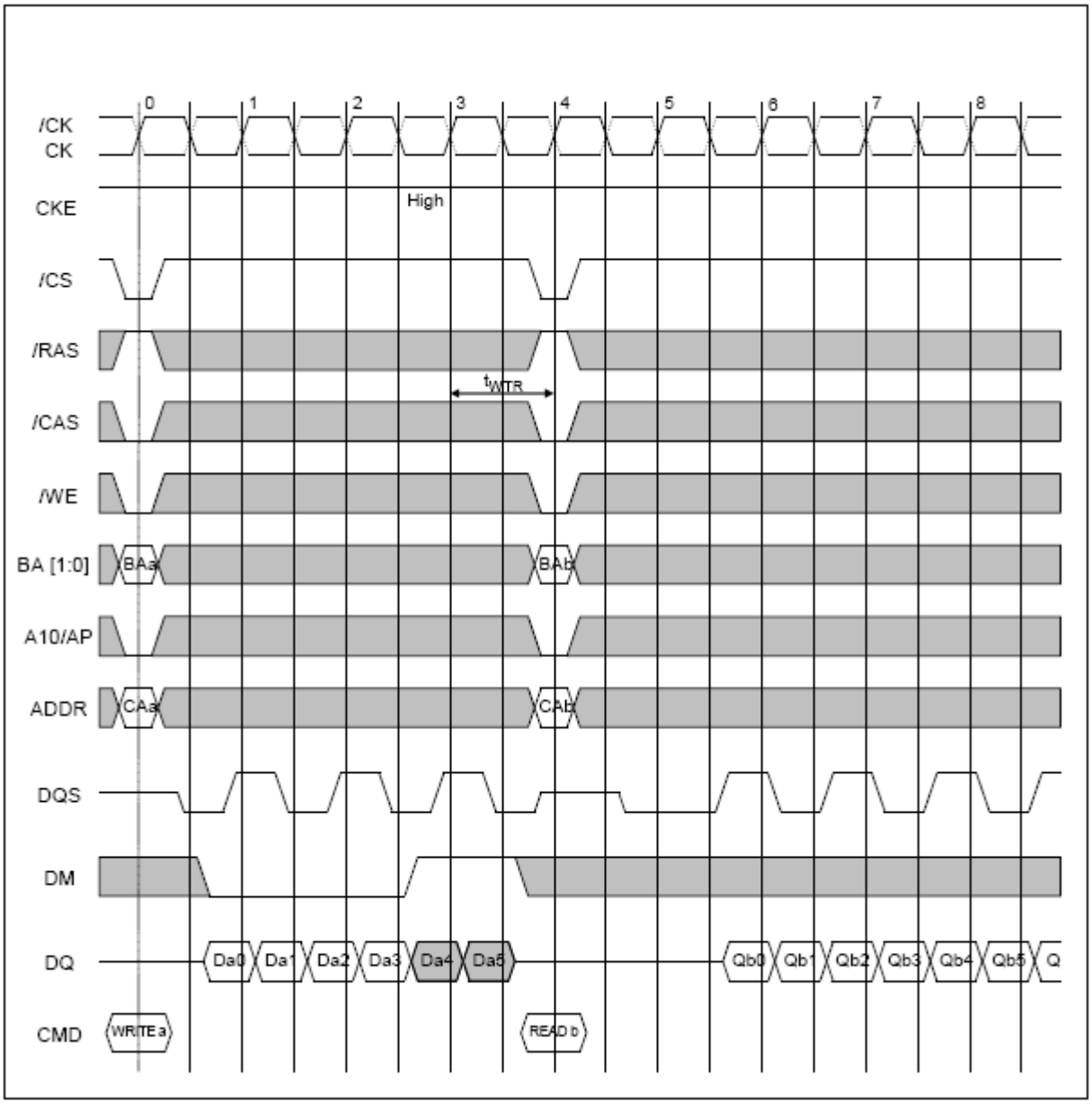
Note: PCG = Precharge.

Write Interrupted by Precharge & DM (@BL = 8)

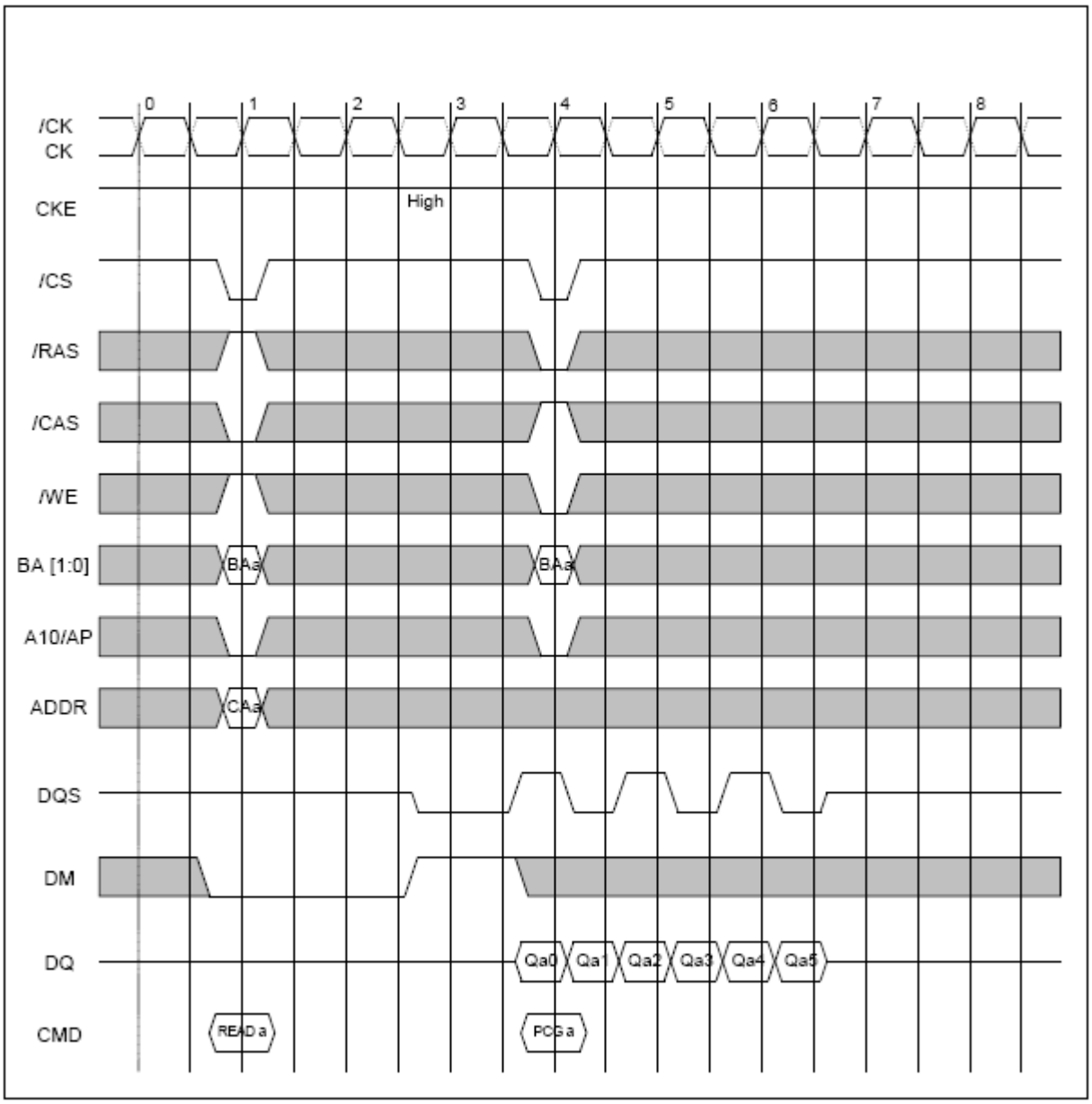


Note: PCG = Precharge.

Write Interrupted by Read (@BL = 8)

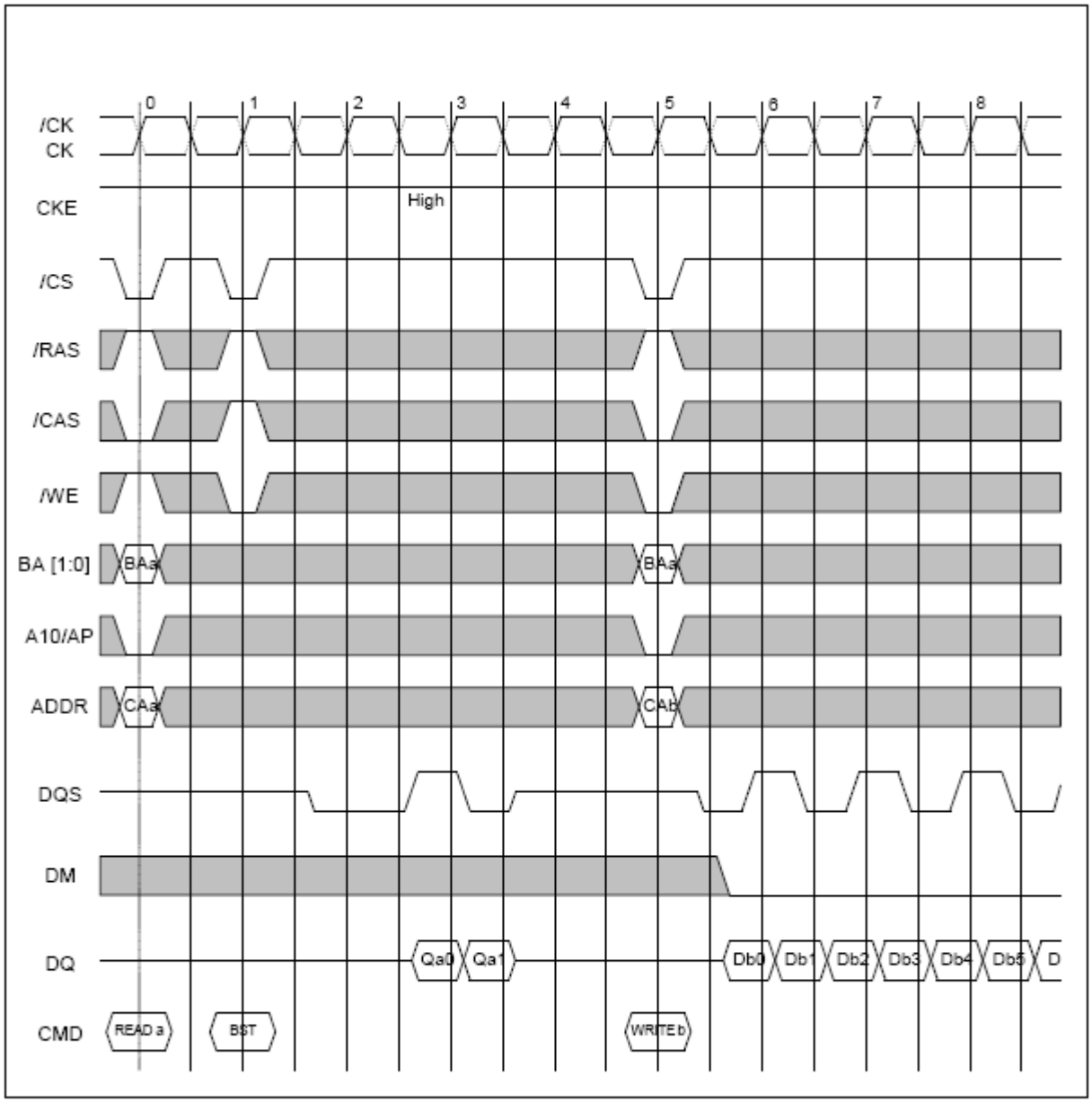


Read Interrupted by Precharge (@BL = 8, CL = 3)



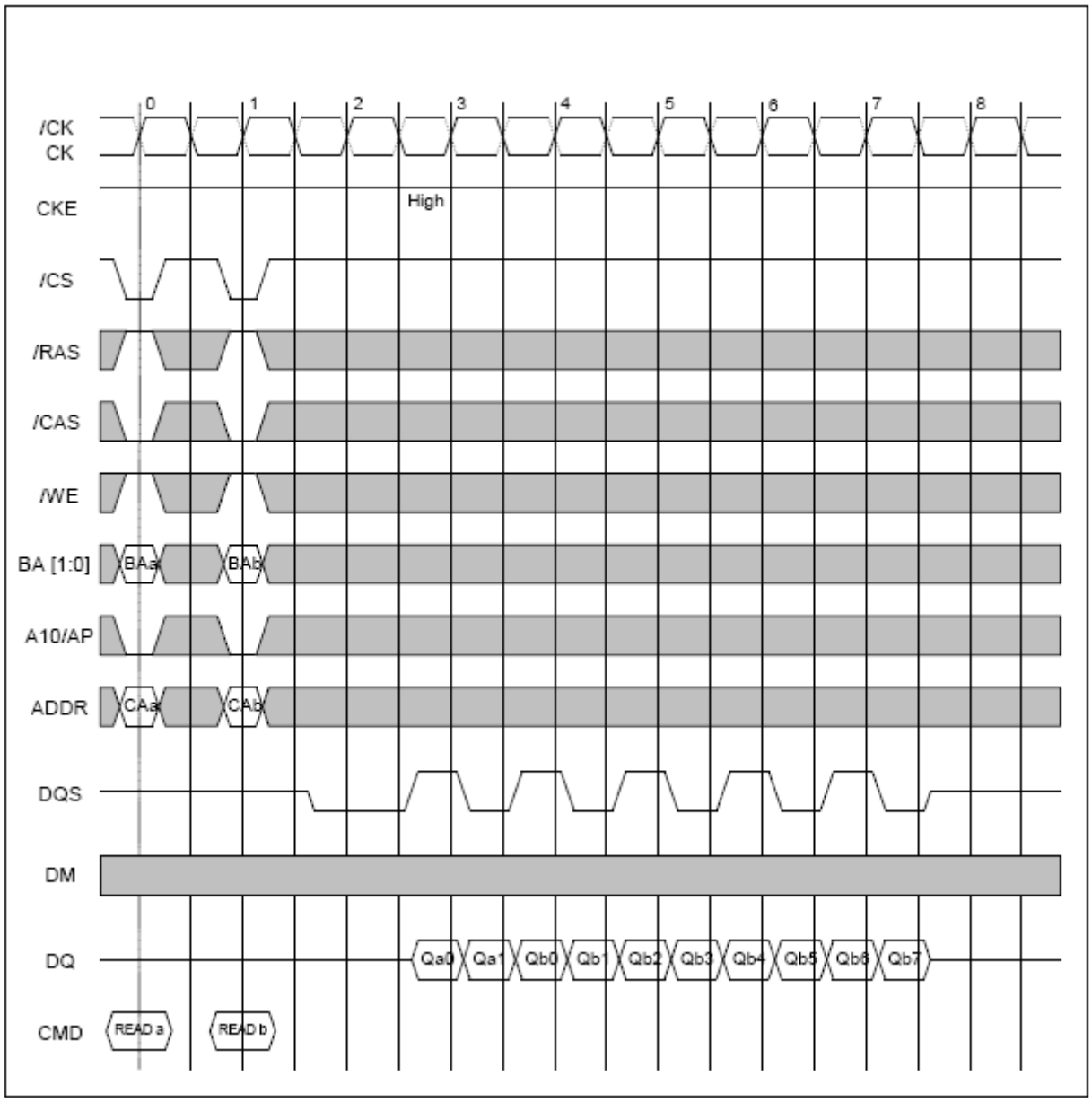
Note: PCG = Precharge.

Read Interrupted by Burst stop & Write (@BL = 8, CL = 3)

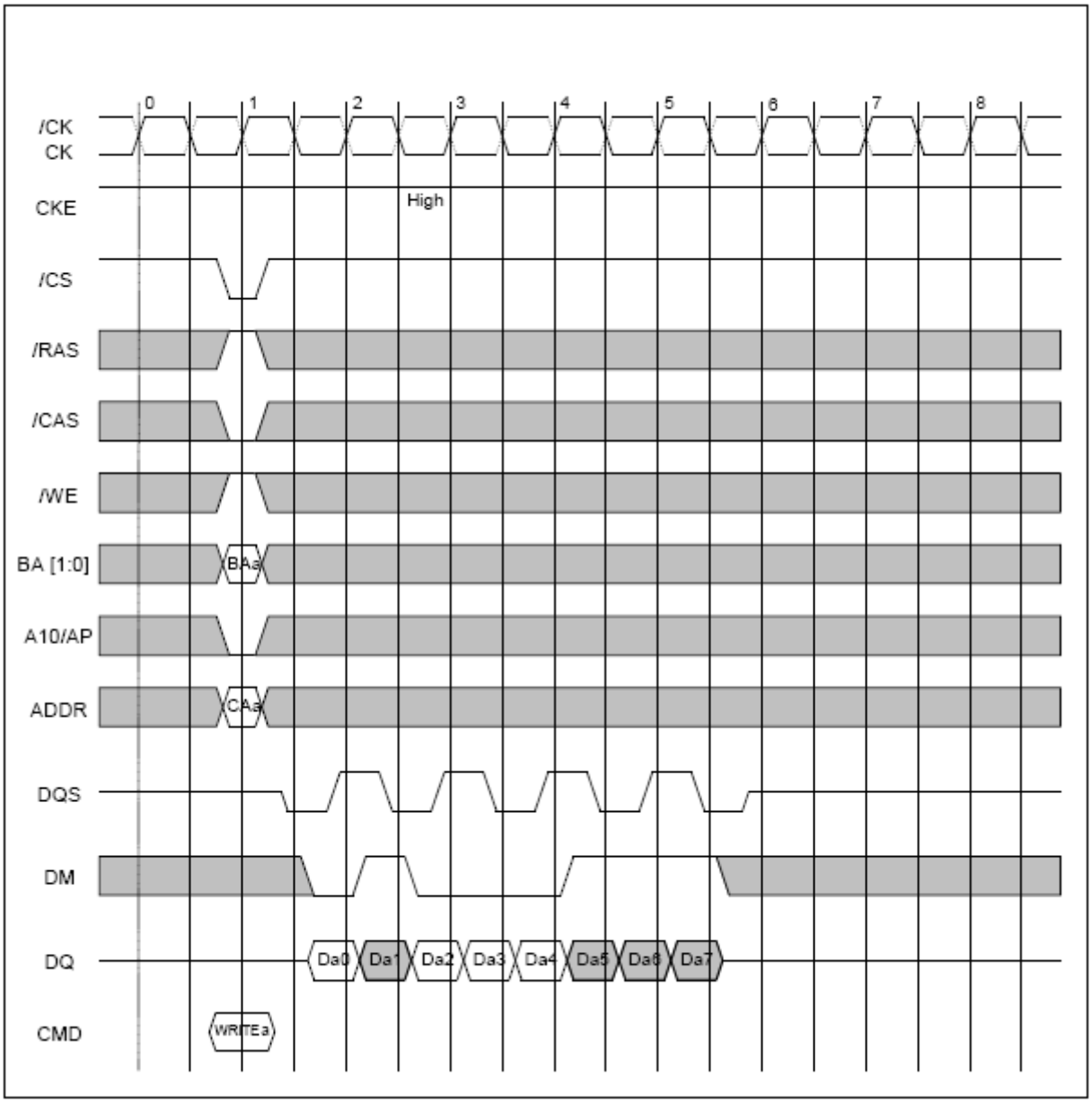


Note: BST = Burst Stop.

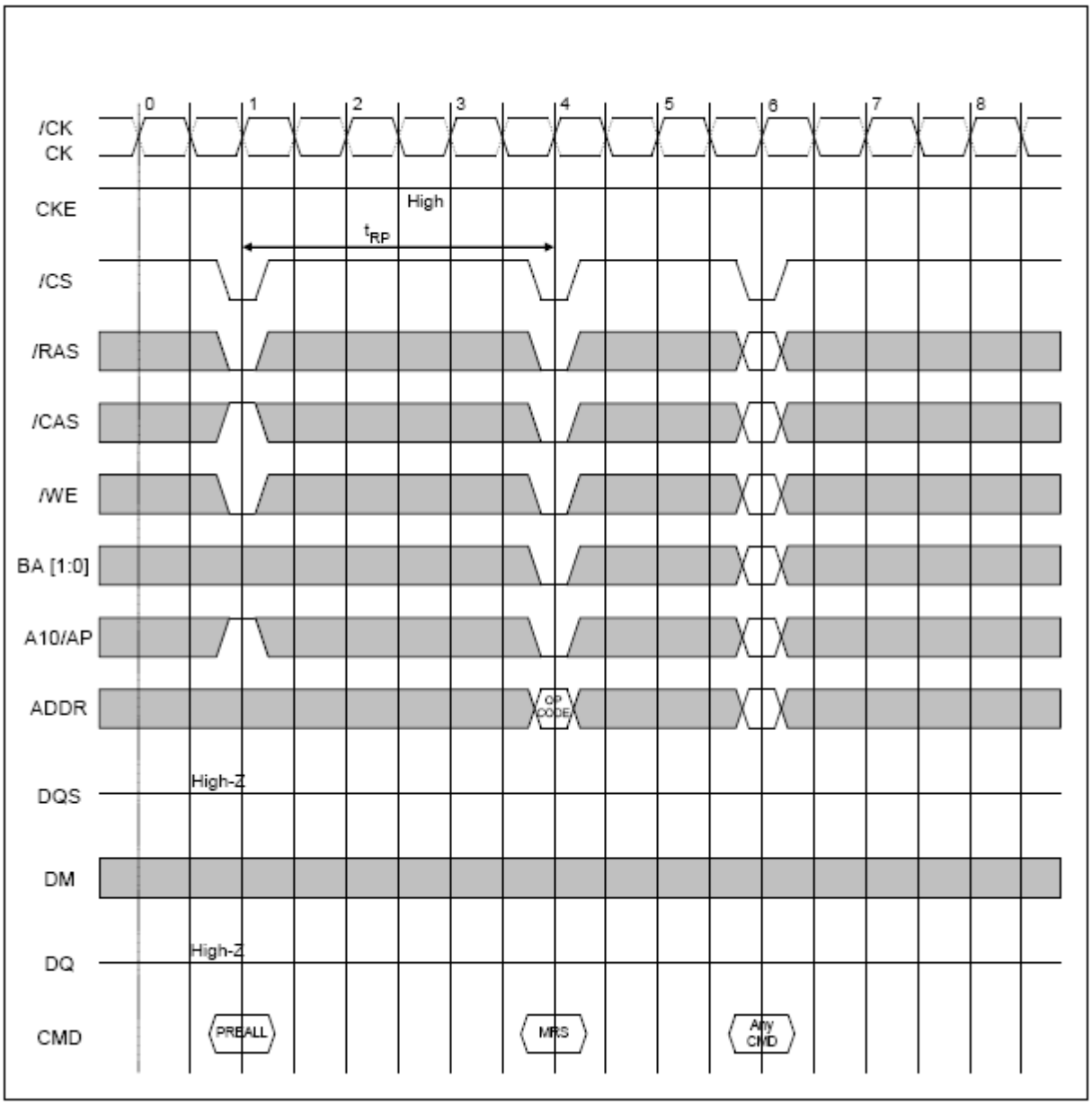
Read Interrupted by Read (@BL = 8, CL = 3)



DM Function for Write (@BL = 8)



Mode Register Set



SPECIAL OPERATIONS FOR LOW POWER CONSUMPTION

TEMPERATURE COMPENSATED SELF REFRESH

In order to reduce power consumption, a Mobile DDR SDRAM includes the internal temperature sensor and other circuitry to control Self Refresh operation automatically according to two temperature ranges: max. 40°C and max. 85°C.

Temperature Range	Self Refresh Current (I_{DD6})			
	Full Array	1/2 Full Array	1/4 Full Array	Unit
Max. 85°C	500	400	300	uA
Max. 40°C	250	220	200	uA

PARTIAL ARRAY SELF REFRESH

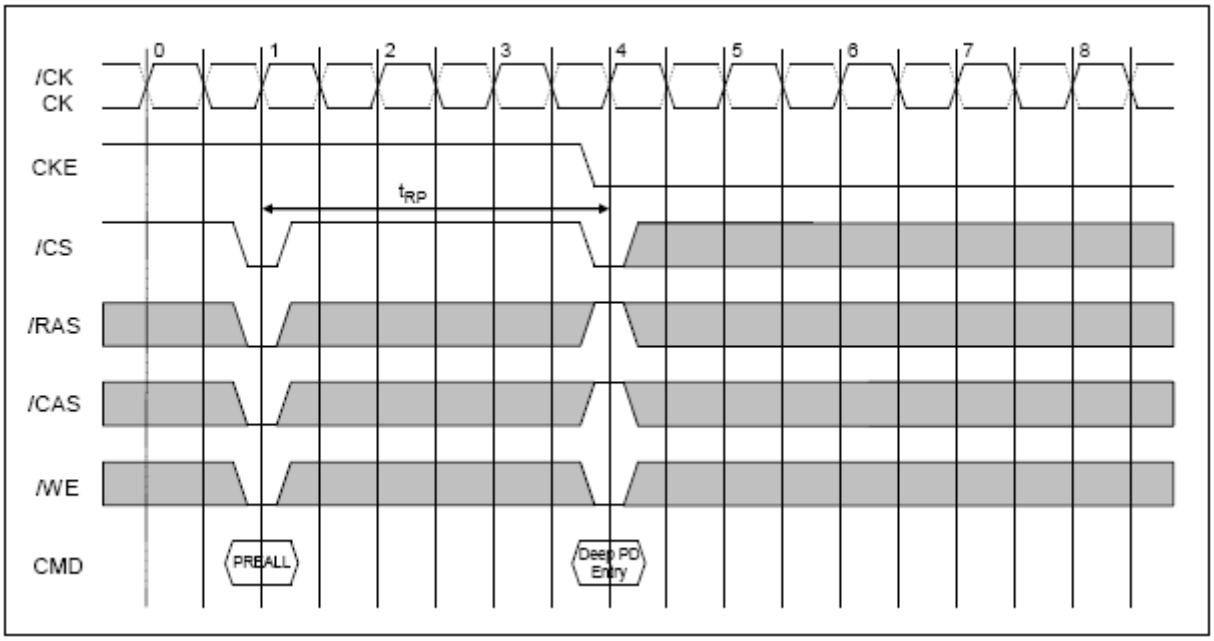
For further power savings during Self Refresh, the PASR feature allows the controller to select the amount of memory that will be refreshed during Self Refresh. The refresh options are all banks (banks 0, 1, 2 and 3); two banks (bank 0 and 1); one bank (bank 0); one-half of one bank (bank 0 with MSB address = 0); and one-quarter of one bank (bank 0 with MSB and MSB - 1 addresses = 0). Write and Read commands can still affect any bank during standard operations, but only the selected banks will be refreshed during Self Refresh. Data in unselected banks will be lost.

DEEP POWER DOWN

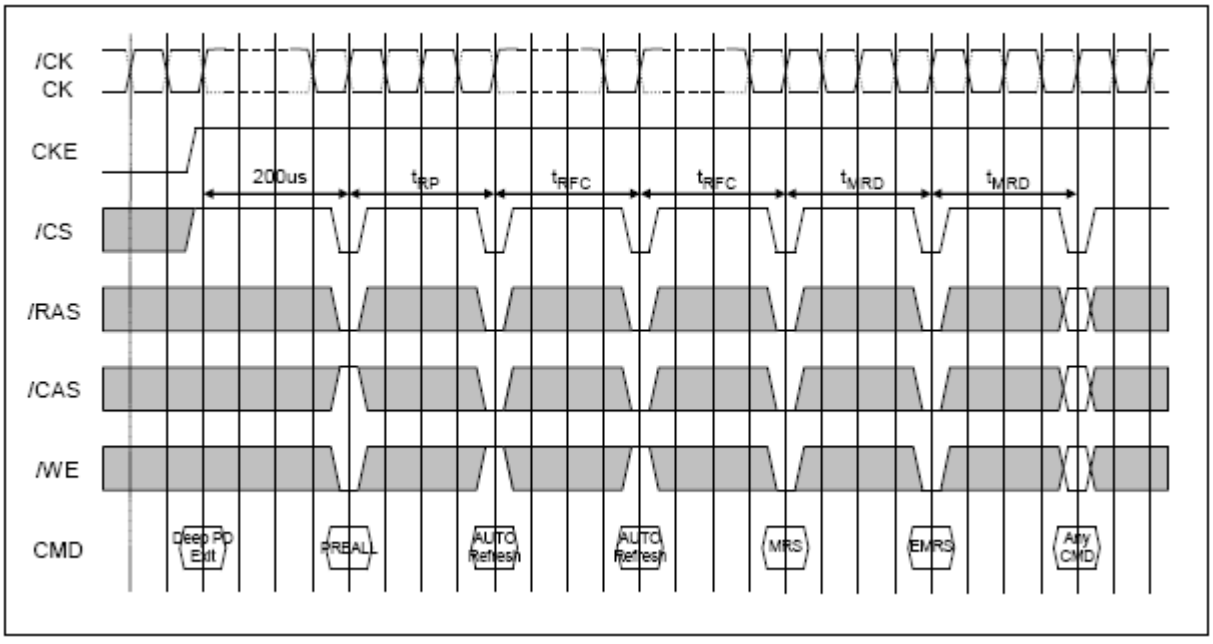
Deep Power Down achieves maximum power reduction by eliminating the power of the whole memory array and surrounding circuitry. Data will not be retained in the memory storage array, the Mode Register, or the Extended Mode Register once the device enters Deep Power Down mode.

This mode is entered by having all banks idle then /CS and /WE held Low with /RAS and /CAS held High at the rising edge of the clock, while CKE is Low. This mode is exited by asserting CKE High, applying only NOP commands for 200 microseconds, and then continuing with steps 4 through 11 of the Power Up and Initialization sequence..

Deep Power Down Mode Entry Timing

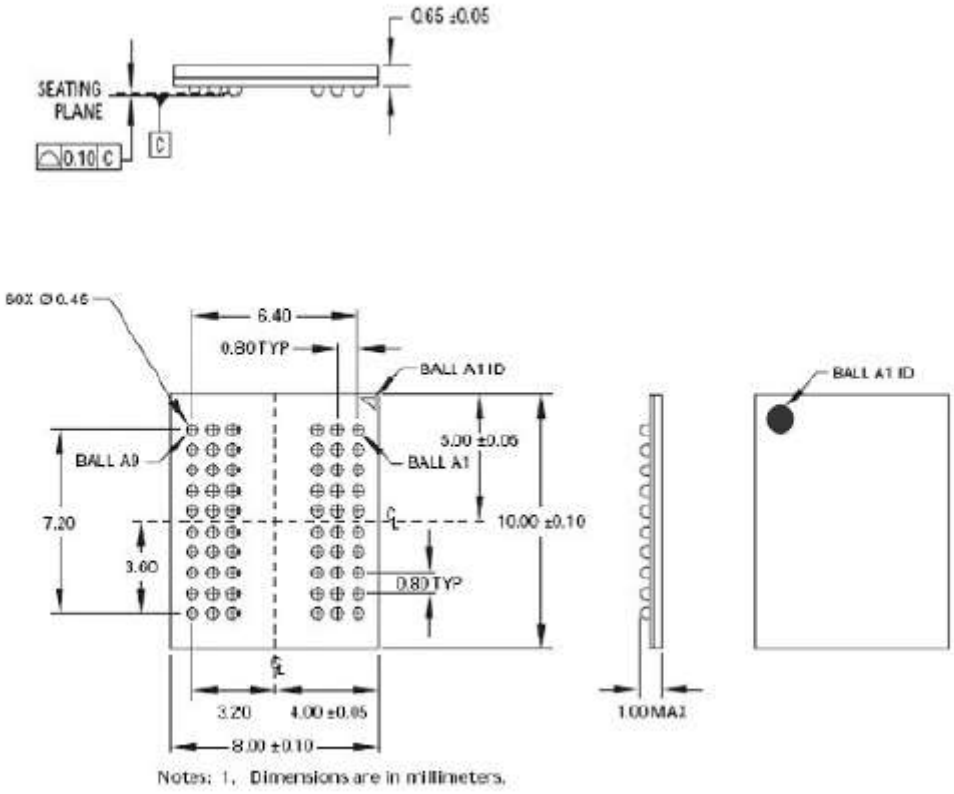


Deep Power Down Mode Exit Timing



PACKAGE DIMENSIONS

60-Ball FpBGA Package



Notes: 1. Dimensions are in millimeters.

Revision history

Revision No.	Revised Item	Issued Date
0.1	Initial Release	08 Nov. '11
0.2	DC Parameter	12 Jan. '12