Document Title

256K x 8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Date	Remark
0.0	-. Initial Draft	Jun. 28 2007	Preliminary
0.1	-. Revised VOH(2.2v to 2.4v),tOH(15ns to 10ns), tOE-55(30ns to 25ns), tWP-55(45ns to 40ns), tWP-70(55ns to 50ns), tWHZ-70(25ns to 20ns), ICC(2mA to 3mA), ICC1(2mA to 3mA)	Jul. 2 2007	
0.2	-. V_{IH} level change from 2.0V to 2.2V	Aug. 16 2007	
0.3	-. Fix typo error	Nov. 13 2007	
1.0	-. EM620FV8B(KGD),EM620FV8BS series & EM620FV8BT series are unified to EM620FV8Bx-xxLF. -. Memory Function Guide updated in the last page.	Apr. 7 2009	Release
1.1	-. Package type corrected in page 2.	Jan. 29 2010	
1.2	-. tDW updated to 40ns	Mar. 2 2010	
1.3	-. Change sTSOP32 Package	Dec. 18 2012	

Emerging Memory & Logic Solutions Inc.
2F Jeju CCI B/D, 574-1 Donam-Dong, Jeju-Si, Jeju-Do, Rep.of Korea Zip Code : 690-029
Tel : +82-64-740-1700 Fax : +82-64-740-1750 / Homepage : www.emlsi.com

EM620FV8B Family
Low Power, 256Kx8 SRAM

FEATURES

- Process Technology : 0.15μm Full CMOS
- Organization : 256K x 8 bit
- Power Supply Voltage : 2.7V ~ 3.6V
- Low Data Retention Voltage : 1.5V(Min.)
- Three state output and TTL Compatible
- Package Type : 32-sTSOP1, 32-TSOP1

GENERAL DESCRIPTION

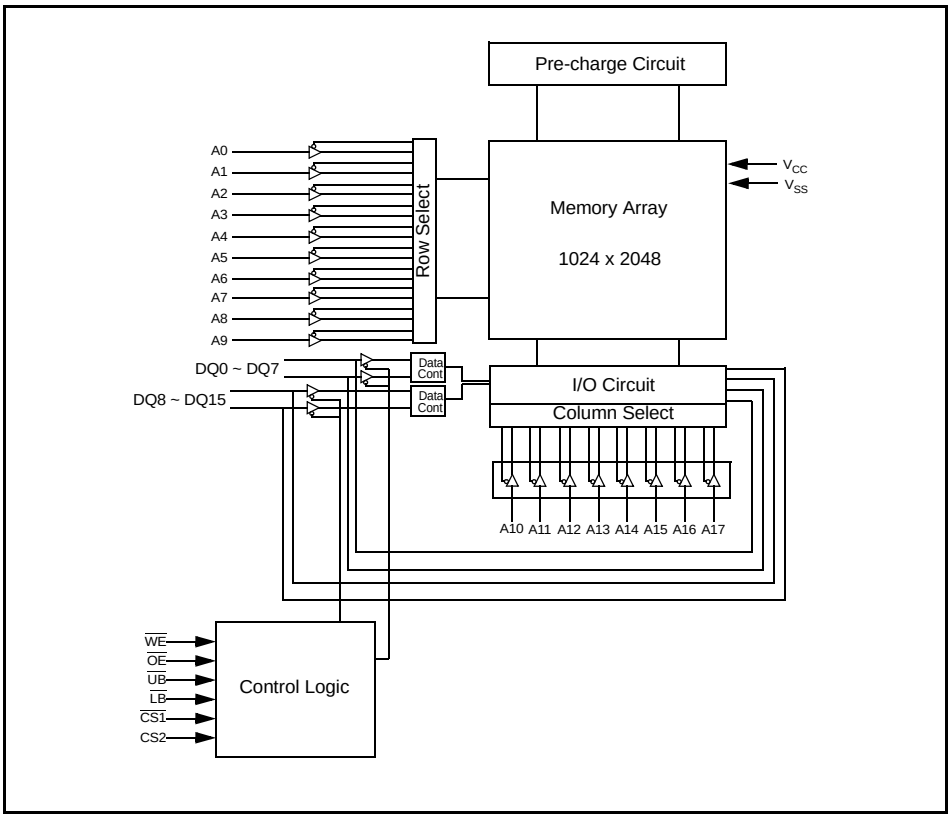
The EM620FV8B families are fabricated by EMLSI's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Typ.)	Operating (I_{CC1}.Max.)	
EM620FV8B	Industrial (-40 ~ 85°C)	2.7 ~ 3.6 V	45/55/70 ns	1 μA[2]	3 mA	KGD
EM620FV8BS - xx[1]LF						32-sTSOP1
EM620FV8BT - xx[1]LF						32-TSOP1

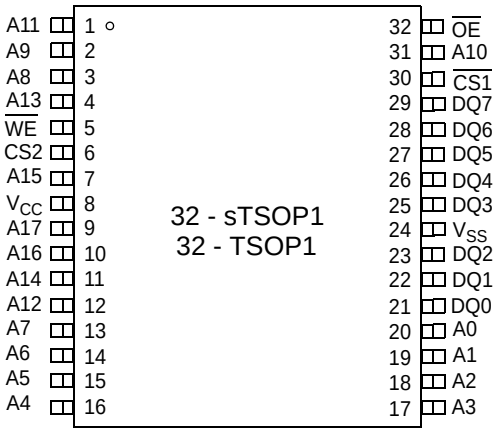
1. "xx" represents speed.
2. Typical values are measured at Vcc=3.3V, T_A=25°C and not 100% tested.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

32 - sTSOP1, 32 - TSOP1 : Top view



PIN DESCRIPTION

Name	Function	Name	Function
$\overline{CS1}$, CS2	Chip Select inputs	V_{CC}	Power Supply
$\overline{OE}$	Output Enable input	V_{SS}	Ground
$\overline{WE}$	Write Enable input	NC	No Connection
A0~A17	Address inputs		
DQ0~DQ7	Data inputs/outputs		

ABSOLUTE MAXIMUM RATINGS[1)]

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.2 to 4.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	^oC

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	DQ0~7	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Word Read	Active
L	H	X	L	Data In	Word Write	Active

NOTE : X means don't care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS [1)]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	-	V_{CC} + 0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. TA= -40 to 85°C, otherwise specified
2. Overshoot: VCC +2.0 V in case of pulse width ≤ 20ns
3. Undershoot: -2.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Ouput capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

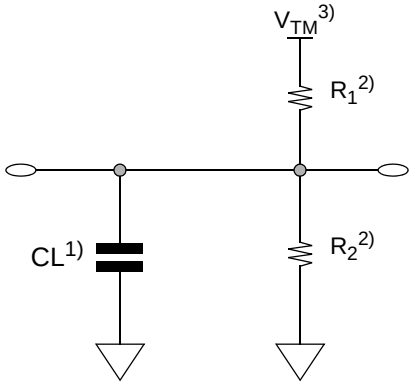
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	-	1	μA
Output leakage current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=V_{SS} to V_{CC}		-1	-	1	μA
Operating power supply	I_{CC}	I_{IO}=0mA, $\overline{CS1}$=V_{IL}, CS2=$\overline{WE}$=V_{IH}, V_{IN}=V_{IH} or V_{IL}		-	-	3	mA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS1}$≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	-	3	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, $\overline{CS1}$=V_{IL}, CS2=V_{IH}, V_{IN}=V_{IL} or V_{IH}	45ns	-	-	35	mA
			55ns	-	-	30	
			70ns	-	-	25	
Output low voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Standby Current (TTL)	I_{SB}	$\overline{CS1}$=V_{IH}, CS2=V_{IL}, Other inputs=V_{IH} or V_{IL}		-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS1}$≥V_{CC}-0.2V, CS2≥V_{CC}-0.2V ($\overline{CS1}$ controlled) or 0V≤CS2≤0.2V (CS2 controlled), Other inputs = 0~V_{CC} (Typ. condition : V_{CC}=3.3V @ 25°C) (Max. condition : V_{CC}=3.6V @ 85°C)	LF	-	1 [1)]	10	μA

1. Typical values are measured at Vcc=3.3V, T_A=25°C and not 100% tested.

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)
Input Pulse Level : 0.4 to 2.2V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : 1.5V
Output Load (See right) : $CL^{1)}$ = 100pF+ 1 TTL(70nsec)
$CL^{1)}$ = 30pF + 1 TTL(45ns/55ns)

1. Including scope and Jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM}=2.8V
4. CL = 5pF + 1 TTL (measurement with t_{LZ}, t_{HZ}, t_{OLZ}, t_{OHZ}, t_{WHZ})



READ CYCLE (V_{cc} =2.7 to 3.6V, Gnd = 0V, T_A = -40°C to +85°C)

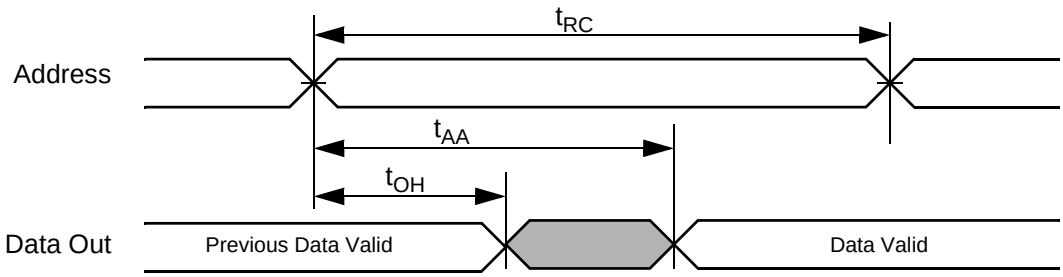
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	45	-	55	-	70	-	ns
Address access time	t_{AA}	-	45	-	55	-	70	ns
Chip select to output	t_{CO1},t_{CO2}	-	45	-	55	-	70	ns
Output enable to valid output	t_{OE}	-	25	-	25	-	35	ns
Chip select to low-Z output	t_{LZ1},t_{LZ2}	10	-	10	-	10	-	ns
$\overline{UB}$, $\overline{LB}$ enable to low-Z output	t_{BLZ}	5	-	5	-	5	-	ns
Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	ns
Chip disable to high-Z output	t_{HZ1},t_{HZ2}	0	20	0	20	0	25	ns
Output disable to high-Z output	t_{OHZ}	0	15	0	20	0	25	ns
Output hold from address change	t_{OH}	10	-	10	-	10	-	ns

WRITE CYCLE (V_{cc} =2.7 to 3.6V, Gnd = 0V, T_A = -40°C to +85°C)

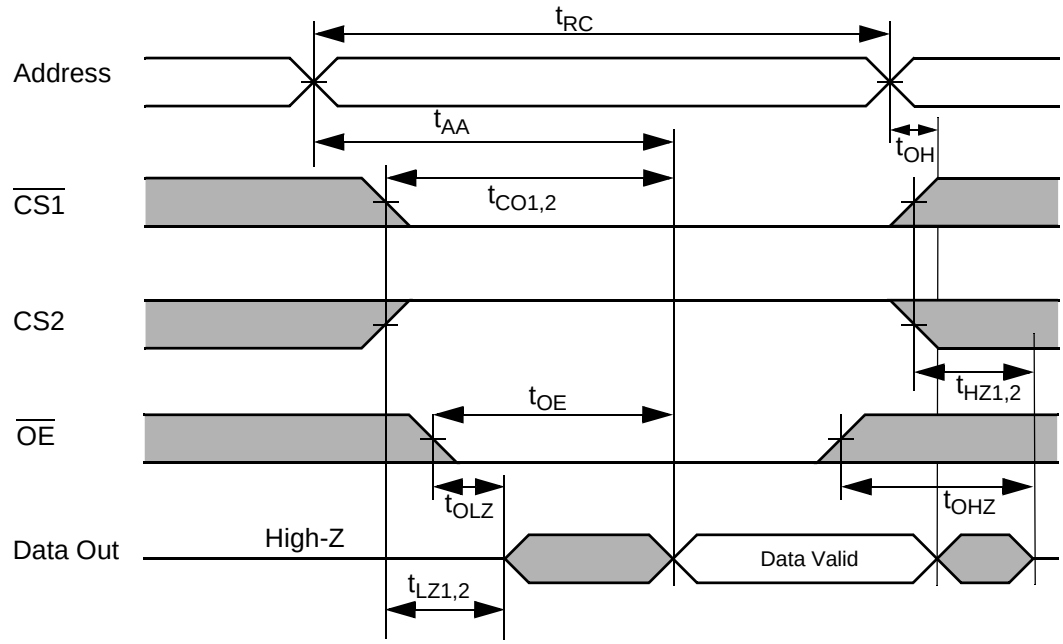
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	45	-	55	-	70	-	ns
Chip select to end of write	t_{CW1},t_{CW2}	45	-	45	-	60	-	ns
Address setup time	t_{AS}	0	-	0	-	0	-	ns
Address valid to end of write	t_{AW}	45	-	45	-	60	-	ns
$\overline{UB}$, $\overline{LB}$ valid to end of write	t_{BW}	45	-	45	-	60	-	ns
Write pulse width	t_{WP}	35	-	40	-	50	-	ns
Write recovery time	t_{WR}	0	-	0	-	0	-	ns
Write to ouput high-Z	t_{WHZ}	0	15	0	20	0	20	ns
Data to write time overlap	t_{DW}	40		40		40		ns
Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
End write to output low-Z	t_{OW}	5	-	5		5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IH})



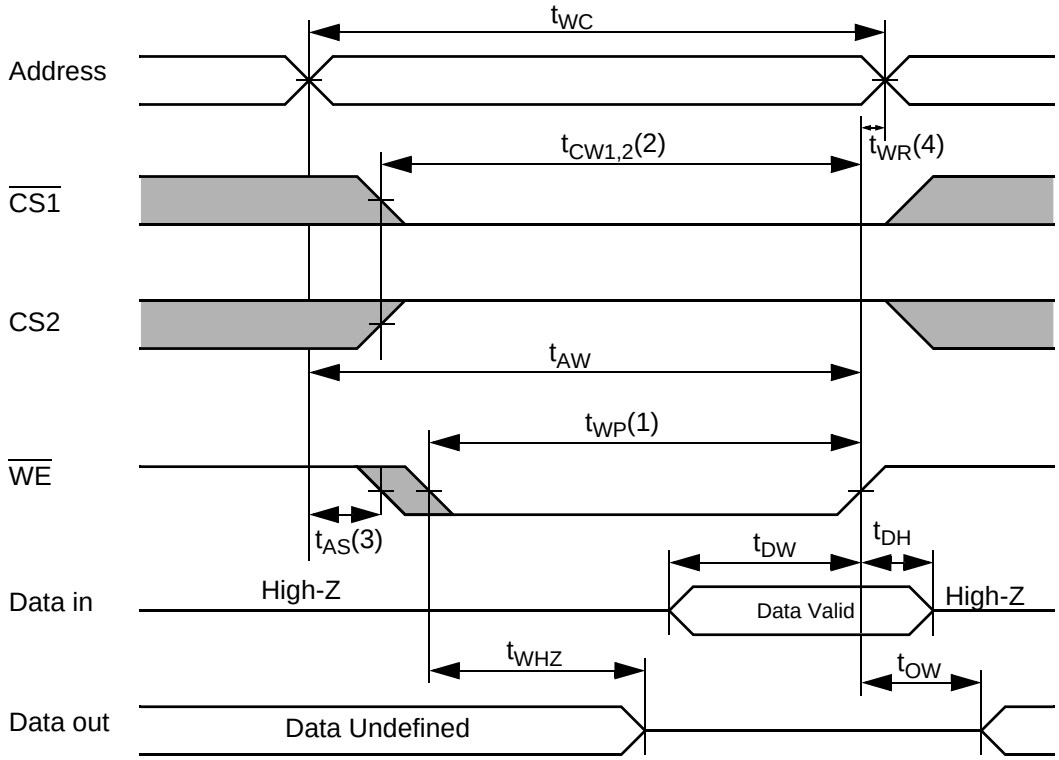
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})



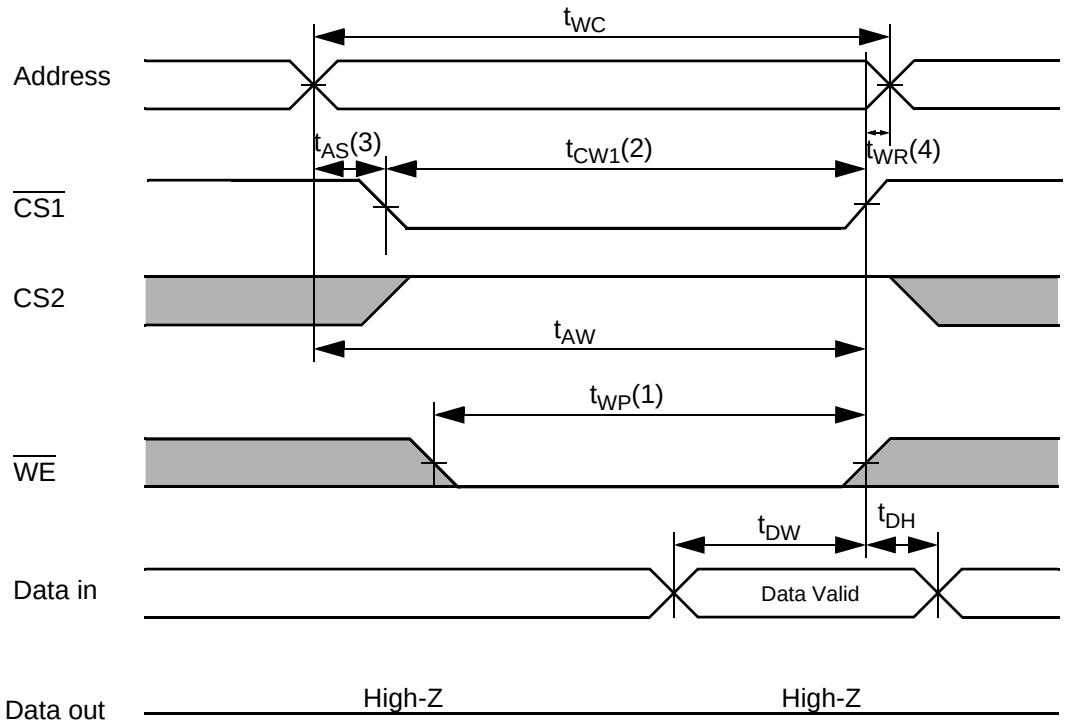
NOTES (READ CYCLE)

1. $t_{HZ1,2}$ and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ1,2}$(Max.) is less than $t_{LZ1,2}$(Min.) both for a given device and from device to device interconnection.

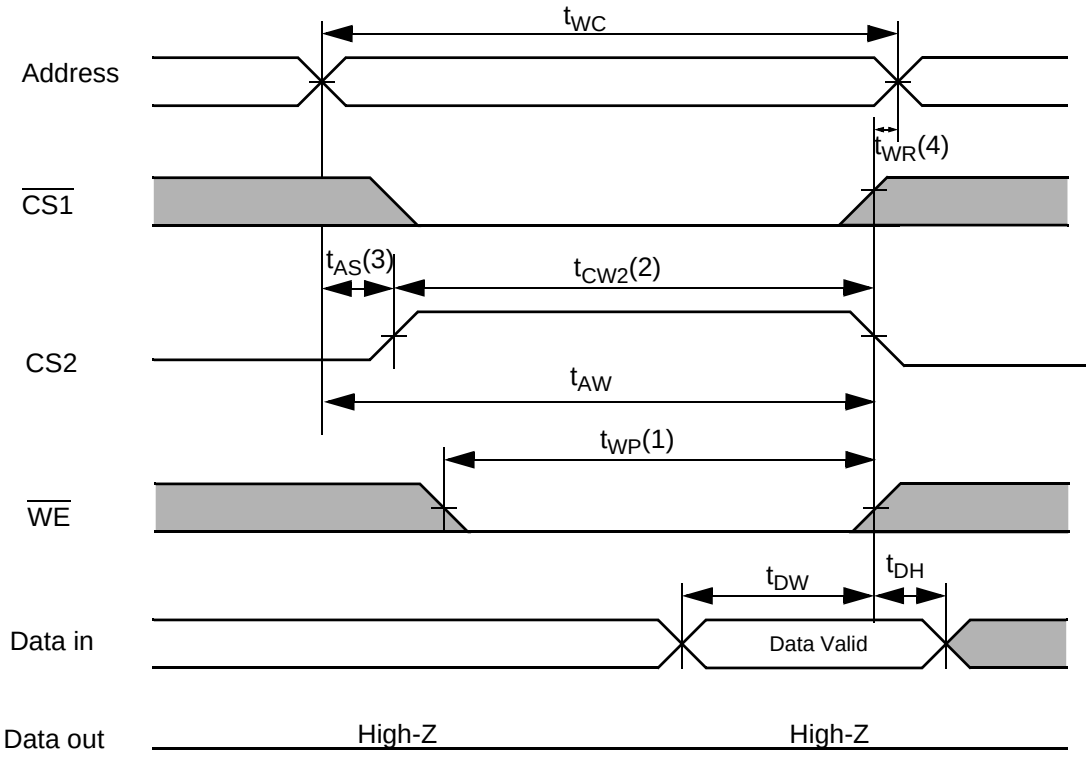
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ goes low, CS2 goes high and $\overline{WE}$ goes low. A write ends at the earliest transition among $\overline{CS1}$ goes high, CS2 goes low and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low.

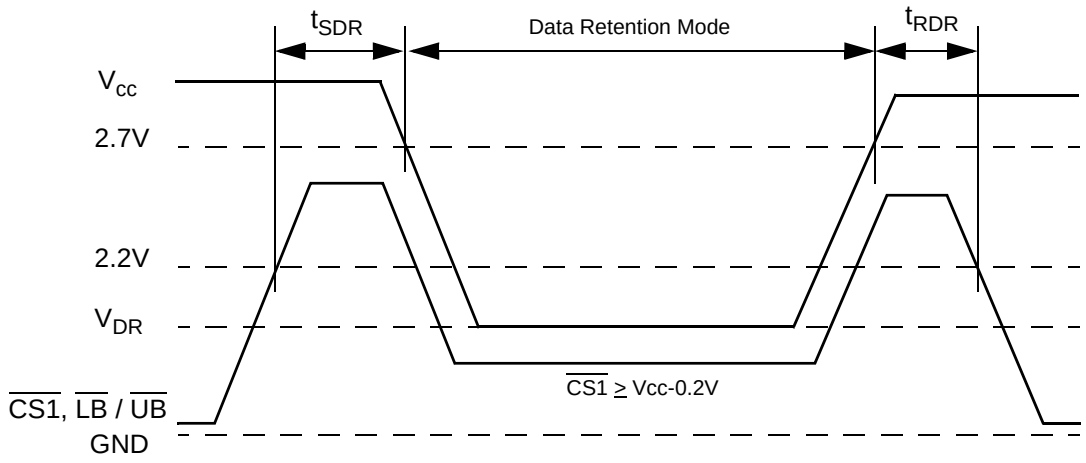
DATA RETENTION CHARACTERISTICS

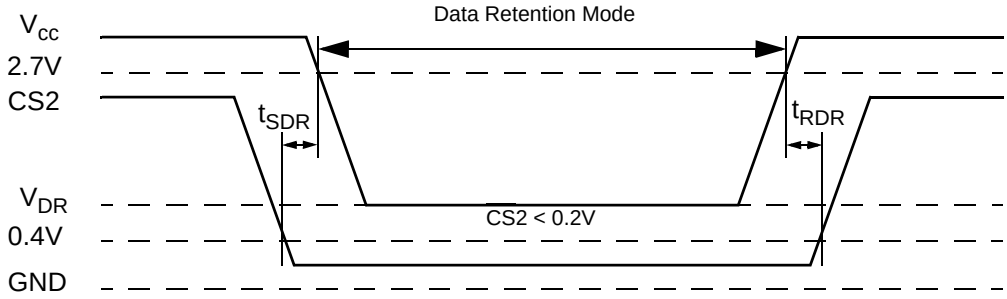
Parameter	Symbol	Test Condition	Min	Typ[2)]	Max	Unit
V_{CC} for Data Retention	V_{DR}	I_{SB1} Test Condition (Chip Disabled)[1)]	1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC}=1.5V, I_{SB1} Test Condition (Chip Disabled)[1)]	-	0.5	5.0	μA
Chip Deselect to Data Retention Time	t_{SDR}	See data retention wave form	0	-	-	ns
Operation Recovery Time	t_{RDR}		t_{RC}	-	-	

NOTES

1. See the I_{SB1} measurement condition of datasheet page 5.
2. Typical values are measured at T_A=25°C and not 100% tested.

DATA RETENTION WAVE FORM

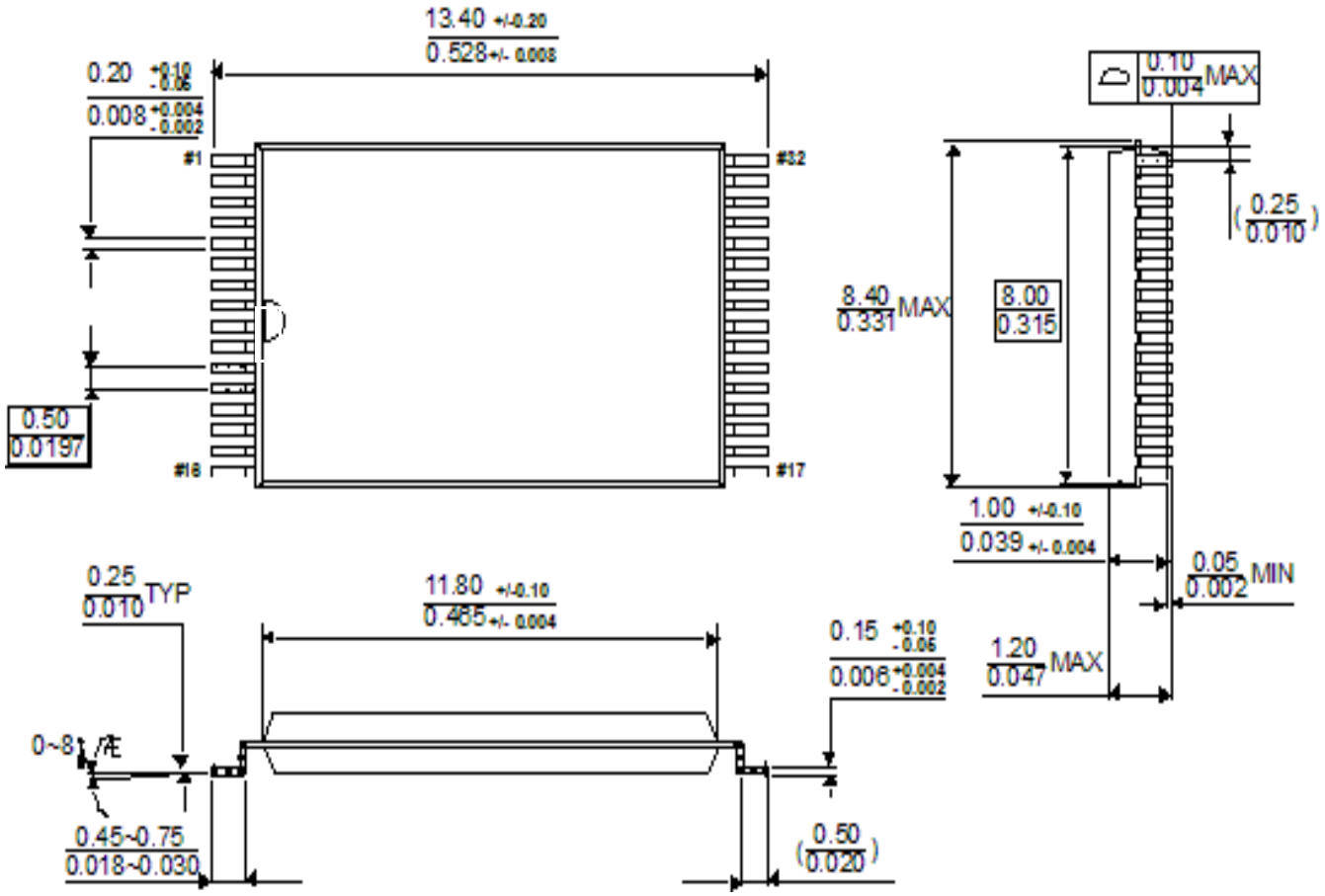




PACKAGE DIMENSION

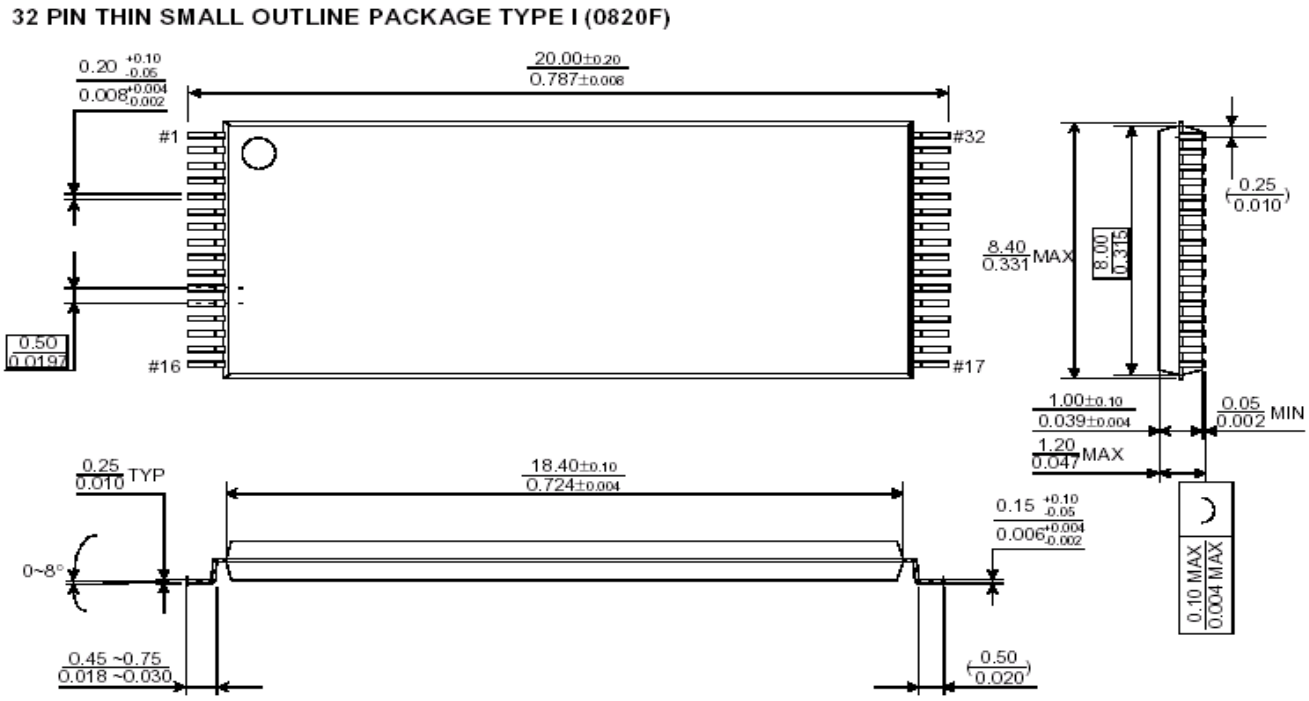
32Pin - sTSOP Type1

Unit : millimeters/Inches



32Pin - TSOP Type1

Unit : millimeters/Inches



MEMORY FUNCTION GUIDE

EM X XX X X X XX X X - XX XX

1. EMLSI Memory
2. Device Type
3. Density
4. Function
5. Technology
6. Operating Voltage
7. Organization
8. Version
9. Package
10. Speed
11. Power

1. Memory Component

2. Device Type

6	----------	Low Power SRAM
7	----------	STRAM
C	----------	CellularRAM

3. Density

1	----------	1M
2	----------	2M
4	----------	4M
8	----------	8M
16	----------	16M
32	----------	32M
64	----------	64M
28	----------	128M

4. Option

0	----------	Dual CS
1	----------	Single CS

5. Technology

F	----------	Full CMOS

6. Operating Voltage

T	----------	5.0V
V	----------	3.3V
U	----------	3.0V
S	----------	2.5V
R	----------	2.0V
P	----------	1.8V

7. Organization

8	----------	X8 bit
16	----------	X16 bit
32	----------	X32 bit

8. Version

Blank	----------	Mother die
A	----------	2 nd generation
B	----------	3 rd generation
C	----------	4 th generation
D	----------	5 th generation
E	----------	6 th generation
F	----------	7 th generation
G	----------	8 th generation

9. Package

Blank	----------	KGD, FBGA
S	----------	32 sTSOP1
T	----------	32 TSOP1
U	----------	44 TSOP2
V	----------	32 SOP

10. Speed

45	----------	45ns
55	----------	55ns
60	----------	60ns
70	----------	70ns
85	----------	85ns
90	----------	90ns
10	----------	100ns
12	----------	120ns

11. Power

LL	----------	Low Low Power
LF	----------	Low Low Power(Pb-free & Green)
L	----------	Low Power
S	----------	Standard Power