



512M X 16 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 10ns
- **low power consumption:**
Operating current:
80mA (TYP. 10/ns)
Standby current:
3mA(TYP)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II
48-ball 6mmx8mm TFBGA

GENERAL DESCRIPTION

The AS7C38098A is a 8M-bit high speed CMOS static random access memory organized as 512K words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C38098A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

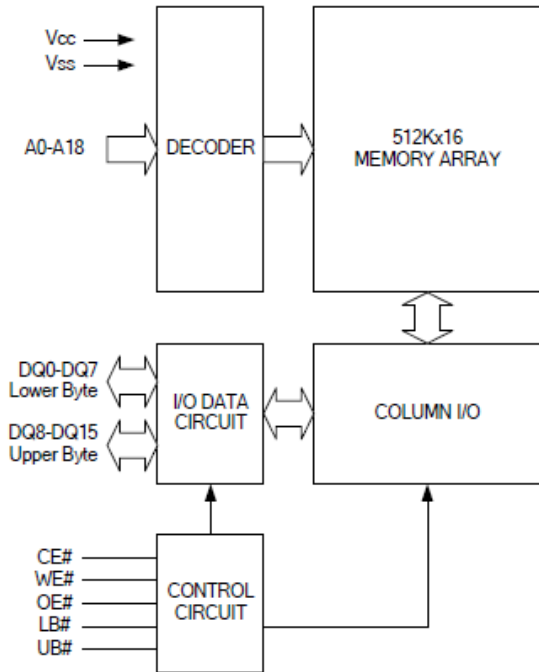
PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed | Power Dissipation | |
|----------------|-----------------------|------------|-------|--------------------|----------------------|
| | | | | Standby(Isb1,TYP.) | Operating(Icc1,TYP.) |
| AS7C38098A | -40 ~ 85°C | 2.7 ~ 3.6V | 10ns | 3mA | 80/70mA |



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FUNCTIONAL BLOCK DIAGRAM



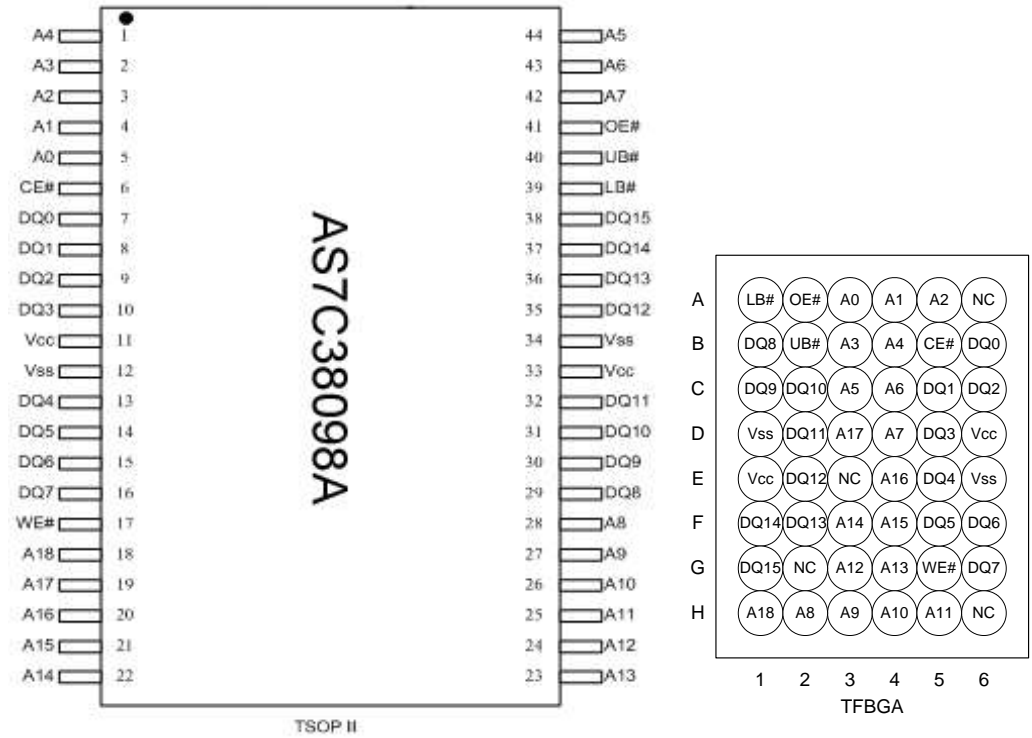
PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|------------|---------------------|
| A0 - A18 | Address Inputs |
| DQ0 – DQ15 | Data Inputs/Outputs |
| CE# | Chip Enable Input |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| LB# | Lower Byte Control |
| UB# | Upper Byte Control |
| Vcc | Power Supply |
| Vss | Ground |



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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|--|---------------------|--------------------|------|
| Terminal Voltage with Respect to V _{SS} | V _{TERM} | -0.5 to 4.6 | V |
| Operating Temperature | T _A | 0 to 70(C grade) | °C |
| | | -40 to 85(I grade) | |
| Storage Temperature | T _{STG} | -65 to 150 | °C |
| Power Dissipation | P _D | 1 | W |
| DC Output Current | I _{OUT} | 50 | mA |
| Soldering Temperature (under 10 sec) | T _{SOLDER} | 260 | °C |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



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TRUTH TABLE

| MODE | CE# | OE# | WE# | LB# | UB# | I/O OPERATION | | SUPPLY CURRENT |
|----------------|-----|-----|-----|-----|-----|------------------|------------------|------------------|
| | | | | | | DQ0-DQ7 | DQ8-DQ15 | |
| Standby | H | X | X | X | X | High - Z | High - Z | I _{SB1} |
| Output Disable | L | H | H | X | X | High - Z | High - Z | I _{CC} |
| | L | X | X | H | H | High - Z | High - Z | |
| Read | L | L | H | L | H | D _{OUT} | High - Z | I _{CC} |
| | L | L | H | H | L | High - Z | D _{OUT} | |
| | L | L | H | L | L | D _{OUT} | D _{OUT} | |
| Write | L | X | L | L | H | D _{IN} | High - Z | I _{CC} |
| | L | X | L | H | L | High - Z | D _{IN} | |
| | L | X | L | L | L | D _{IN} | D _{IN} | |

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. ⁴ | MAX. | UNIT | |
|--|------------------------------|---|------|-------------------|------|----------------------|----|
| Supply Voltage | V _{CC} | | -10 | 2.7 | 3.3 | 3.6 | V |
| Input High Voltage | V _{IH} ¹ | | | 2.2 | - | V _{CC} +0.3 | V |
| Input Low Voltage | V _{IL} ² | | | -0.3 | - | 0.8 | V |
| Input Leakage Current | I _{LI} | V _{CC} ≥ V _{IN} ≥ V _{SS} | | -1 | - | 1 | μA |
| Output Leakage Current | I _{LO} | V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled | | -1 | - | 1 | μA |
| Output High Voltage | V _{OH} | I _{OH} = -8mA | | 2.4 | - | - | V |
| Output Low Voltage | V _{OL} | I _{OL} = 4mA | | - | - | 0.4 | V |
| Average Operating Power supply Current | I _{CC} | CE# = V _{IL} , I _{I/O} = 0mA ;f=max | -10 | - | 100 | 130 | mA |
| | I _{CC1} | CE# ≥ V _{CC} - 0.2V, Other pin is at 0.2V or V _{CC} -0.2V, I _{I/O} = 0mA;f=max | -10 | | 80 | 110 | mA |
| Standby Power Supply Current | I _{SB} | CE# ≥ V _{IH} Other pin is at V _{IL} or V _{IH} | | | | 40 | mA |
| Standby Power Supply Current | I _{SB1} | CE# ≥ V _{CC} - 0.2V; Other pin is at 0.2V or V _{CC} -0.2V | | | 3 | 25 | mA |

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C



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CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|--------------------------|-----------|------|-----|------|
| Input Capacitance | C_{IN} | - | 8 | pF |
| Input/Output Capacitance | $C_{I/O}$ | - | 10 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

| | |
|--|---|
| speed | 10ns |
| Input Pulse Levels | 0.2V to $V_{CC}-0.2\text{V}$ |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | $C_L = 30\text{pF} + 1\text{TTL}$, $I_{OH}/I_{OL} = -4\text{mA}/8\text{mA}$ |

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

| PARAMETER | SYM. | AS7C38098A-10 | | UNIT |
|------------------------------------|-------------|---------------|------|------|
| | | MIN. | MAX. | |
| Read Cycle Time | t_{RC} | 10 | - | ns |
| Address Access Time | t_{AA} | - | 10 | ns |
| Chip Enable Access Time | t_{ACE} | - | 10 | ns |
| Output Enable Access Time | t_{OE} | - | 4.5 | ns |
| Chip Enable to Output in Low-Z | t_{CLZ}^* | 2 | - | ns |
| Output Enable to Output in Low-Z | t_{OLZ}^* | 0 | - | ns |
| Chip Disable to Output in High-Z | t_{CHZ}^* | - | 4 | ns |
| Output Disable to Output in High-Z | t_{OHZ}^* | - | 4 | ns |
| Output Hold from Address Change | t_{OH} | 2 | - | ns |
| LB#, UB# Access Time | t_{BA} | - | 4.5 | ns |
| LB#, UB# to High-Z Output | t_{BHZ}^* | - | 4 | ns |
| LB#, UB# to Low-Z Output | t_{BLZ}^* | 0 | - | ns |

(2) WRITE CYCLE

| PARAMETER | SYM. | AS7C38098A-10 | | UNIT |
|----------------------------------|-------------|---------------|------|------|
| | | MIN. | MAX. | |
| Write Cycle Time | t_{WC} | 10 | - | ns |
| Address Valid to End of Write | t_{AW} | 8 | - | ns |
| Chip Enable to End of Write | t_{CW} | 8 | - | ns |
| Address Set-up Time | t_{AS} | 0 | - | ns |
| Write Pulse Width | t_{WP} | 8 | - | ns |
| Write Recovery Time | t_{WR} | 0 | - | ns |
| Data to Write Time Overlap | t_{DW} | 6 | - | ns |
| Data Hold from End of Write Time | t_{DH} | 0 | - | ns |
| Output Active from End of Write | t_{OW}^* | 2 | - | ns |
| Write to Output in High-Z | t_{WHZ}^* | - | 4 | ns |
| LB#, UB# Valid to End of Write | t_{BW} | 8 | - | ns |

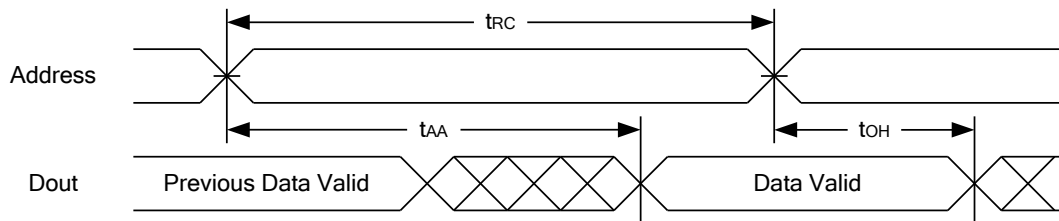
*These parameters are guaranteed by device characterization, but not production tested.



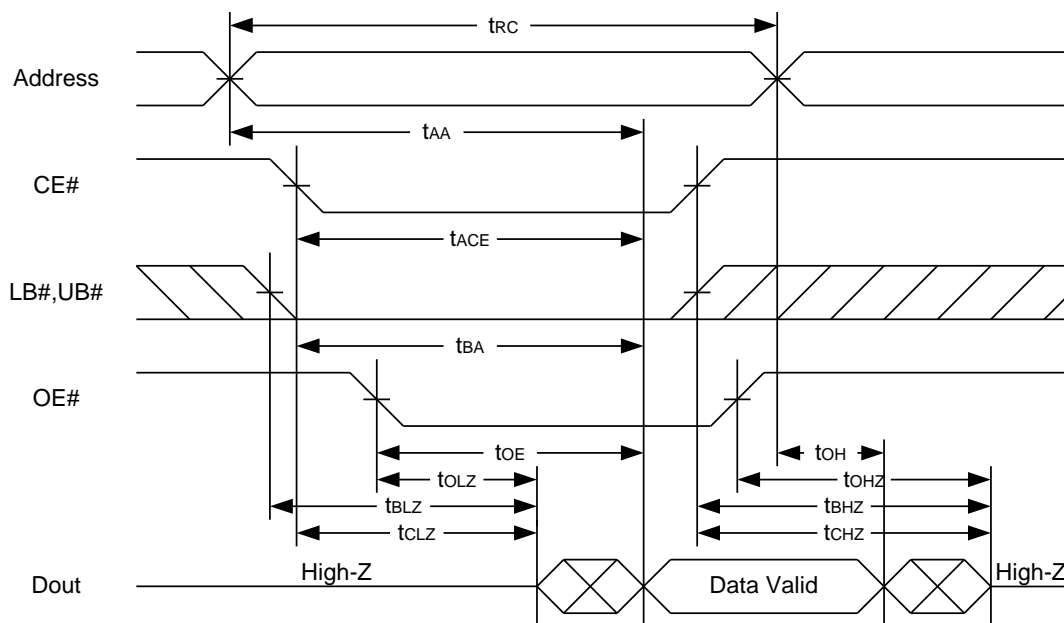
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TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



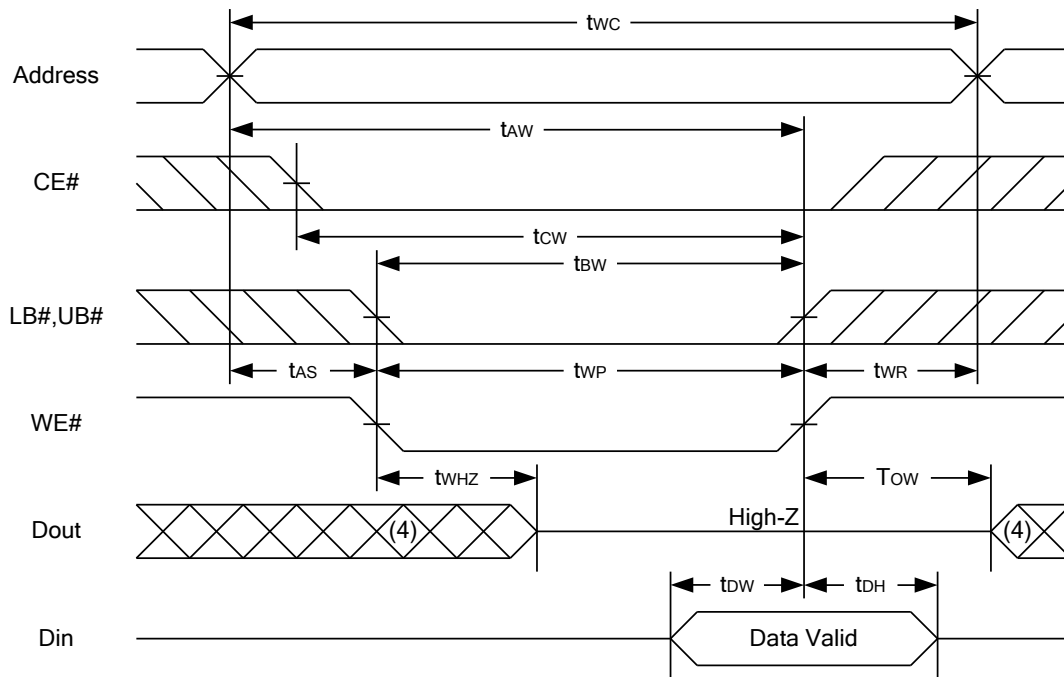
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .

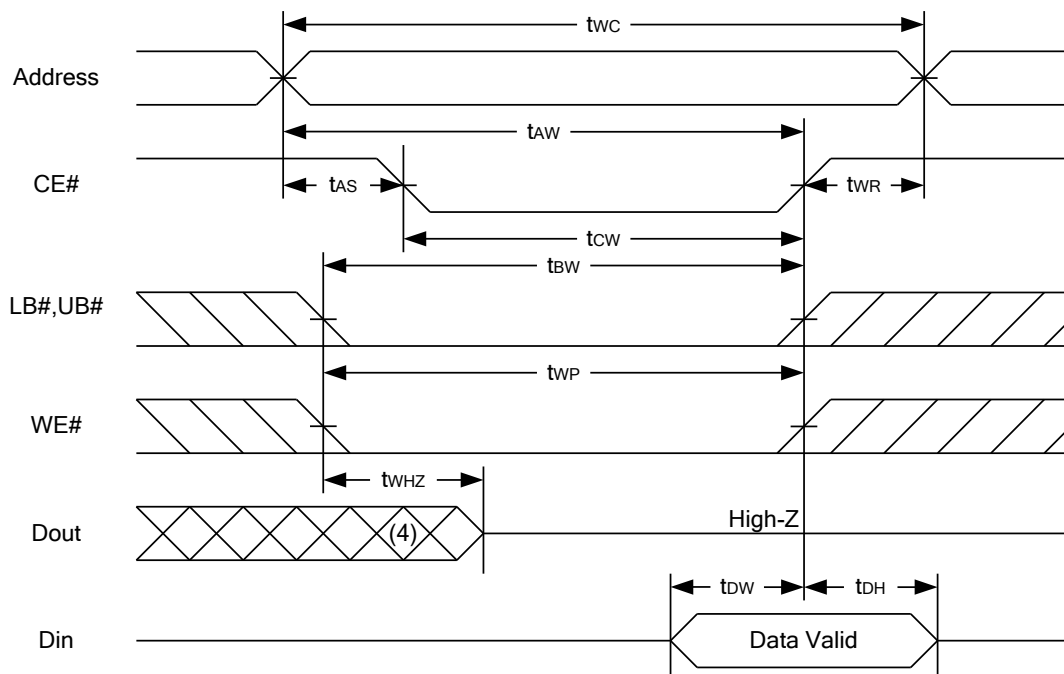


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WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



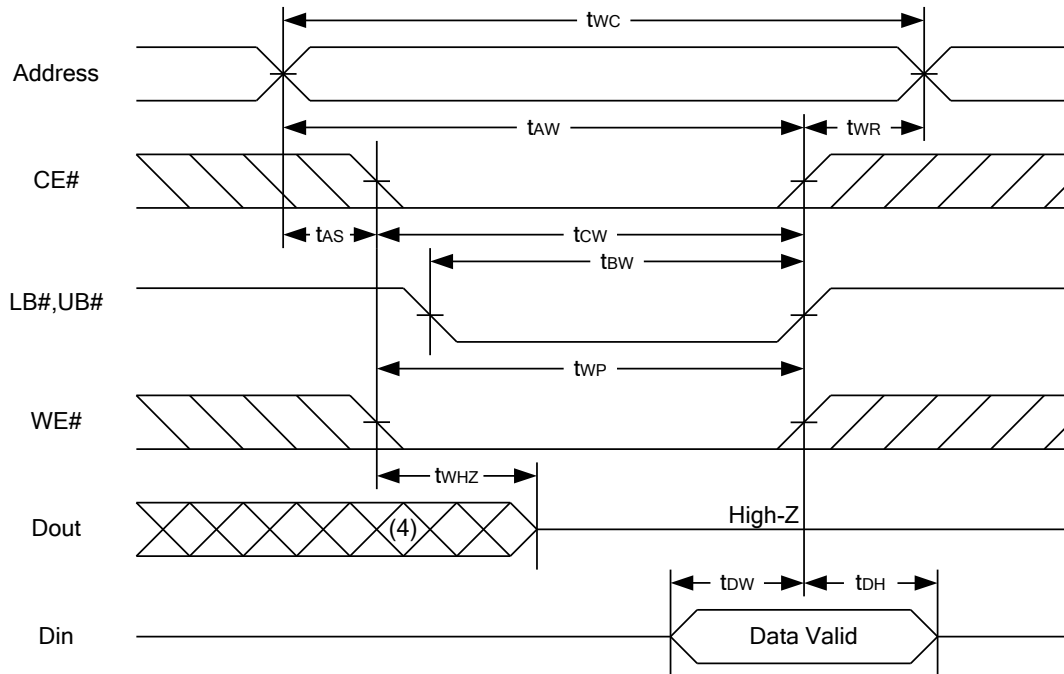
WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)





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WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE#, LB#, UB# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, twp must be greater than twhz + tdw to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tow and twhz are specified with CL = 5pF. Transition is measured ±500mV from steady state.



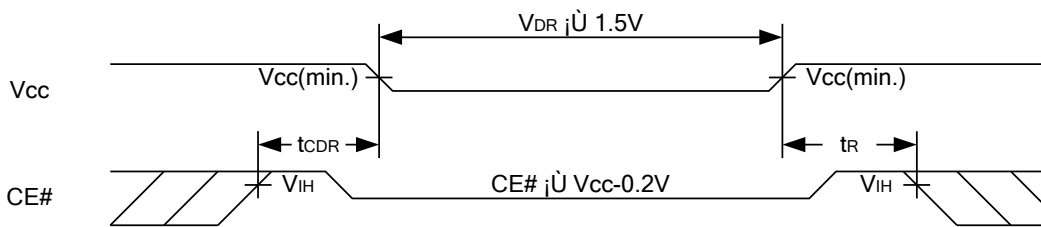
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DATA RETENTION CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|-----------|---|------------|------|------|------|
| VCC for Data Retention | V_{DR} | $CE\# \geq V_{CC} - 0.2V$ | 1.5 | - | 3.6 | V |
| Data Retention Current | I_{DR} | $V_{CC} = 1.5V$ $CE\# \geq V_{CC} - 0.2V$; Other pin is at 0.2V or $V_{CC} - 0.2V$ | - | 3 | 25 | mA |
| Chip Disable to Data Retention Time | t_{CDR} | See Data Retention Waveforms (below) | 0 | - | - | ns |
| Recovery Time | t_R | | t_{RC}^* | - | - | ns |

t_{RC}^* = Read Cycle Time

DATA RETENTION WAVEFORM

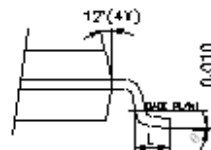
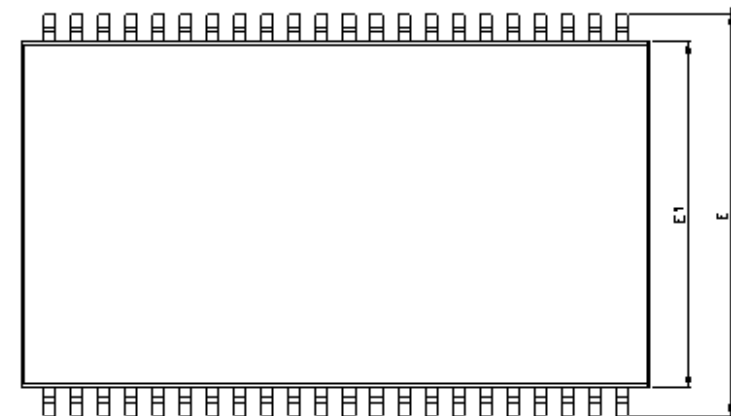




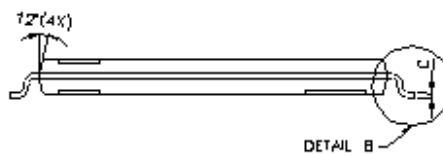
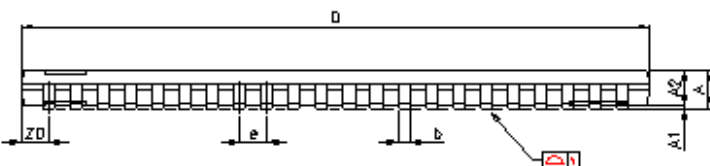
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PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-II Package Outline Dimension



DETAIL B



DETAIL B

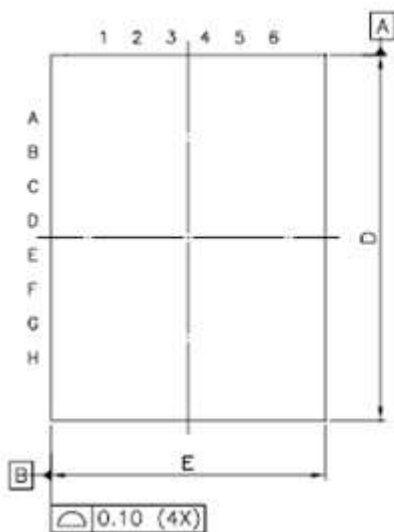
| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN MILS | | |
|---------|---------------------------|--------|--------|--------------------|------|------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | - | - | 1.20 | - | - | 47.2 |
| A1 | 0.05 | 0.10 | 0.15 | 2.0 | 3.9 | 5.9 |
| A2 | 0.95 | 1.00 | 1.05 | 37.4 | 39.4 | 41.3 |
| b | 0.30 | - | 0.45 | 11.8 | - | 17.7 |
| c | 0.12 | - | 0.21 | 4.7 | - | 8.3 |
| D | 18.212 | 18.415 | 18.618 | 717 | 725 | 733 |
| E | 11.506 | 11.760 | 12.014 | 453 | 463 | 473 |
| E1 | 9.957 | 10.160 | 10.363 | 392 | 400 | 408 |
| e | - | 0.800 | - | - | 31.5 | - |
| L | 0.40 | 0.50 | 0.60 | 15.7 | 19.7 | 23.6 |
| ZD | - | 0.805 | - | - | 31.7 | - |
| y | - | - | 0.076 | - | - | 3 |
| θ | 0° | 3° | 6° | 0° | 3° | 6° |



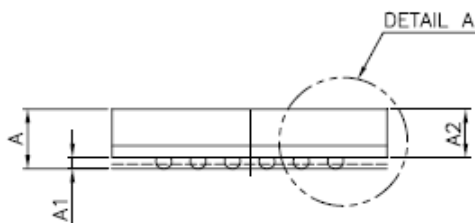
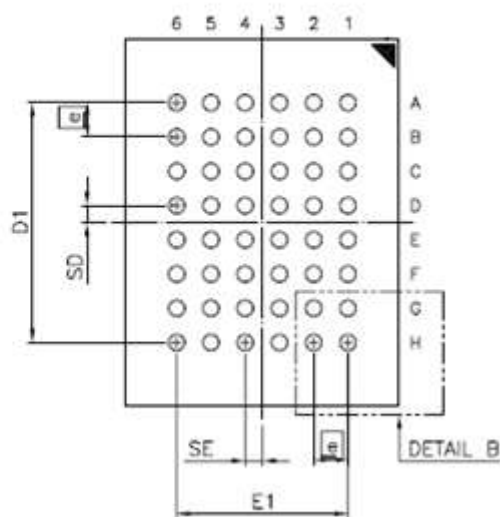
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48-ball 6mm x 8mm TFBGA Package Outline Dimension

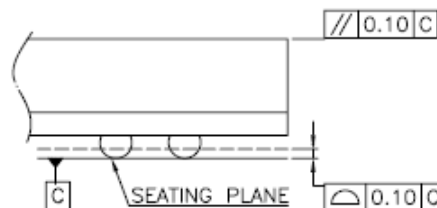
TOP VIEW



BOTTOM VIEW

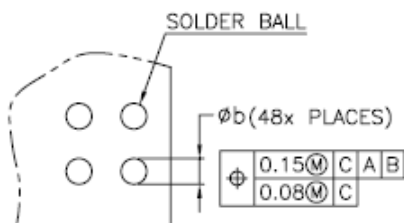


SIDE VIEW



DETAIL A

| SYM. | DIMENSION (mm) | | | DIMENSION (inch) | | |
|------|----------------|------|------|------------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.40 | — | — | 0.055 |
| A1 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| A2 | — | — | 1.05 | — | — | 0.041 |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| D | 7.95 | 8.00 | 8.05 | 0.313 | 0.315 | 0.317 |
| D1 | 5.25 BSC | | | 0.207 BSC | | |
| E | 5.95 | 6.00 | 6.05 | 0.234 | 0.236 | 0.238 |
| E1 | 3.75 BSC | | | 0.148 BSC | | |
| SE | 0.375 TYP | | | 0.015 TYP | | |
| SD | 0.375 TYP | | | 0.015 TYP | | |
| Ⓢ | 0.75 BSC | | | 0.030 BSC | | |



DETAIL B

NOTE:

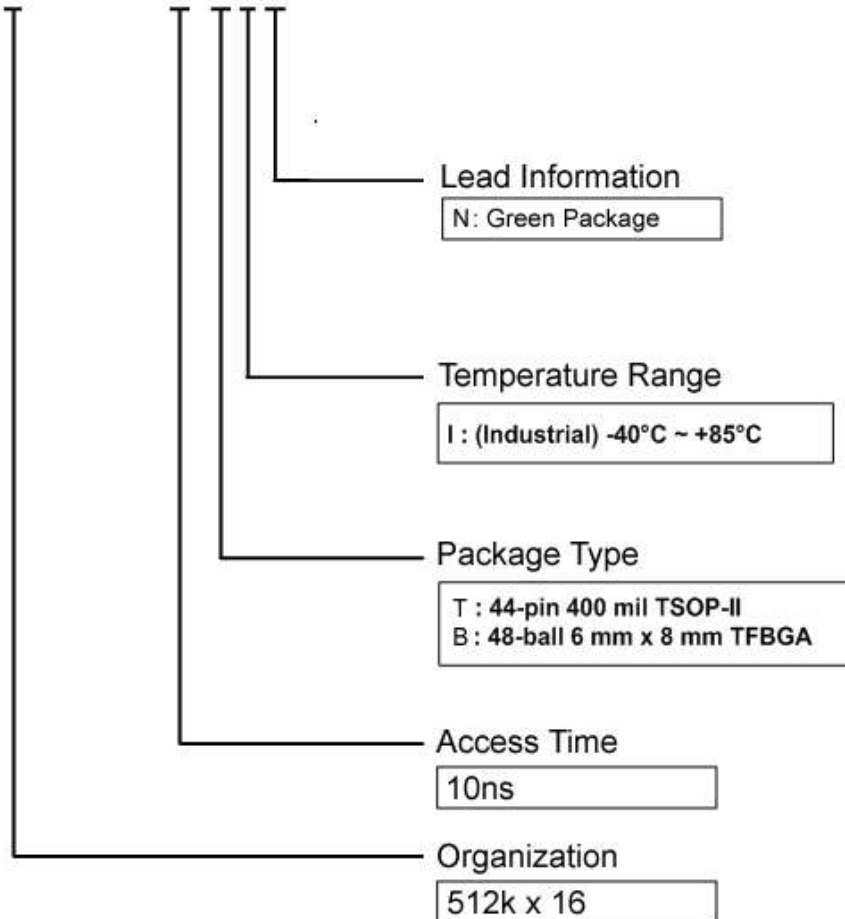
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.



512M X 16 BIT HIGH SPEED CMOS SRAM

ORDERING INFORMATION

AS7C38098A - 10 x I N



| | | |
|----------------------------------|--------------------------|------------------|
| BGA : 48-ball 6 mm x 8 mm TFBGA | Industrial -40°C ~ +85°C | AS7C38098A-10BIN |
| TSOP II : 44-pin 400 mil TSOP II | Industrial -40°C ~ +85°C | AS7C38098A-10TIN |