Preliminary Specification

PRODUCT NUMBER: 9OL9935801000
PRODUCT DESCRIPTION: RGS27128064YR000

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REV.: X01   2017/03/30

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2017. 03. 30	

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored in the original packages at 25°C±5°C, 55%±10%RH or used as the conditions specified in the specifications.

Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : Yellow
- Panel resolution : 128x64
- Driver IC : SPD0301
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 2.02 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800/8080-series parallel interface, Serial Peripheral Interface, I^{2}C Interface.
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 64	dot
2	Dot Size	0.45 (W) x 0.45 (H)	mm^2
3	Dot Pitch	0.48 (W) x 0.48 (H)	mm^2
4	Aperture Rate	88	%
5	Active Area	61.41 (W) x 30.69 (H)	mm^2
6	Panel Size	64.61 (W) x 37 (H)	mm^2
7	Panel Thickness	1.82 $\pm$ 0.1	mm
8	Module Size	64.61 (W) x 109.92 (H) x 2.02 (T)	mm^3
9	Diagonal A/A size	2.7	inch
10	Module Weight	TBD	gram

* Panel thickness includes substrate glass, cover glass and UV glue
thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	4	V	Ta = 25℃	IC maximum rating
Supply Voltage (Vcc)	8	17	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃		-
Storage Temp	-40	85	℃		Note (2)

Note:

(1) Maximum ratings are those values beyond which damages to the OLED module may occur. The OLED functional operation should be restricted to the limits in the section 6. Electrical Characteristics tables.

(2) The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Operating Voltage (for OLED panel)	Ta = 25℃	TBD	TBD	TBD	V
V_{DD}	Logic Supply Voltage	Ta = 25℃	1.65	-	3.3	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	$0.9* V_{DD}$	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	$0.1*V_{DD}$	V
V_{IH}	High Logic Input Level	-	$0.8* V_{DD}$	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	$0.2*V_{DD}$	V

REV.: X01   2017/03/30

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption (ICC)	-	TBD	TBD	mA	All pixels on (1)
	-	TBD	TBD	mA	20% pixels on (1)
Standby mode current consumption (ICC)	-	TBD	TBD	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	TBD	TBD	mW	All pixels on (1)
	-	TBD	TBD	mW	20% pixels on (1)
Standby mode power consumption	-	TBD	TBD	mW	Standby mode 10% pixels on (2)
IDD sleep mode current	-	-	10	uA	Sleep mode Current (3)
ICC sleep mode current	-	-	10	uA	Sleep mode Current (3)
Pixel Luminance	TBD	TBD		cd/m^2	Display Average
Standby Luminance		TBD		cd/m^2	
CIEx (Yellow)	0.43	0.47	0.51		CIE1931
CIEy (Yellow)	0.45	0.49	0.53		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		µs	

(1) Normal mode condition :
- Driving Voltage : TBD
- Contrast setting : TBD
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition :
- Driving Voltage : TBD
- Contrast setting : TBD
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Sleep mode condition :
When send 0xae command OLED display off and memory data will be maintained.

(4) Wake up condition :
When send 0xaf command OLED will be turned on.

7. LIFETIME SPECIFICATION

ITEM	MIN	UNIT	Condition	Remark
Life Time	TBD	Hrs	TBD cd/m^2, 50% checkerboard	Note (1)

Note:
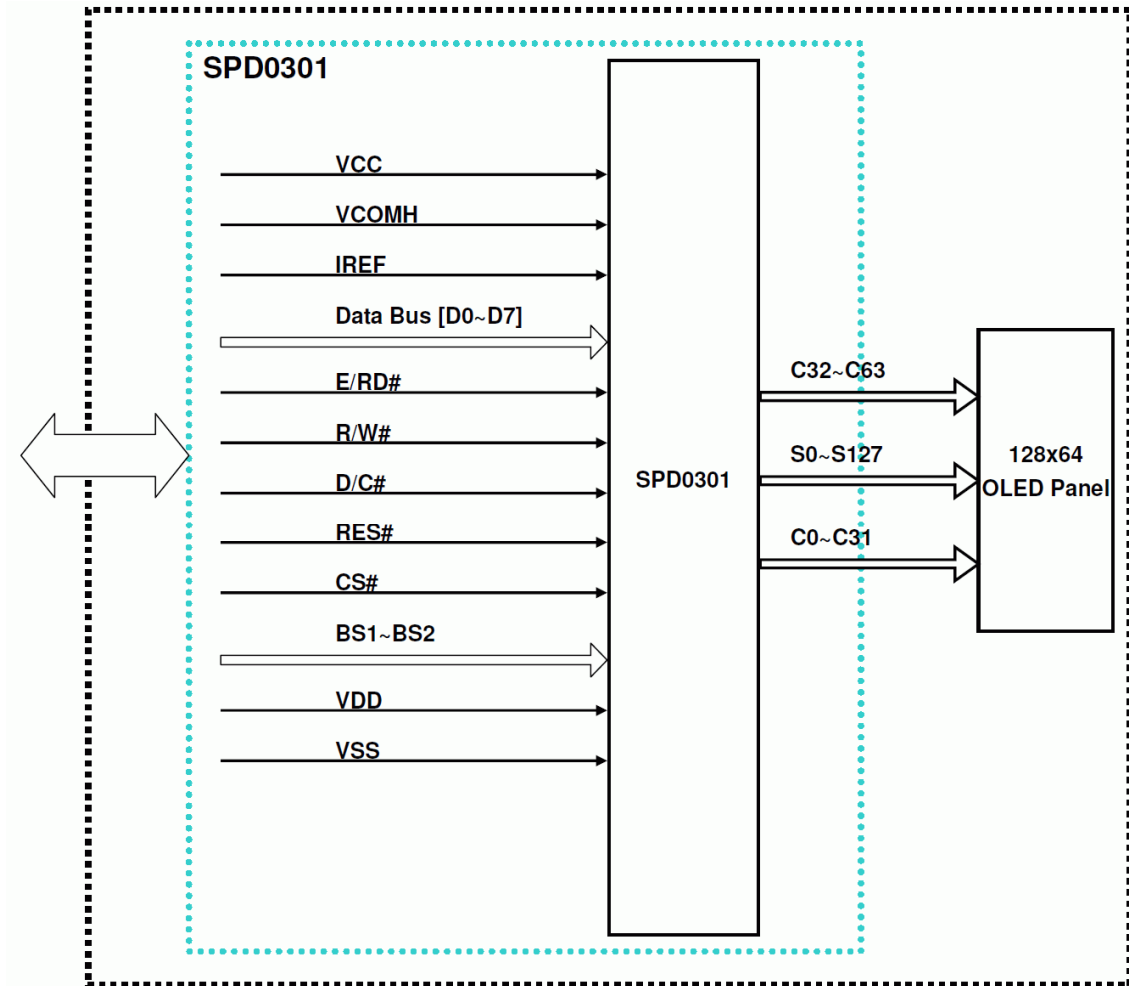
   (A) Under VCC = TBD, Ta = 25℃, 50% RH.

   (B) Life time is defined the amount of time when the luminance has decayed
        to less than 50% of the initial measured luminance.

(1) Setting of TBD cd/m^2 :
   - Contrast setting : TBD
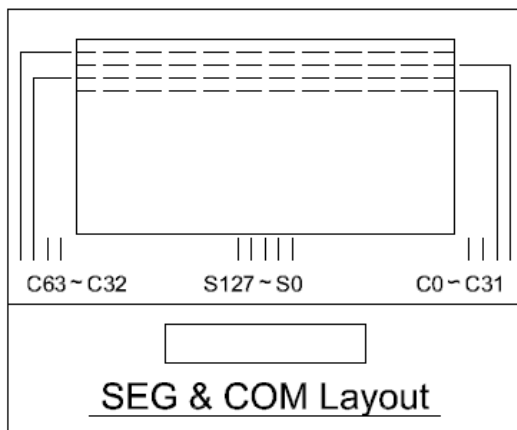   - Frame rate : 105Hz
   - Duty setting : 1/64

8. INTERFACE

8.1 FUNCTION BLOCK DIAGRAM

RiTdisplay 128x64 OLED Module

8.2 PANEL LAYOUT DIAGRAM

8.3 PIN ASSIGNMENTS

Pin No.	Pin Name	Description	Setting at each interface		
			8080 parallel	SPI	IIC
1	VCC	Power supply for panel driving voltage.			
2	VCOMH	Com Voltage Output. A capacitor should be connected between this pin and VSS.			
3	IREF	The current reference input pin, a resistor should be connected between this pin and VSS.			
4	D7	These pins are bi-directional data bus connecting to the MCU data bus. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I^{2}C mode is selected, D2, D1 should be tied together and serve as SDA$_{out}$, SDA$_{in}$ in application and D0 is the serial clock input, SCL.	D7	Tie LOW	Tie LOW
5	D6		D6	Tie LOW	Tie LOW
6	D5		D5	Tie LOW	Tie LOW
7	D4		D4	Tie LOW	Tie LOW
8	D3		D3	Tie LOW	Tie LOW
9	D2		D2	NC	SDAOUT
10	D1		D1	SDIN	SDAIN
11	D0		D0	SCLK	SCL
12	E/RD#	8080: data read enable pin; 6800:Read/Write enable pin.When serial or I^{2}C interface is selected, this pin must be connected to VSS.	E/RD#	Tie LOW	Tie LOW
13	R/W#	This pin is read / write control input pin connecting to the MCU interface. 8080: data write enable pin; 6800:Read/Write select pin.When serial or I^{2}C interface is selected, this pin must be connected to VSS.	R/W#	Tie LOW	Tie LOW
14	D/C#	This is Data/Command control pin.	D/C#	D/C#	SA0
15	RES#	Reset signal input.			
16	CS#	Chip select input.	CS#	CS#	Tie LOW
17	BS2	MCU bus interface selection pins.	High	Low	Low
18	BS1		High	Low	High
19	VDD	Power supply for logic circuit.			
20	NC	No connection.			
21	VSS	Ground pin.			
22	VSS	Ground pin.			

Note

(1) Low is connected to VSS

(2) High is connected to VDD

8.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in below figures.

GDDRAM pages structure of SPD0301

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 --SEG127	
Column re-mapping	SEG127 --SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in below figures.

Enlargement of GDDRAM (No row re-mapping and column-remapping)

Each box represents one bit of image data
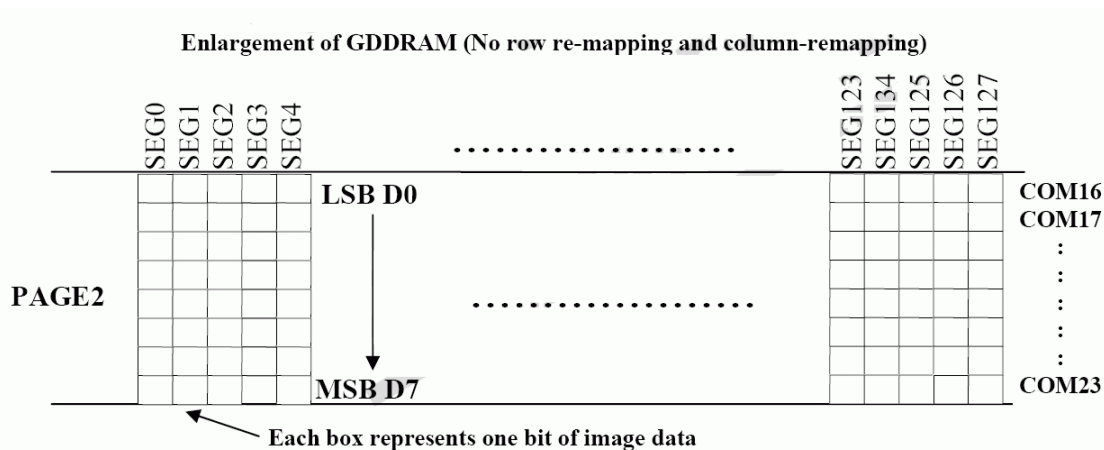
For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

8.5 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V ~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DW}	Data Write Time	70	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics

Write cycle

Read Cycle
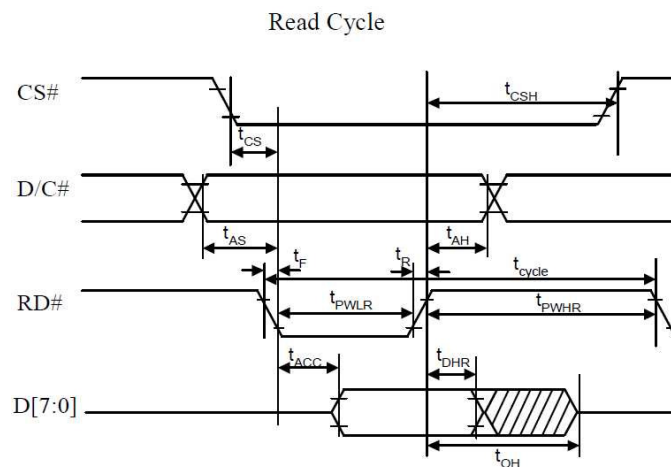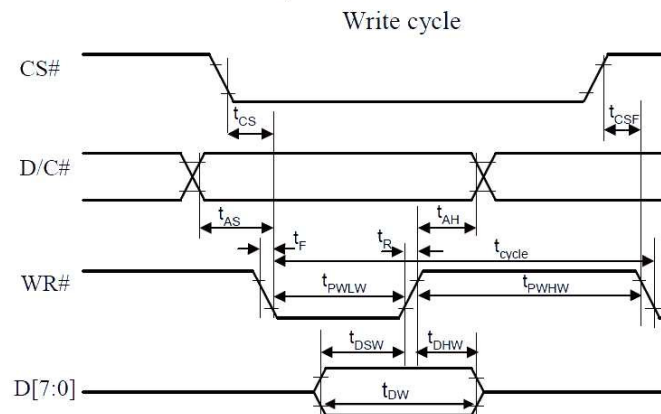
9. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

9.1 POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SPD0301

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [3] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. [1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

The Power ON sequence
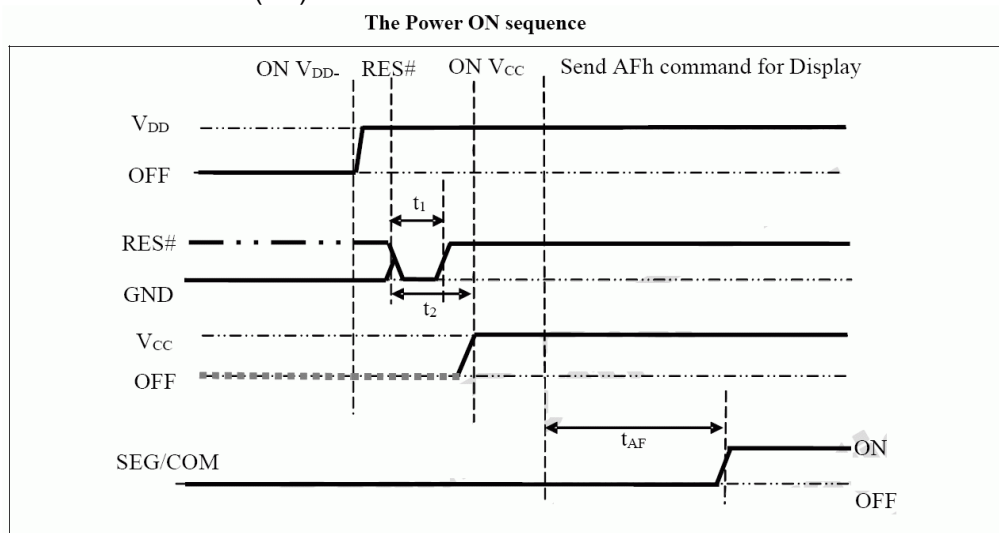
Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} [1], [2]
3. Power OFF V_{DD} after t_{OFF}.[4] (where Minimum t_{OFF}=80ms,Typical t_{OFF}=100ms)

The Power OFF sequence
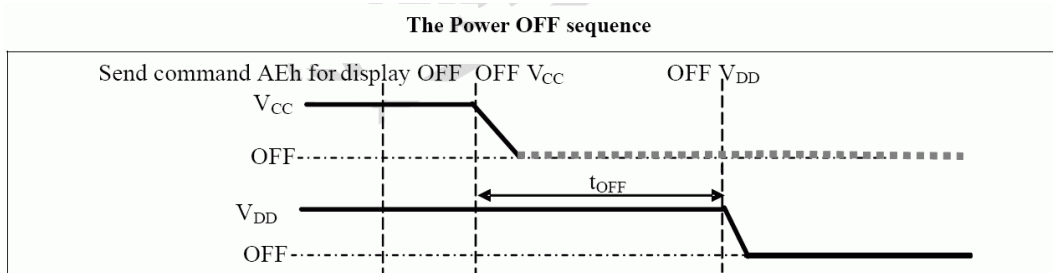
Note:

[1] V_{CC} should be disabled when it is OFF.

[2] Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

[3] The register values are reset after t_1.

[4] V_{DD} should not be Power OFF before V_{CC} Power OFF.

9.2 APPLICATION CIRCUIT

TBD

9.3 COMMAND TABLE

Refer to IC Spec.: SPD0301

10. RELIABILITY TEST CONDITIONS

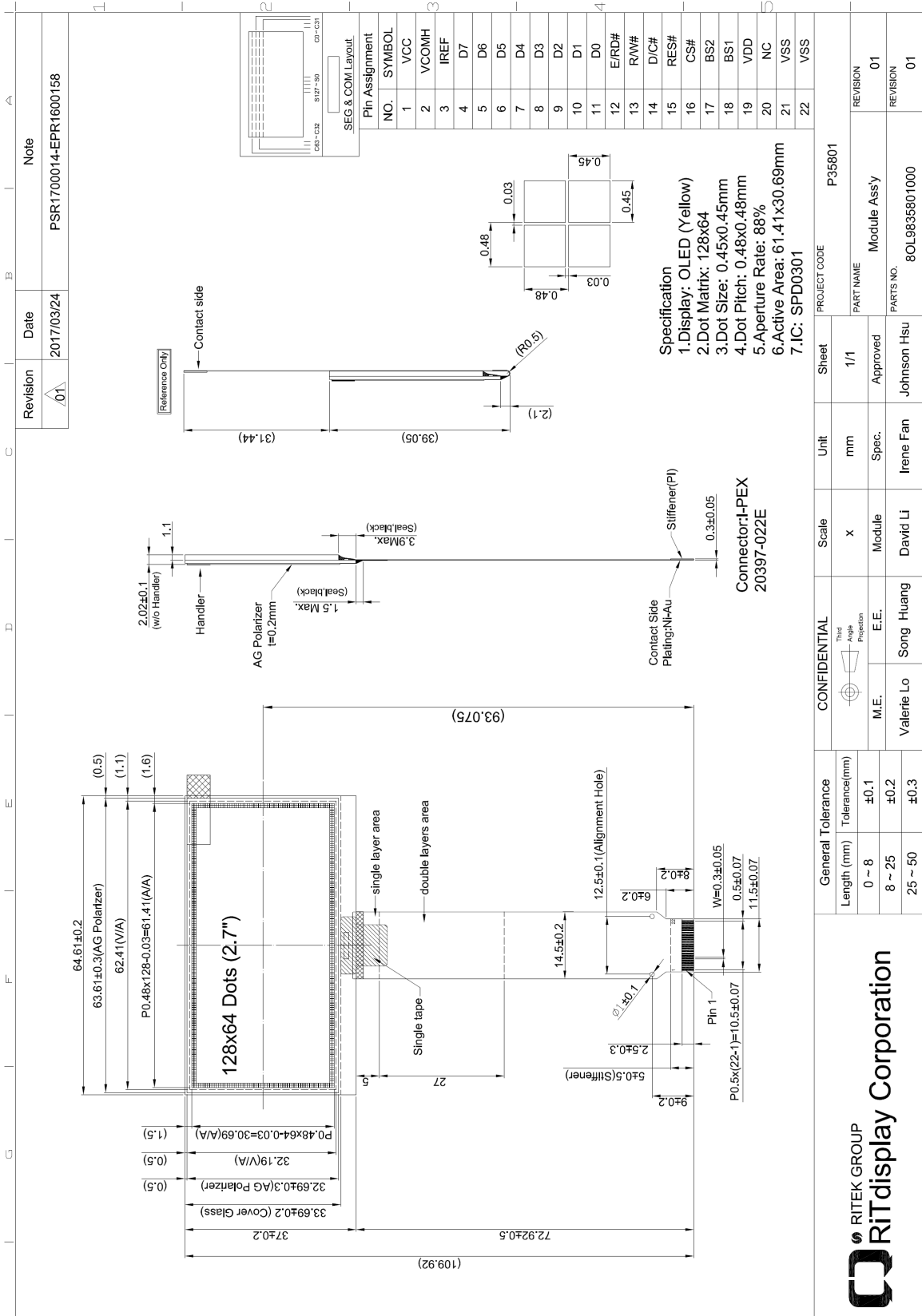| No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

REV.: X01   2017/03/30

11. EXTERNAL DIMENSION

Specification
1. Display: OLED (Yellow)
2. Dot Matrix: 128x64
3. Dot Size: 0.45x0.45mm
4. Dot Pitch: 0.48x0.48mm
5. Aperture Rate: 88%
6. Active Area: 61.41x30.69mm
7. IC: SPD0301

SEG & COM Layout

Pin Assignment

NO.	SYMBOL
1	VCC
2	VCOMH
3	IREF
4	D7
5	D6
6	D5
7	D4
8	D3
9	D2
10	D1
11	D0
12	E/RD#
13	R/W#
14	D/C#
15	RES#
16	CS#
17	BS2
18	BS1
19	VDD
20	NC
21	VSS
22	VSS

Note: PSR1700014-EPR1600158

Revision	Date
01	2017/03/24

Reference Only
Contact side

Connector:I-PEX
20397-022E
Contact Side
Plating:Ni-Au
Stiffener(PI)
0.3±0.05

AG Polarizer
t=0.2mm
Handler
2.02±0.1 (w/o Handler)
1.1
3.9Max. (Seal,black)
1.5 Max. (Seal,black)

128x64 Dots (2.7")

single layer area
double layers area
Single tape
Pin 1

64.61±0.2
63.61±0.3(AG Polarizer)
62.41(V/A)
P0.48x128-0.03=61.41(A/A)
(0.5) (1.1) (1.6)
(93.075)

P0.48x64-0.03=30.69(A/A)
32.19(V/A)
32.69±0.3(AG Polarizer)
33.69±0.2 (Cover Glass)
37±0.2
72.92±0.5
(109.92)

12.5±0.1(Alignment Hole)
14.5±0.2
W=0.3±0.05
0.5±0.07
11.5±0.07
8±0.2
6±0.2
9±0.2
2.5±0.3
5±0.5(Stiffener)
P0.5x(22-1)=10.5±0.07
5
27

RiTdisplay Corporation

PROJECT CODE	P35801
PART NAME	Module Ass'y
PARTS NO.	8OL9835801000

Sheet	1/1
Approved	Johnson Hsu
Spec.	Irene Fan
Module	David Li
E.E.	Song Huang
M.E.	Valerie Lo

| Unit | mm |
| Scale | x |

CONFIDENTIAL
Third Angle Projection

REVISION 01
REVISION 01

General Tolerance

Length (mm)	Tolerance(mm)
0 ~ 8	±0.1
8 ~ 25	±0.2
25 ~ 50	±0.3

12. PACKING SPECIFICATION

TBD

REV.: X01   2017/03/30

13. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.
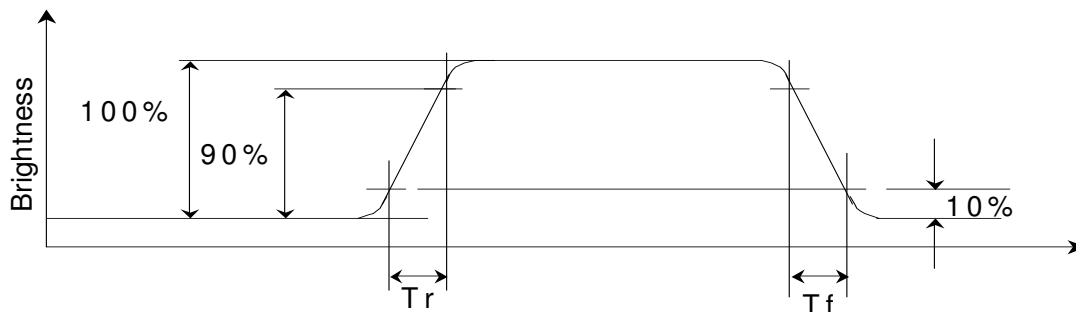
Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.
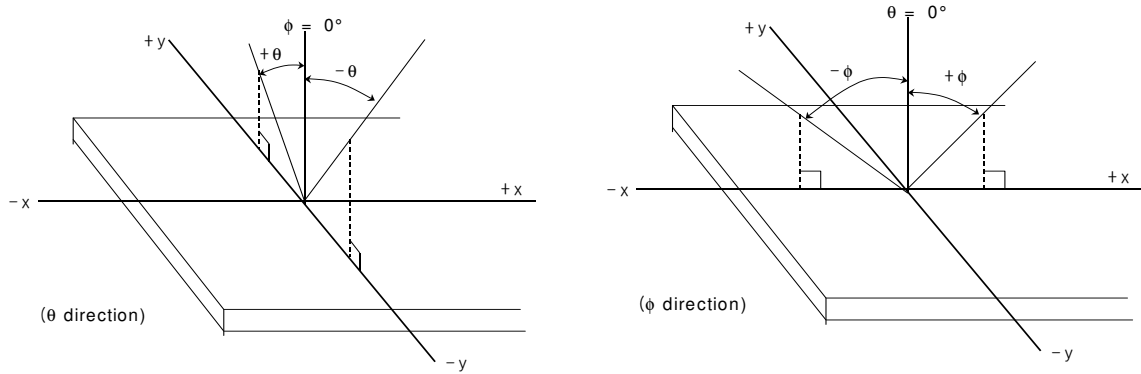
Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-670, MINOLTA CS-100

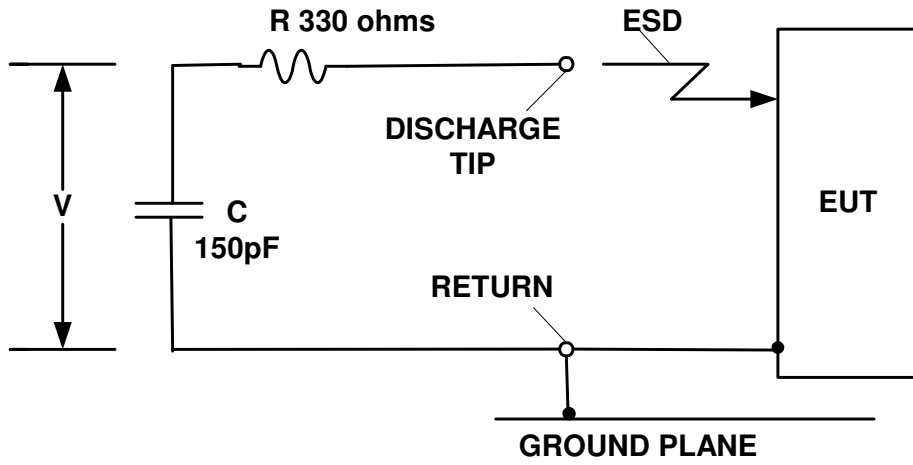**Measurement**
Header

Panel

Plate Form

PR-670 /
MINOLTA CS-100
Color Analyzer
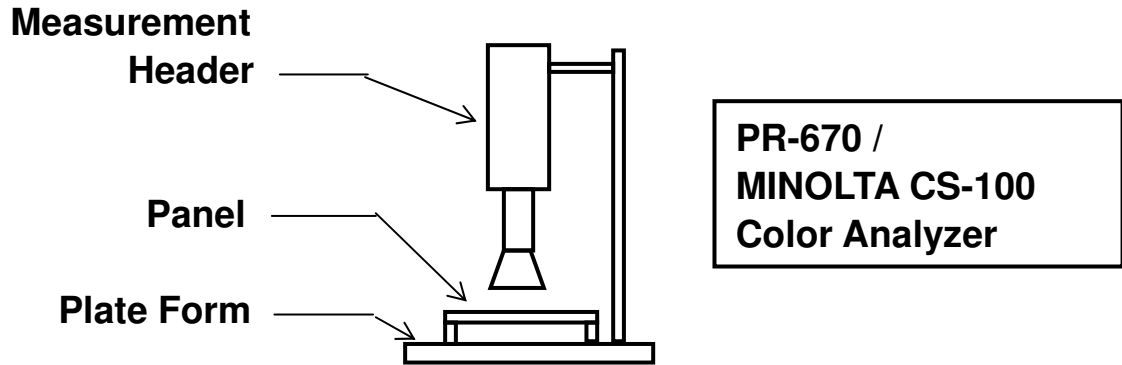
B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510

Measurement
Header

Panel

Plate Form

Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer

REV.: X01   2017/03/30

C. ESD ON AIR DISCHARGE MODE

R 330 ohms   **ESD**

DISCHARGE TIP

V

C 150pF

EUT

RETURN
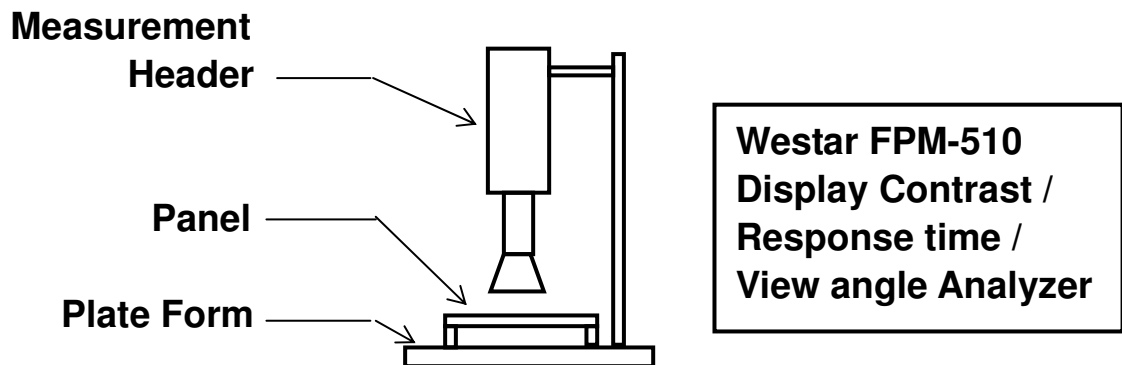
GROUND PLANE

APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

Precautions for Handling

1. When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

2. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.

3. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).
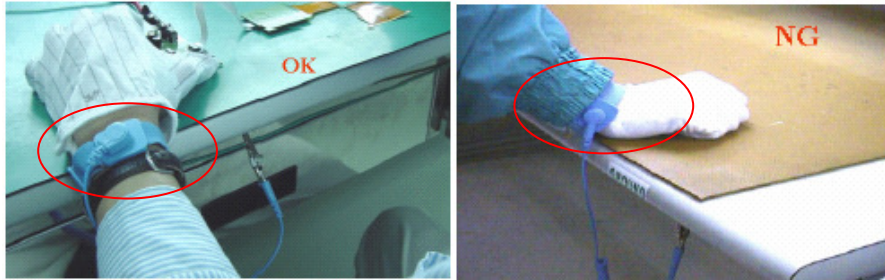
4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.

5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.

6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.

7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.
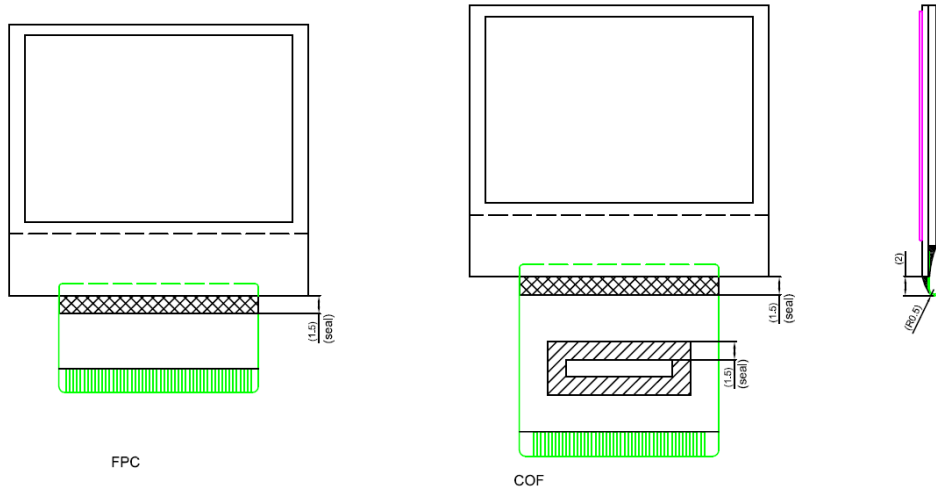
REV.: X01   2017/03/30

8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area >1.5mm; R>0.5mm).
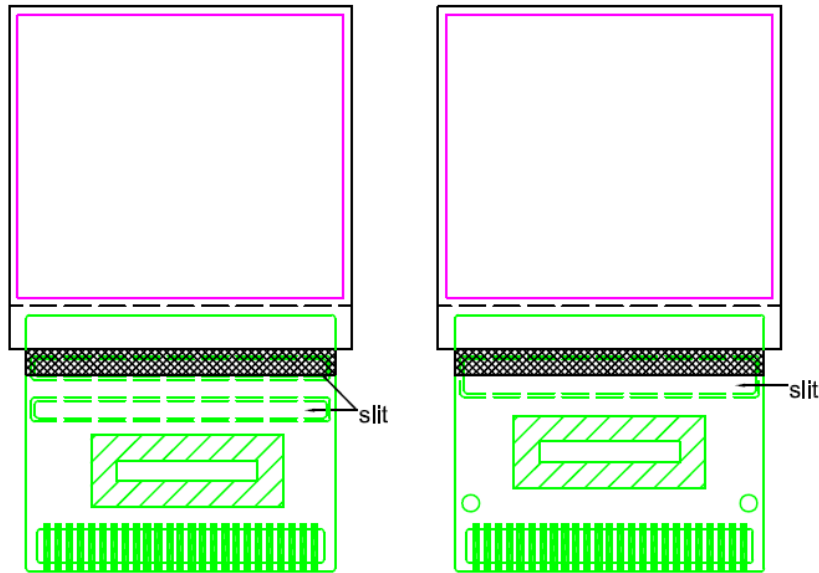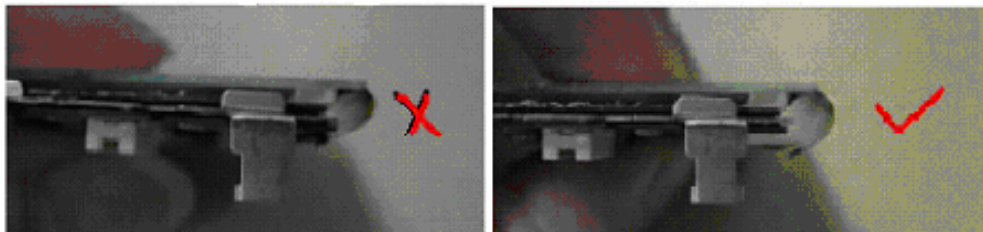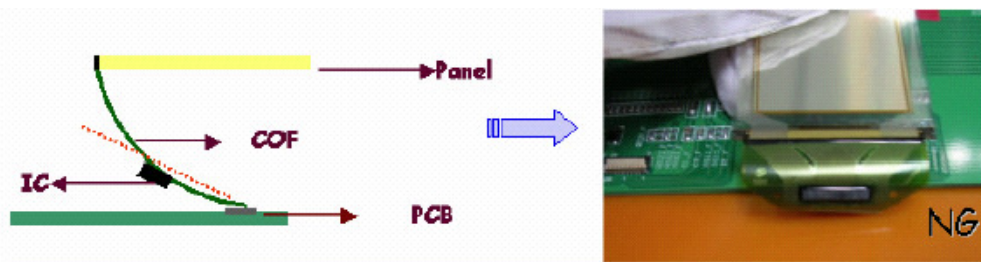
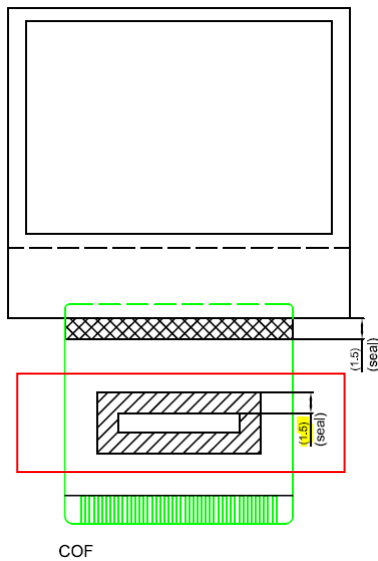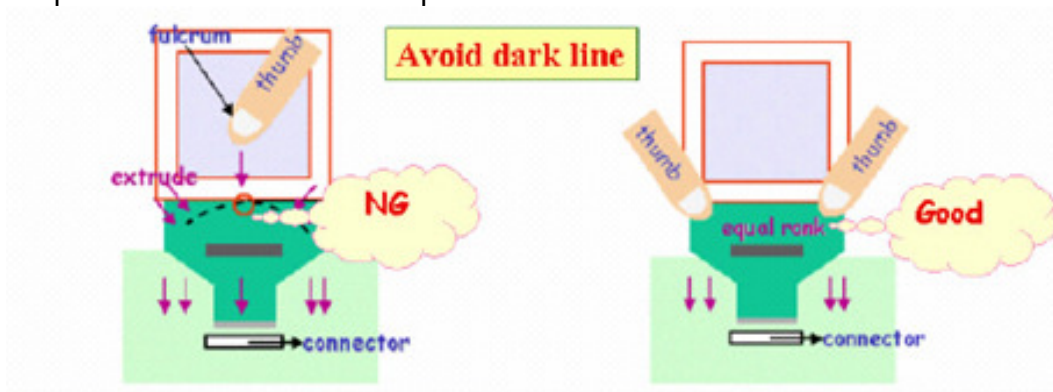9. Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.

COF

10. Use both thumbs to insert COF into the connector when assembling the panel. Please refer to the photo.

11. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.

12. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.

13. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering.

14. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.

15. Use the voltage and current settings listed in the specification to do the function test after the module assembly.

16. Suggestion for soldering process:
    i. TAB Lead- free soldering hot bar process
       1. Use pulse heated bonding tool equipment
       2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature.
       3. Bonding Force:--4kg per centimeter square as the starting point.
       4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.
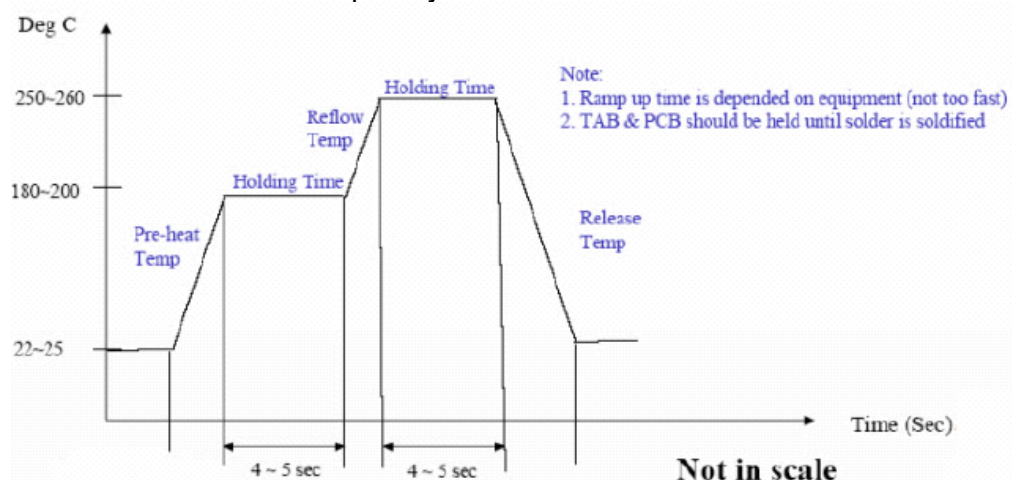
    ii. TAB Lead- free soldering wire process
        In case of manual soldering (Lead- free solder wire)
      1. Solder wire contact iron directly: 280±5℃ at 3-5secs
      2. Solder wire contact TAB lead directly (near iron but not contact): 380±5℃, 3-5secs
      3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.

   iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below 380℃. Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

REV.: X01   2017/03/30

Precautions for Electrical

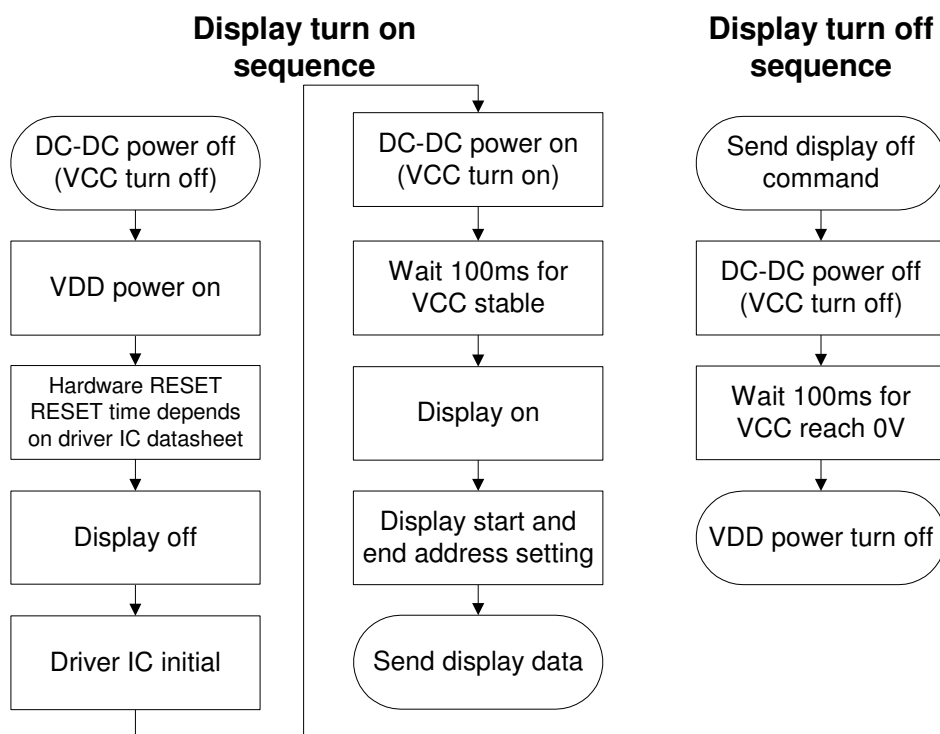## 1. Design using the settings in the specification

It is very important to design and operate the panel using the settings listed in the specification. It includes voltage, current, frame rate and duty cycle... etc. Operation the OLED outside the range of the specification should be entirely avoided to ensure proper operation of the OLED.

2. Maximum Ratings

To ensure the proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.
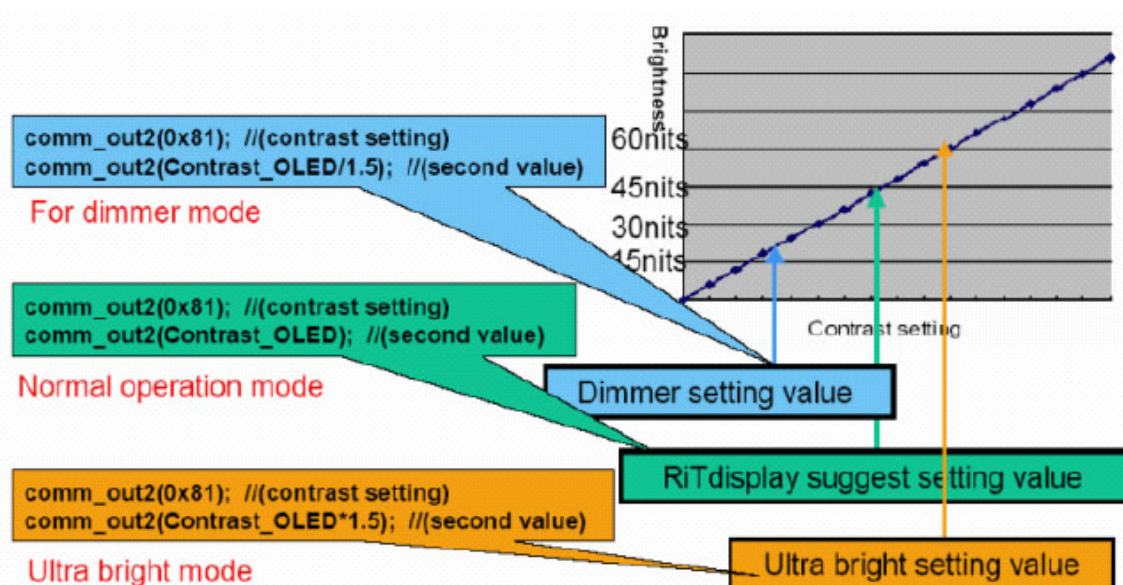
3. Power on/off procedure

To avoid any inadvertent effects resulting from inappropriate power on/off operations, please follow the directions of power on/off procedure on page 6. Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, would cause OLED panel malfunction.

Display turn on sequence

- DC-DC power off (VCC turn off)
- VDD power on
- Hardware RESET RESET time depends on driver IC datasheet
- Display off
- Driver IC initial
- DC-DC power on (VCC turn on)
- Wait 100ms for VCC stable
- Display on
- Display start and end address setting
- Send display data

Display turn off sequence

- Send display off command
- DC-DC power off (VCC turn off)
- Wait 100ms for VCC reach 0V
- VDD power turn off

REV.: X01   2017/03/30

4. Power savings

To save power consumption of the OLED, please use partial display or sleep mode when the panel is not fully activated. Also, if possible, make the black background to save power.

The OLED is a self-luminous device and a particular pixel cluster or image can be lit on via software control. So power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode. The power consumption is almost in directly proportion to the brightness of the panel, and also in directly proportion to the number of pixels lit on the panel. The customer can save the power by the use of black background and sleeping mode. One benefit from using these design schemes is the extension of the OLED lifetime.


```
comm_out2(0x81); //(contrast setting)
comm_out2(Contrast_OLED/1.5); //(second value)
```
For dimmer mode

```
comm_out2(0x81); //(contrast setting)
comm_out2(Contrast_OLED); //(second value)
```
Normal operation mode

```
comm_out2(0x81); //(contrast setting)
comm_out2(Contrast_OLED*1.5); //(second value)
```
Ultra bright mode

Dimmer setting value

RiTdisplay suggest setting value

Ultra bright setting value

5. Adjusting the luminance of the panel

Although there are a couple of ways to adjust the luminance of the panel, it is strongly recommended that the customer change the contrast setting to adjust the luminance of the panel. Adjusting voltages to achieve desired luminance is not allowed. Be aware that the adjustment of luminance would accompany the change of lifetime of the panel and its power consumption as well.

6. Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following four strategies to minimize image sticking.

1. <u>Employ image scrolling or animation</u> to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. <u>Minimize the use of all-pixels-on or full white background</u> in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays.
3. Avoid displaying the characters or menu with high brightness level in a fix position for a long time or repeatedly. If necessary, using the auto fadeout technology.
4. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.

Black Background

Scrolling example

Frame1

Frame2

Frame3

Example: setup and start

```
comm_out2(0x26); // scrolling setup
comm_out2(0x08); // scrolling numbers/step
comm_out2(0x00); // start page
comm_out2(0x00); // scrolling step/frame
comm_out2(0x08); // end page
comm_out2(0x2F); // start
```
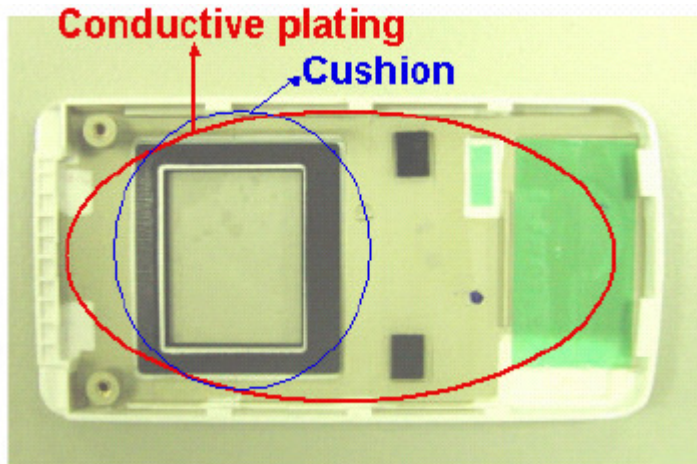
Frame4

Frame5

Example: stop

```
comm_out2(0x2E); //stop
```

Precautions for Mechanical

1. Cushion or Buffer tape on the cover glass

It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.

It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

2. Avoid excessive bending of film when handling or designing the panel into the product

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.

Precautions for Storage and Reliability Test

1. Storage

Store the packed cartons or packages at 25°C±5°C, 55%±10%RH. Do not store the OLED module under direct sunlight or UV light. For best panel performance, unpack the cartons and start the production of the panels within six months after the reception of them.

2. Reliability Test

RiTdisplay only guarantees the reliability of the OLEDs under the test conditions and durations listed in the specification.

REV.: X01   2017/03/30