Specification for Approval

PRODUCT NAME: RGS18160128FH007
PRODUCT NO.: 9916807000

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2007. 10. 09	
A01	■ Transfer from X version ■ Modify CIE specification	2007. 12. 03	Page 8
A02	■ Modify power off sequence ■ Rename IC (SSD1353U4→ SSD1353U7) ■ Modify single tape	2008. 05. 23	Page 14 & 17
A03	■ Modify polarizer	2008. 09. 17	Page 4, 5 & 17
A04	■ Modify definition of panel thickness ■ Modify packing specification	2009. 03. 11	Page 5 & 18
A05	■ Modify polarizer ■ Add appendixes of ROHS test report	2009. 07. 20	Page 4, 5, 6, 8, 17 & 24~31
A06	■ Add appendix of precautions for using the OLED module	2014. 03. 31	Page 23~32

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : 262 K color and 65K colors
- Panel resolution : 160*128
- Driver IC : SSD1353
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design. : 2.01 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8/9/16/18-bits 6800/8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70℃
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	160 x 3x 128	dot
2	Dot Size	0.048 (W) x 0.199 (H)	mm^2
3	Dot Pitch	0.073 (W) x 0.219 (H)	mm^2
4	Aperture Rate	60	%
5	Active Area	35.015 (W) x 28.012 (H)	mm^2
6	Panel Size	42.7 (W) x 33.4 (H)	mm^2
7*	Panel Thickness	1.82 ± 0.1	mm
8	Module Size	42.7 (W) x 47.5 (H) x 2.01 (T)	mm^3
9	Diagonal A/A size	1.8	inch
10	Module Weight	5.92 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	-0.5	3.5	V	Ta = 25℃	IC maximum rating
Supply Voltage (Vcc)	10	21	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃		
Storage Temp	-40	85	℃		
Humidity		85	%		
Life Time	12,000	-	Hrs	80 cd/m^2, 50% checkerboard	Note (1)
Life Time	16,000	-	Hrs	60 cd/m^2, 50% checkerboard	Note (2)

Note:

(A) Under Vcc = 17V, Ta = 25℃, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 80 cd/m^2 :

- Master contrast setting : 0x0f
- Frame rate : 85Hz
- Duty setting : 1/128

(2) Setting of 60 cd/m^2 :

- Master contrast setting : 0x0b
- Frame rate : 85Hz
- Duty setting : 1/128

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)		16.5	17	17.5	V
V_{CI}	Low voltage power supply (for driver IC)		2.4	2.8	3.5	V
V_{DDIO}	Logic I/O operating voltage		1.6	1.8	V_{CI}	V
V_{OH}	High logic output level	Iout=100uA	0.9*V_{DDIO}		V_{DDIO}	V
V_{OL}	Low logic output level	Iout=100uA	0		0.1*V_{DDIO}	V
V_{IH}	High logic input level	Iout=100uA	0.8*V_{DDIO}		V_{DDIO}	V
V_{IL}	Low logic input level	Iout=100uA	0		0.2*V_{DDIO}	V
I_{CC}	Operating current for V_{CC} (No panel attached)	Contrast=FF		8.9	10	mA
I_{CI}	Operating current for V_{CI} (No panel attached)	Contrast=FF		890	980	uA
I_{SEG}	Segment output current (No panel attached)	Contrast=FF		160	175	uA
		Contrast=7F		80		uA

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current	-	39	41	mA	All pixels on (1)
Standby mode current	-	3	5	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	663	697	mW	All pixels on (1)
Standby mode power consumption	-	51	85	mW	Standby mode 10% pixels on (2)
Pixel Luminance	60	80		cd/m^2	Display Average
Standby Luminance		20		cd/m^2	
CIEx (White)	0.27	0.31	0.35		CIE1931
CIEy (White)	0.29	0.33	0.37		CIE1931
CIEx (Red)	0.62	0.66	0.70		CIE1931
CIEy (Red)	0.29	0.33	0.37		CIE1931
CIEx (Green)	0.26	0.30	0.34		CIE1931
CIEy (Green)	0.59	0.63	0.67		CIE1931
CIEx (Blue)	0.10	0.14	0.18		CIE1931
CIEy (Blue)	0.14	0.18	0.22		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

Normal mode condition :

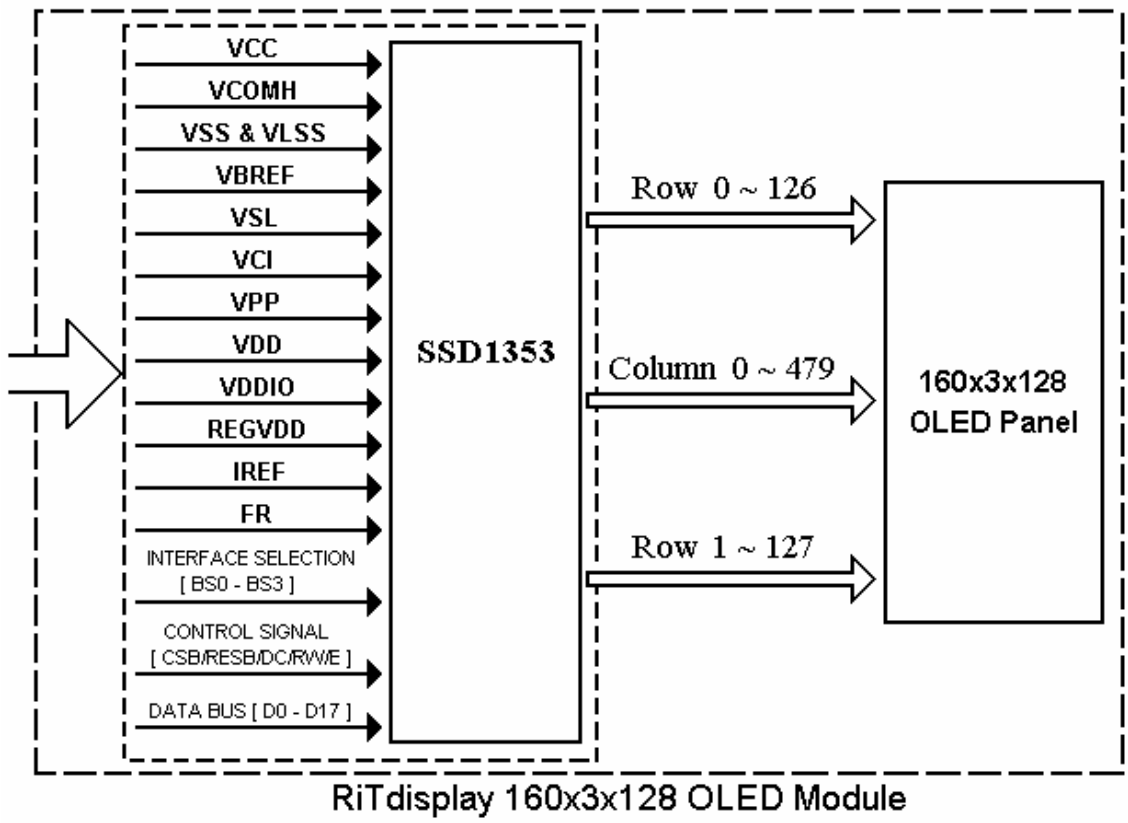
- Driving Voltage : 17V
- Contrast setting : 0x0f
- Frame rate : 85Hz
- Duty setting : 1/128

Standby mode condition :

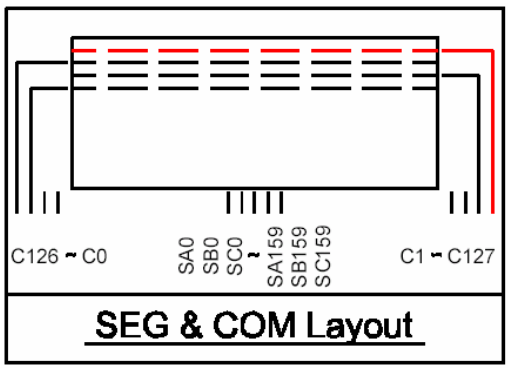
- Driving Voltage : 17V
- Contrast setting : 0x05
- Frame rate : 85Hz
- Duty setting : 1/128

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NO	PIN NAME	DESCRIPTION
1	VCC	Power supply for panel driving voltage.
2	VCOMH	A capacitor should be connected between this pin and VSS.
3	VLSS	Analog system ground pin.
4	VSS	Ground pin.
5	VBREF	Connect to ground with a capacitor.
6	VSL	This is segment voltage reference pin.
7	VCI	Low voltage power supply.
8	VPP	Connect to VDD.
9	VDD	Power supply input for logic.
10	VDDIO	Power supply for interface logic level.It should be match with the MCU interface voltage level. VDDIO must always be equal or lower than VCI.
11.	REGVDD	Internal VDD regulator selection pin. When this pin is pulled high,internal VDD regulator is enabled. When this pin is pulled low,external VDD regulator is used.
12	BS0	Interface selection pins.
13	BS1	
14	BS2	
15	BS3	
16	FR	It should be kept NC.
17	CSB	This pad is the chip select input. Low active.
18	RESB	This is a reset signal input. Low active.
19	DC	D/C=”H”: Data. D/C=”L”: Command.
20	RW	When connected to 8080-series MPU. WR pin. When RW =”L”: Write signal input. When connected to 6800-series MPU. When RW =”H”: Read. When RW =”L”: Write.
21	E	When connected to 8080-series MPU. RD pin. When E =”L”: Read signal input. When connected to 6800-series MPU. Enable clock input of the 6800 series MPU.
22	D0	18 bit / 16bit / 9bit / 8 bit Data bus I/O.
23	D1	
24	D2	
25	D3	
26	D4	
27	D5	
28	D6	
29	D7	
30	D8	

31	D9	
32	D10	
33	D11	
34	D12	
35	D13	
36	D14	
37	D15	
38	D16	
39	D17	
40	IREF	A resistor should be connected between this pin and VSS.
41	VSS	Ground pin.
42	VLSS	Analog system ground pin.
43	VCOMH	A capacitor should be connected between this pin and VSS.
44	VCC	Power supply for panel driving voltage.
45	NC	No connection.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 160x132x18bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

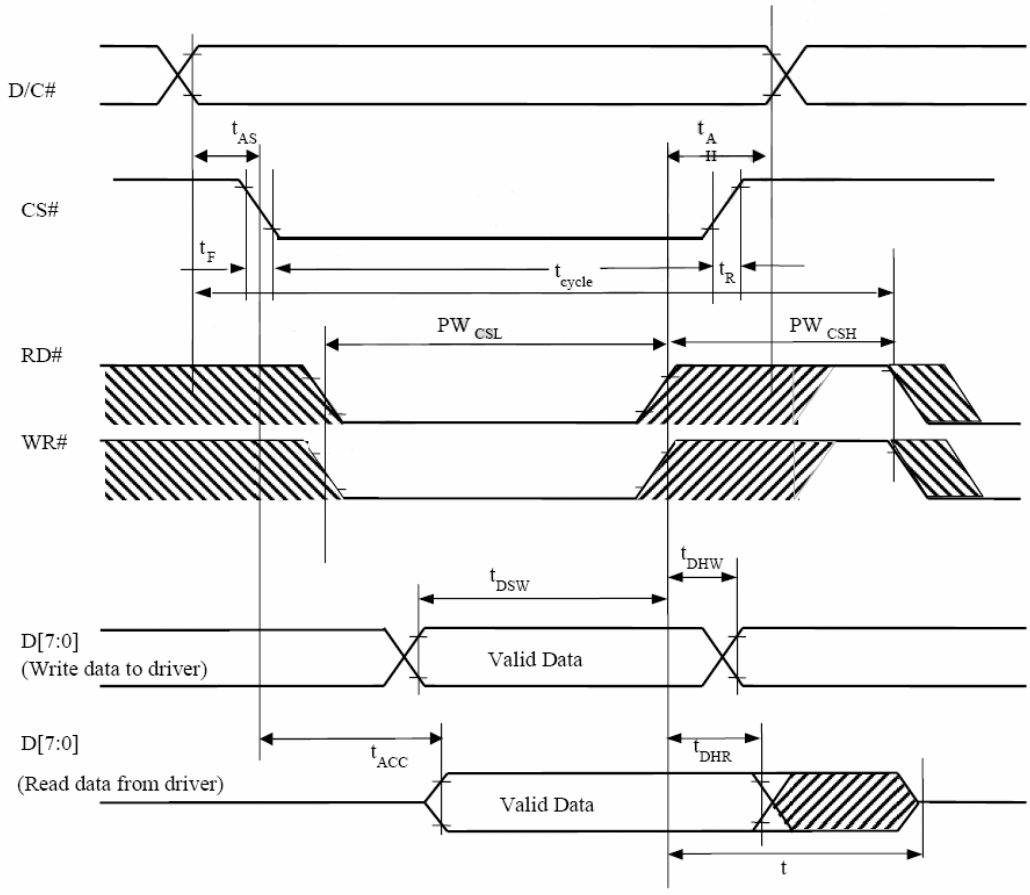
Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0	Common output
Normal	Remapped														
0	131	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM0
1	130	6	6	6					.....	.....					COM1
2	129								.....	.....					COM2
3	128								.....	.....					COM3
4	127								.....	.....					COM4
5	126								.....	.....					COM5
6	125			no of bits in this cell					.....	.....					COM6
7	124								.....	.....					COM7
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
127	4								.....	.....					
128	3								.....	.....					COM128
129	2								.....	.....					COM129
130	1								.....	.....					COM130
131	0								.....	.....					COM131

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC158	SA159	SB159	SA159

7.5 INTERFACE TIMING CHART

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080-series MPU parallel interface characteristics

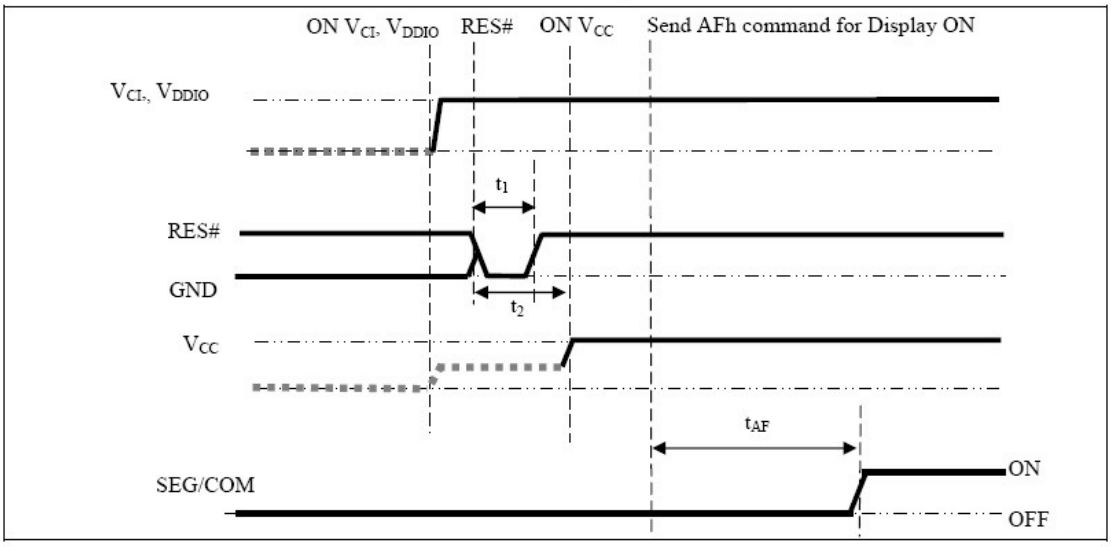
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

Power ON sequence:

1. Power ON V_{CI}, V_{DDIO}.
2. After V_{CI}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 100us (t_1) and then HIGH(logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

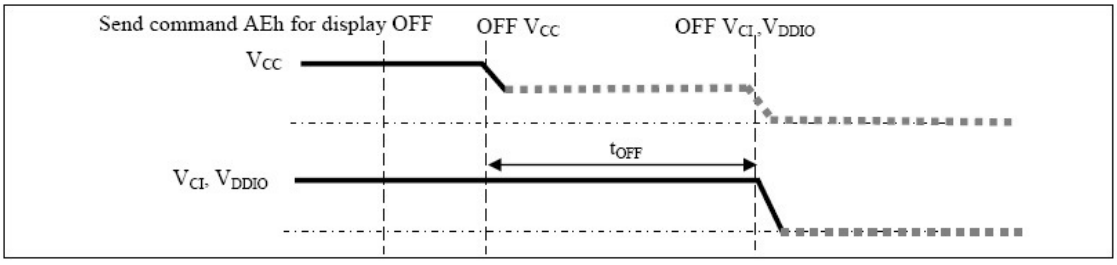
The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.(1), (2)
3. Wait for t_{OFF}. Power OFF V_{CI},, V_{DDIO}.
   (Where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)

The Power OFF sequence

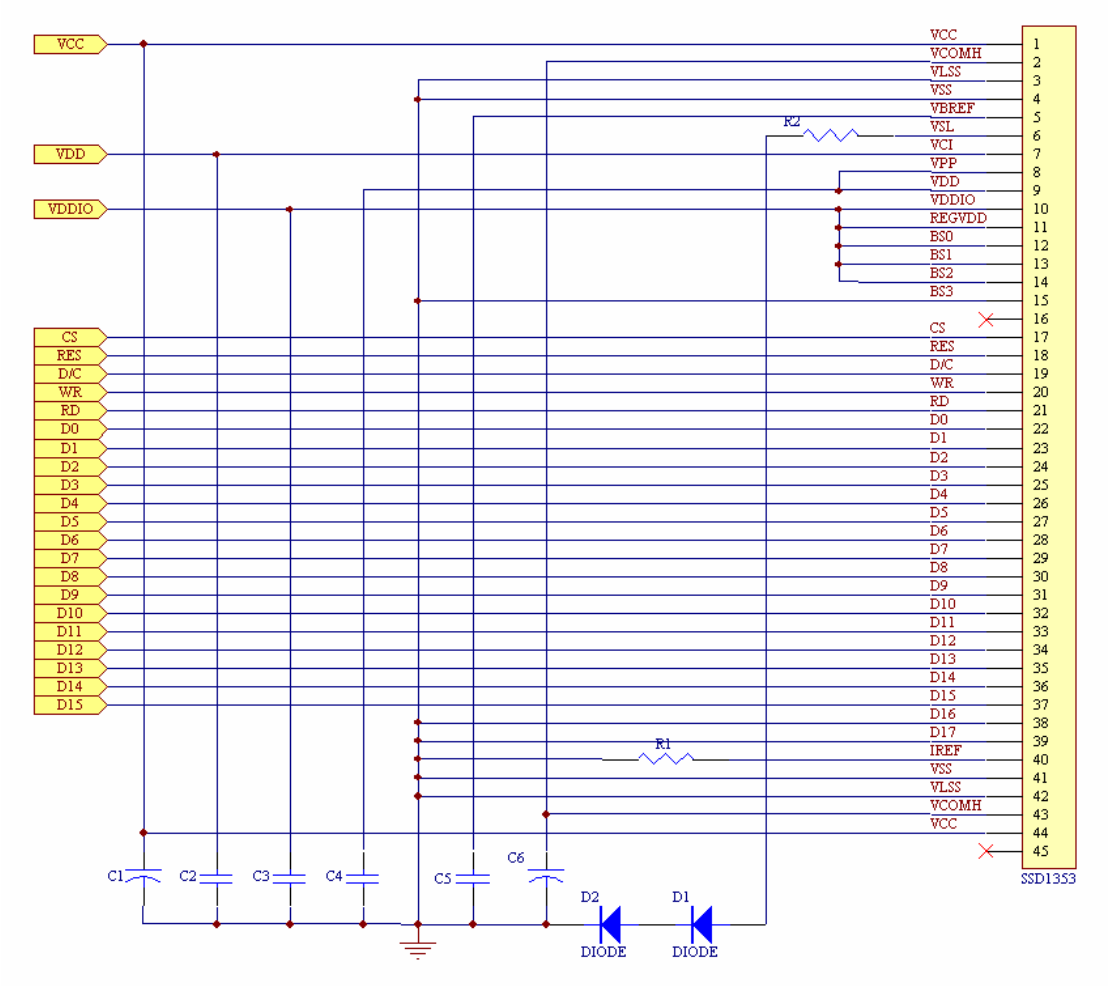


Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI},V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

8.2 APPLICATION CIRCUIT



Component:

C1, C6 : 4.7 uF/25 ~ 35V **Tantalum type capacitor.**

C2, C3, C4 : 1uF/ 16V

C5 : 0.1uF/ 16V

R1: 1.2M ohm 1%

R2: 50ohm 1/4W

D1 and D2: RB480K (ROHM)

This circuit is for 8080 16bits interface.

8.3 COMMAND TABLE

Refer to IC Spec : SSD1353

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 96hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

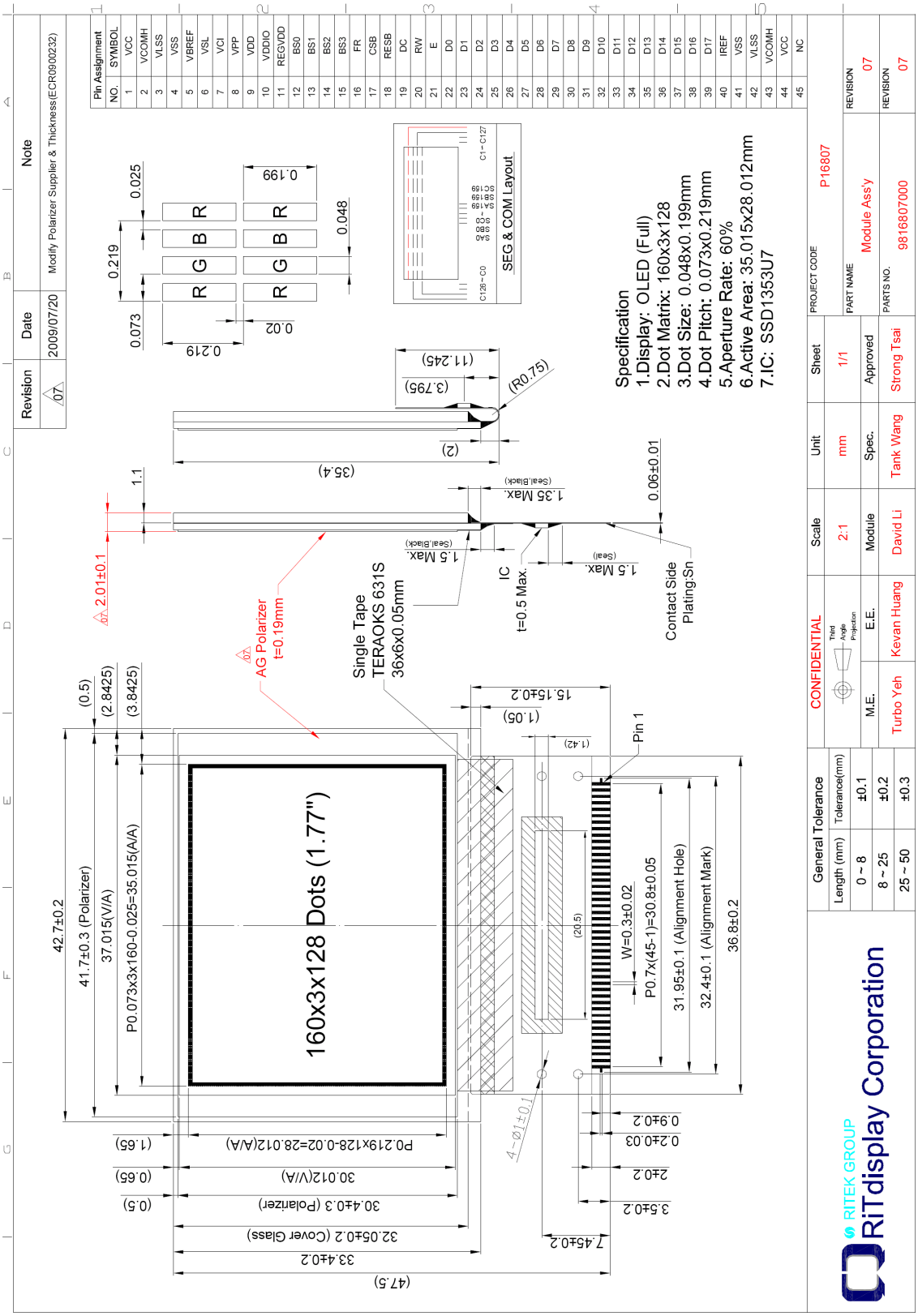
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

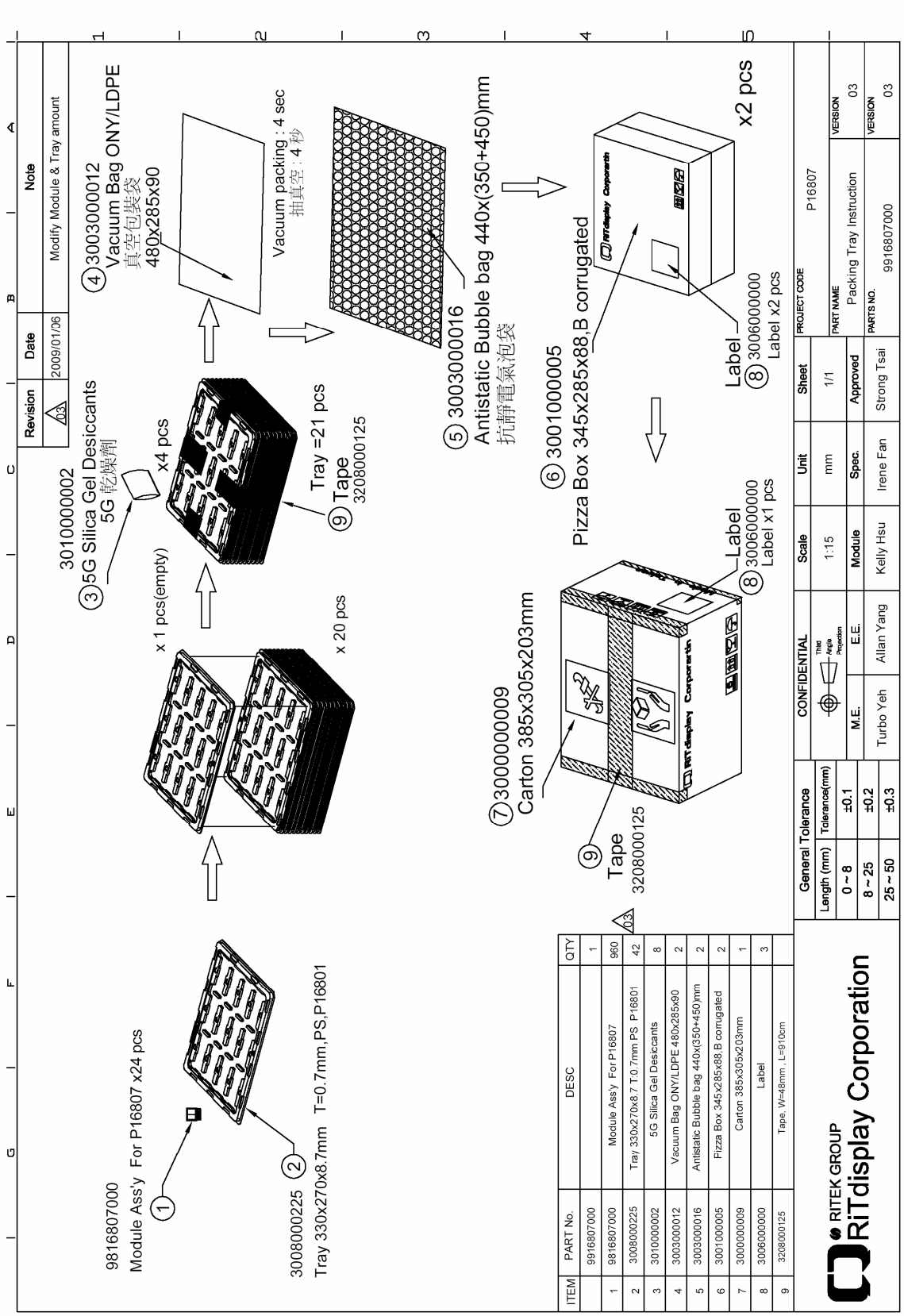
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

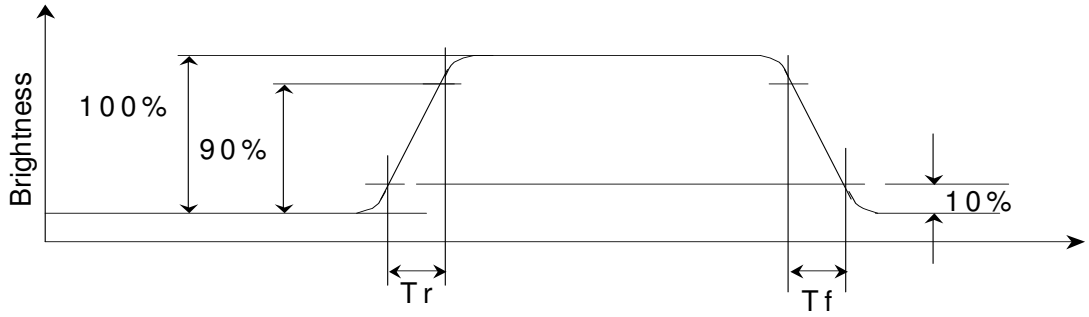
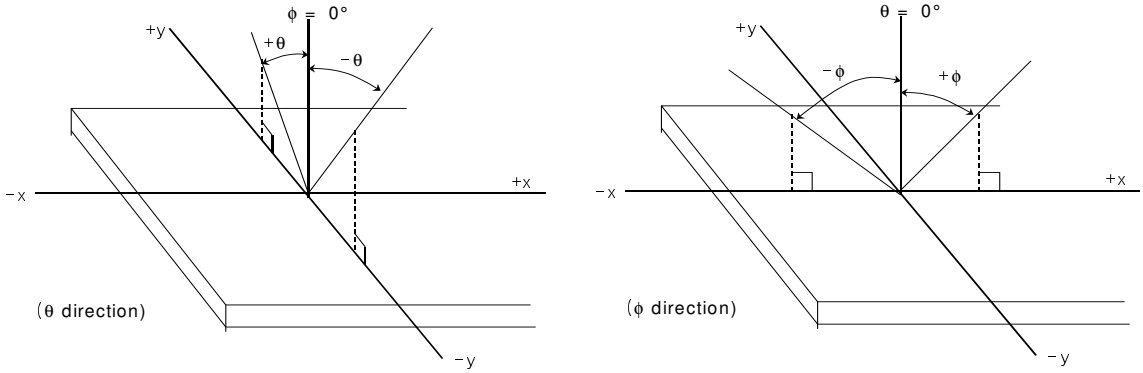


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.



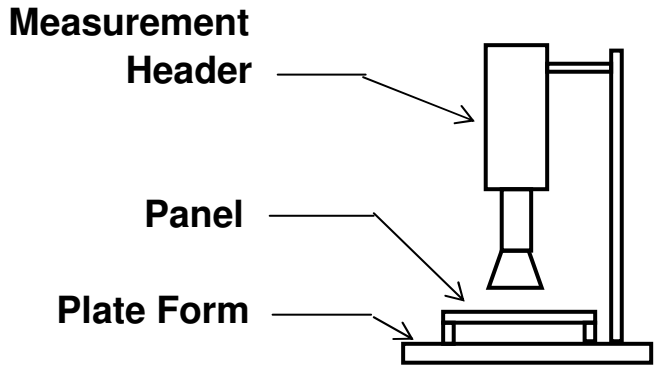
Vertical angles **Horizontal angles**

Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

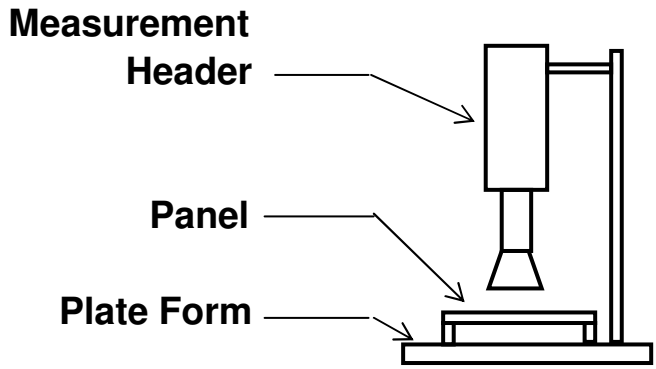
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

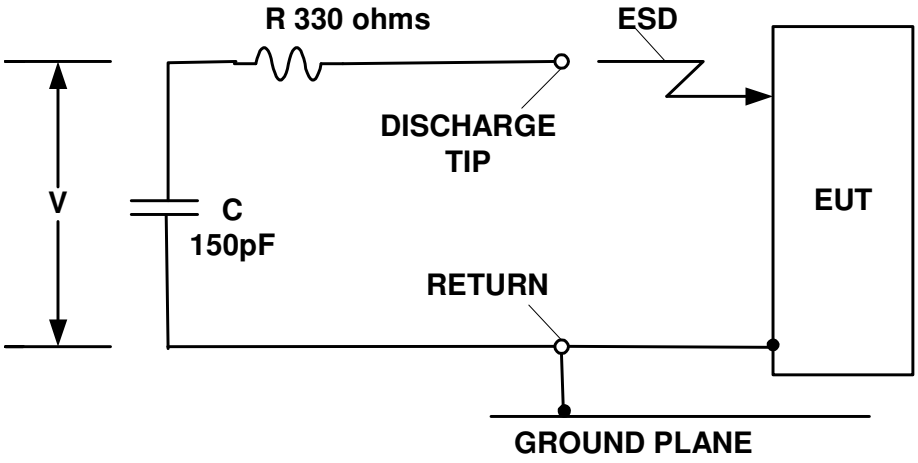
B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



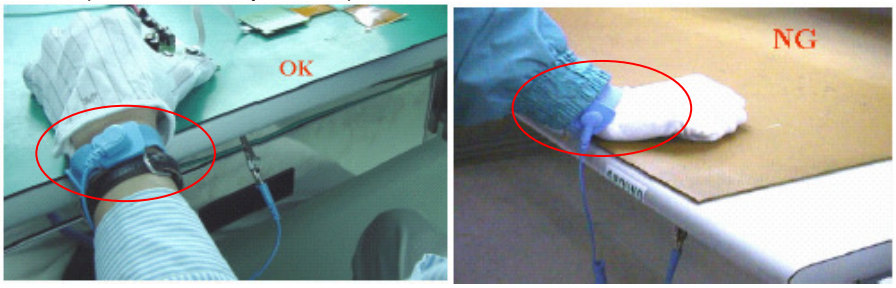
APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

Precautions for Handling

1. When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

2. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.

3. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).



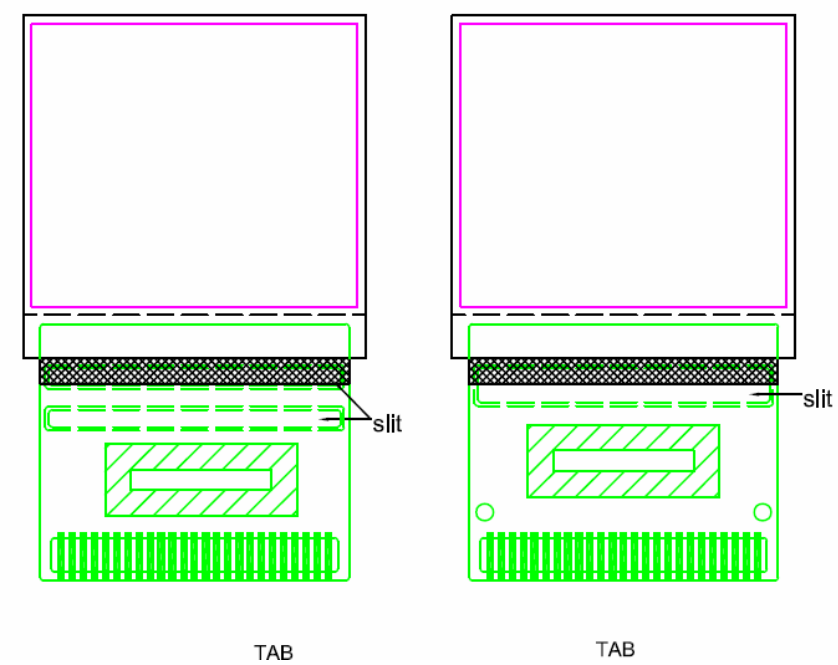
4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.

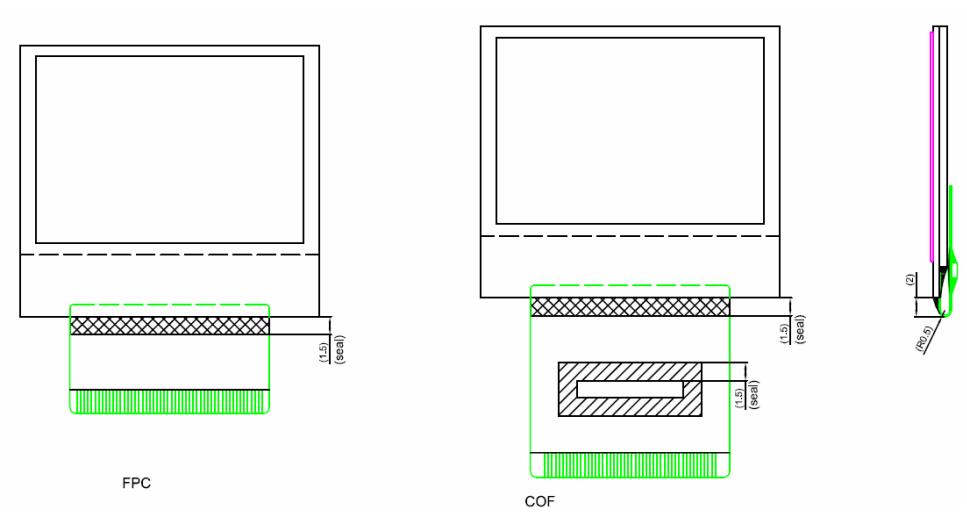
5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.

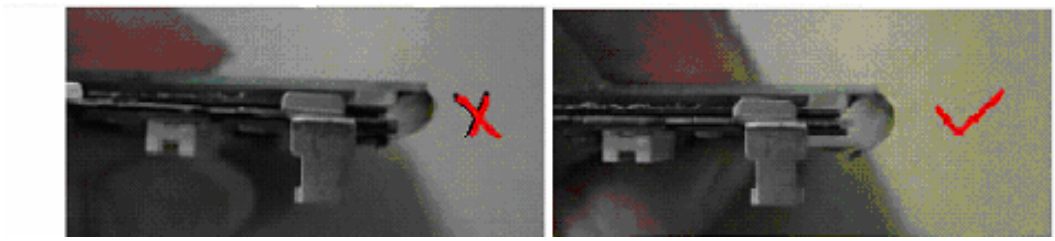
6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.

7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.

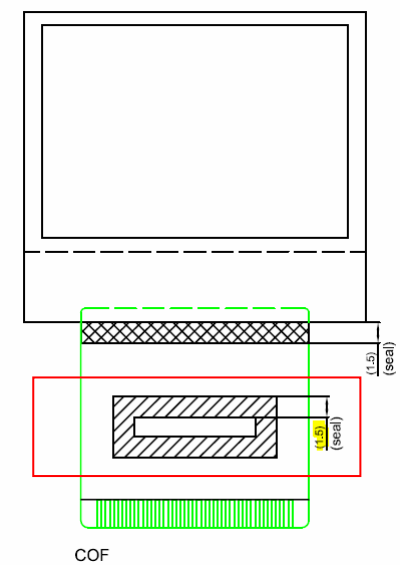
8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area >1.5mm; R>0.5mm).

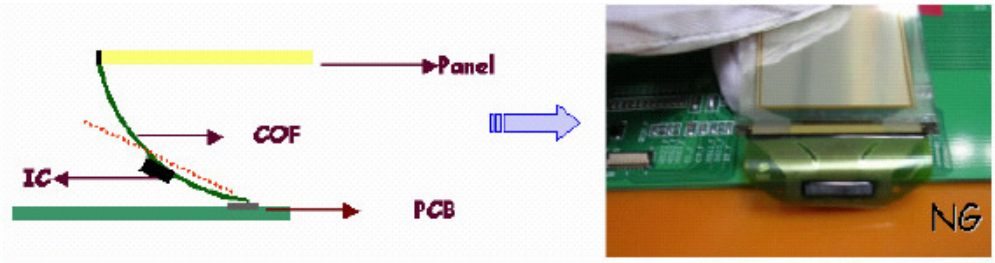




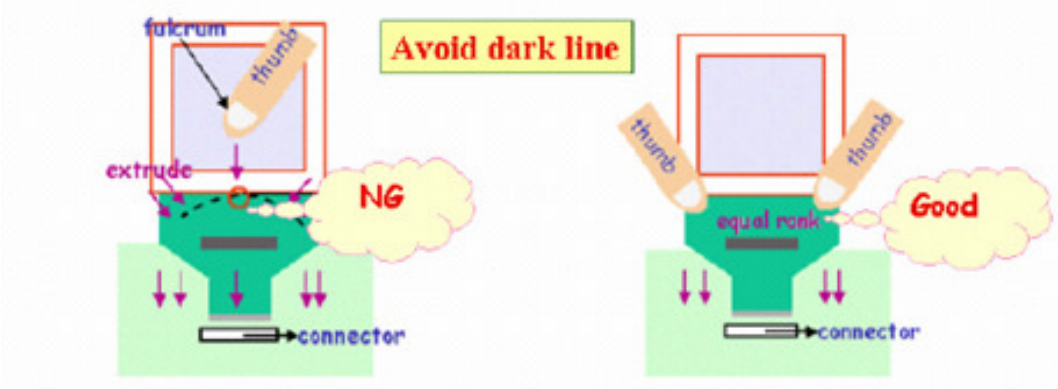


9. Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.





10. Use both thumbs to insert COF into the connector when assembling the panel. Please refer to the photo.



11. The working area for the panel should be kept clean. If the panel is accidentally dropped on the floor, do visual inspection of the panel first. Please use clean-room wiping cloth moistened with alcohol to wipe it off if dirt or grease stains the panel.

12. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.

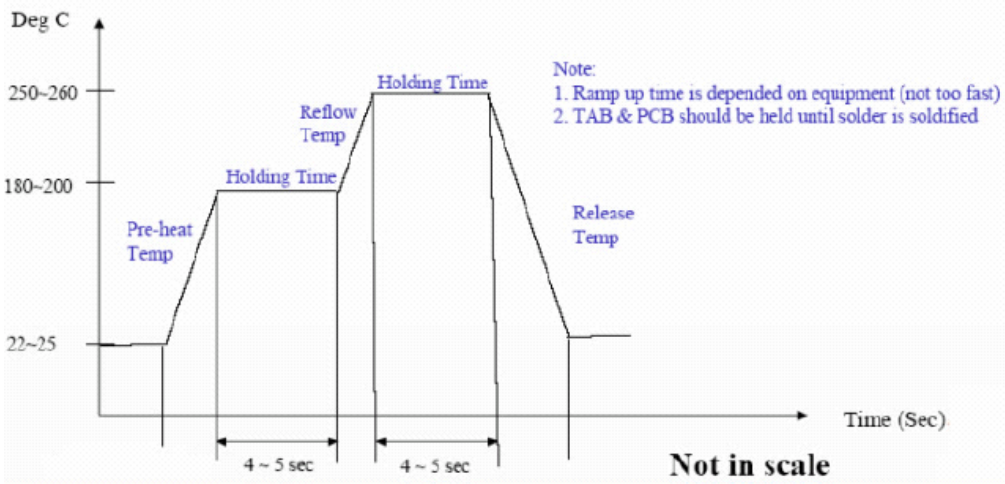
13. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.

14. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering.

15. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.

16. Use the voltage and current settings listed in the specification to do the function test after the module assembly.

17. Suggestion for soldering process:
    i. TAB Lead- free soldering hot bar process
        1. Use pulse heated bonding tool equipment
        2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature.
        3. Bonding Force:--4kg per centimeter square as the starting point.
        4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.



ii. TAB Lead- free soldering wire process
In case of manual soldering (Lead- free solder wire)
1. Solder wire contact iron directly: 280±5℃ at 3-5secs
2. Solder wire contact TAB lead directly (near iron but not contact): 380±5 ℃, 3-5secs
3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.

iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below 380 ℃. Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

Precautions for Electrical

1. Design using the settings in the specification

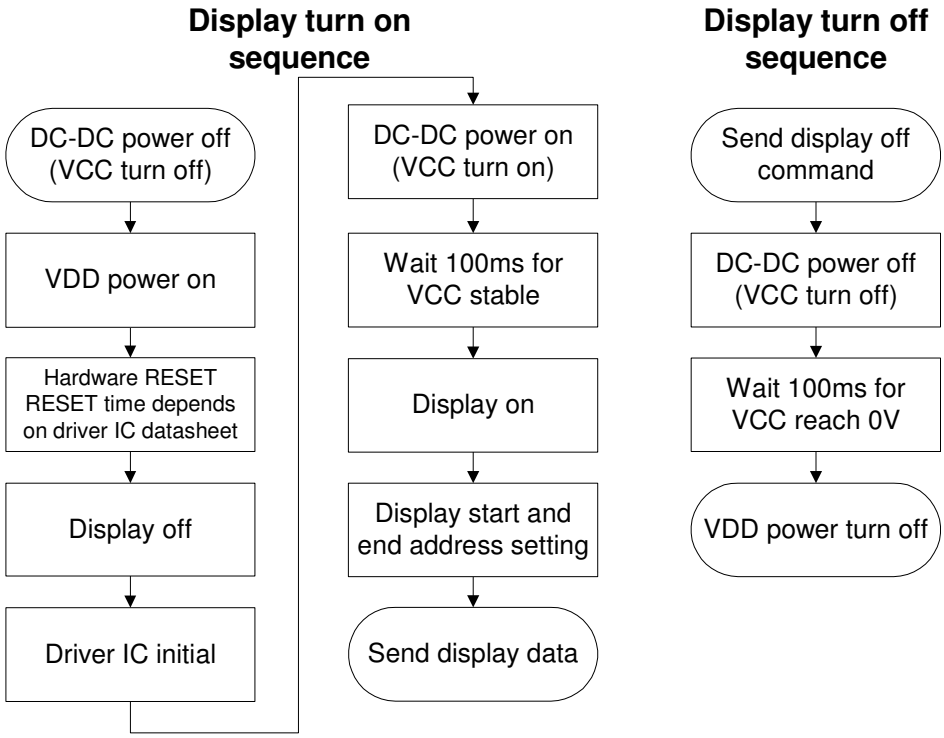
It is very important to design and operate the panel using the settings listed in the specification. It includes voltage, current, frame rate and duty cycle... etc. Operation the OLED outside the range of the specification should be entirely avoided to ensure proper operation of the OLED.

2. Maximum Ratings

To ensure the proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

3. Power on/off procedure

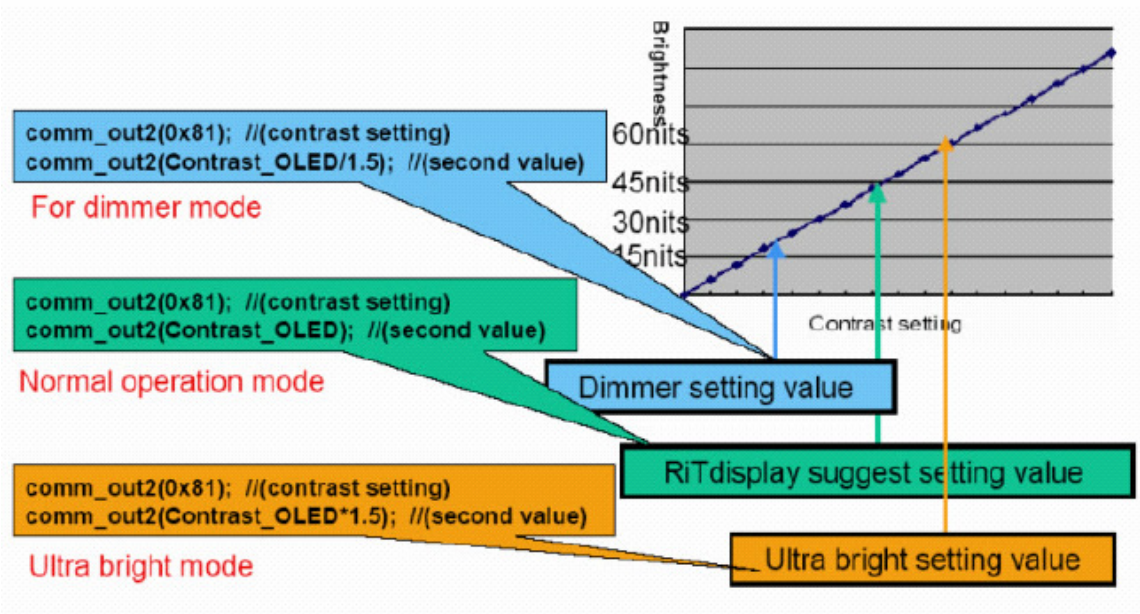
To avoid any inadvertent effects resulting from inappropriate power on/off operations, please follow the directions of power on/off procedure on page 6. Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, would cause OLED panel malfunction.



4. Power savings

To save power consumption of the OLED, please use partial display or sleep mode when the panel is not fully activated. Also, if possible, make the black background to save power.

The OLED is a self-luminous device and a particular pixel cluster or image can be lit on via software control. So power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode. The power consumption is almost in directly proportion to the brightness of the panel, and also in directly proportion to the number of pixels lit on the panel. The customer can save the power by the use of black background and sleeping mode. One benefit from using these design schemes is the extension of the OLED lifetime.



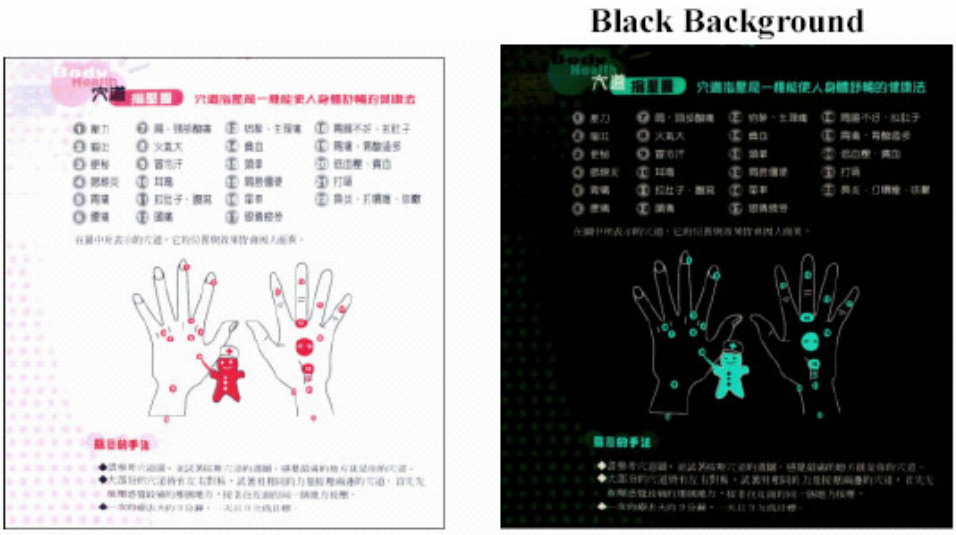
5. Adjusting the luminance of the panel

Although there are a couple of ways to adjust the luminance of the panel, it is strongly recommended that the customer change the contrast setting to adjust the luminance of the panel. Adjusting voltages to achieve desired luminance is not allowed. Be aware that the adjustment of luminance would accompany the change of lifetime of the panel and its power consumption as well.

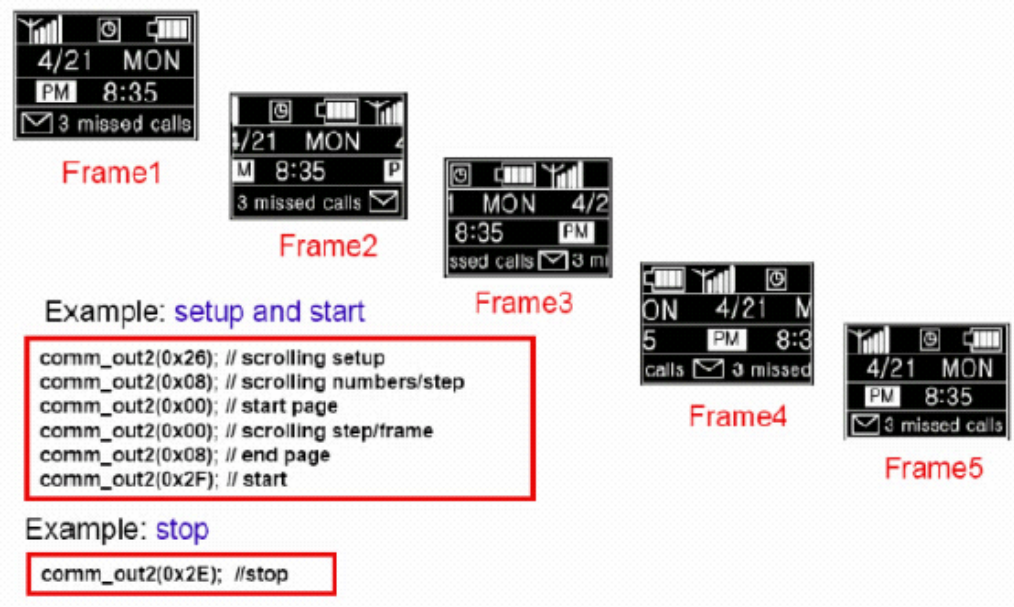
6. Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking.

1. Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays
3. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.



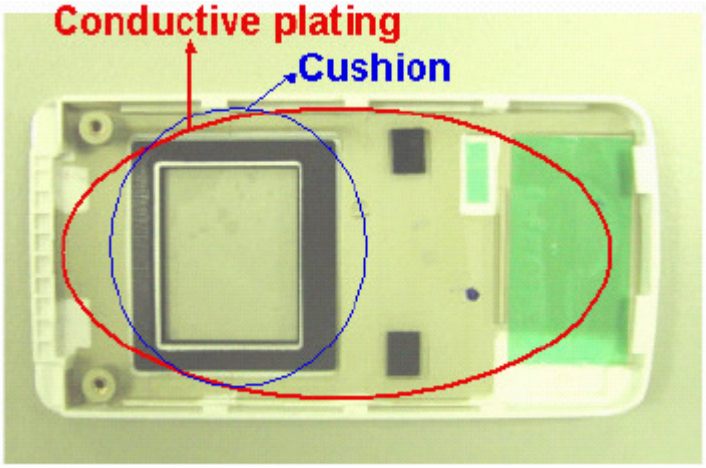
Scrolling example



Precautions for Mechanical

1. Cushion or Buffer tape on the cover glass

It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.



It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

2. Avoid excessive bending of film when handling or designing the panel into the product

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.

Precautions for Storage and Reliability Test

1. Storage

Store the packed cartons or packages at 25℃±5℃, 55%±10%RH. Do not store the OLED module under direct sunlight or UV light. For best panel performance, unpack the cartons and start the production of the panels within six months after the reception of them.

2. Reliability Test

RiTdisplay only guarantees the reliability of the OLEDs under the test conditions and durations listed in the specification.

APPENDIX 4: ROHS TEST REPORT

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TEST REPORT

NO.: A002R12052305-46R01 Date: May. 28, 2012 Page 1 of 8

Customer: Kunshan Hutek Corporation Co.,Ltd
客户/申请商: 昆山沪铼光电科技有限公司
Address: 88, Second Avenue, Kunshan Export Processing Zone, Jiangsu Province, China
地　　址: 江苏省昆山市综合保税区第二大道 88 号
Report on the submitted sample said to be
委托检验的样品及申请者对样品的说明如下
Sample name: OLED
样品名称: OLED
Supplier: Hutek
供 应 商: 滸鉢
Manufacturer: Hutek
制造商: 滸鉢
Sample received date: May. 23, 2012
样品接收日期: 2012-05-23

Testing Requested/ 测 试 要 求:

1）As specified by client, to determine the Lead, Cadmium, Mercury, Hexavalent Chromium, PBB & PBDE content in the submitted sample in accordance with Directive 2002/95/EC (RoHS).
依照欧盟 RoHS 指令 2002/95/EC，测定委托样品中铅、镉、汞、六价铬、多溴联苯（PBBs）和多溴联苯醚（PBDEs）的含量。
2）As specified by client, to determine the Fluorine, Chlorine, Bromine and Iodine content in the submitted sample.
依据客户要求，测定委托样品中氟，氯，溴，碘的含量。
3) As specified by client, to determine PFOS content in the submitted samples in accordance with Directive (EU) No 757/2010.
依照(EU) No 757/2010 指令，测定委托样品中的全氟辛烷磺酸（PFOS）的含量。

Results/ 结果:

Please refer to the next pages.
见下页。

******FOR FURTHER DETAILS, PLEASE REFER TO THE FOLLOWING PAGE(S)******
******更多详细信息请查阅下页******

Signed for and on behalf of
Shenzhen AOV Testing Technology Co., Ltd, Kunshan Branch

Project Leader: Maggie	Reviewed by: Weikin	Approved by: Mickey
Li Tingting, Maggie	Wang Wexin, Weikin	Yuan Qi, Mickey
Chemical Test Director	Technical Director	Lab Manager

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中国江苏省昆山市综合保税区第二大道88号厂房
电话号码：86-512-5510 8000 公司网址：www.aovt.com
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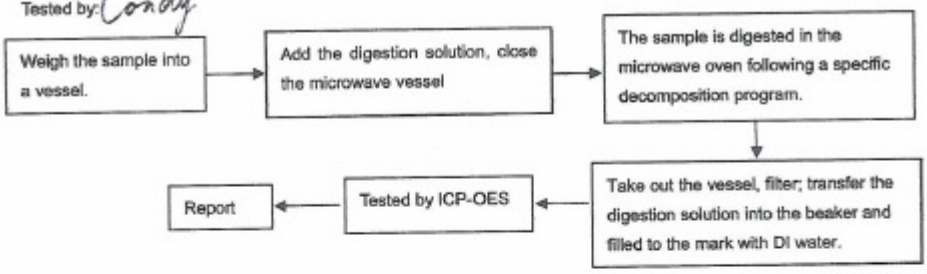
Testing method/ 测 试 方 法:

Testing Item/测试项目	Pretreatment method / 前处理方法	Measuring instrument / 测试仪器	MQL
Lead (Pb)/铅 (Pb)	IEC 62321: 2008, section 8/ IEC 62321: 2008, 第 8 部分	ICP-OES	2 mg/kg
Cadmium (Cd)/镉 (Cd)	IEC 62321: 2008, section 8/ IEC 62321: 2008, 第 8 部分	ICP-OES	2 mg/kg
Mercury (Hg)/汞 (Hg)	IEC 62321: 2008, section 7/ IEC 62321: 2008, 第 7 部分	ICP-OES	2 mg/kg
Chromium (Cr VI)/六价铬 (Cr^{6+})	IEC 62321:2008, Annex C / IEC 62321: 2008, 附件 C	UV-VIS	2 mg/kg
PBBs/ PBDEs /多溴联苯（PBBs）及多溴联苯醚（PBDEs）	IEC 62321: 2008, Annex A / IEC 62321: 2008, 附件 A	GC-MS	5 mg/kg
Fluorine/ Chlorine/ Bromine/ Iodine /氟(F)/ 氯(Cl)/ 溴(Br)/ 碘(I)	BS EN 14582：2007	IC	50 mg/kg
PFOS	US EPA 3540C:1996	LC-MS	10 mg/kg

Test Flow/检测流程:

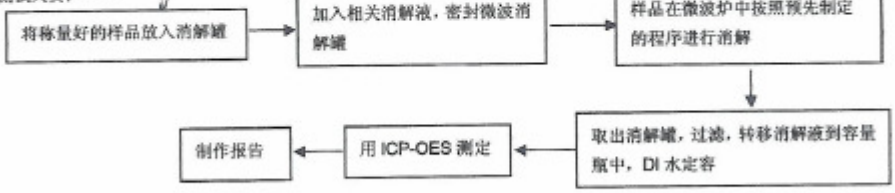
1. To Determine Lead, Cadmium Content:

Tested by: Condy



测定铅，镉含量

测试人员：Condy



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2. To Determine Mercury Content:

Tested by: Condy

Weigh the sample into a vessel. → Add the digestion solution, close the microwave vessel. → The sample is digested in the microwave oven following a specific decomposition program. → Cooling the vessel, filter; washed and filled to the mark with DI water. → Tested by ICP-OES → Report

测定汞含量

测试人员: Condy

将称量好的样品放入消解罐中 → 加入相关消解液，密封微波消解罐 → 样品在微波炉中按照预先制定的程序进行消解 → 取出消解罐，过滤，转移消解液到容量瓶中，DI 水定容 → 用 ICP-OES 测定 → 制作报告

3. To Determine Hexavalent Chromium Content (for Polymer):

Tested by: Danal

Weigh the sample; add the digestion solution. → Stir 3 hours while heating the samples continuously to 90-95 °C, Gradually cool each solution to room temperature → Filter; adjust the pH of the solution and filled to the mark with DI water. → Add the diphenylcarbazide solution and adjust the pH to acidic. → Transfer a portion of the solution to absorption cell, measure the absorbance with UV-VIS. → Report

测定六价铬含量(聚合物中)

测试人员: Danal

将称量好的样品放入锥形瓶中，加入消解剂 → 在 90-95 °C 中持续加热搅拌 3 个小时，冷却至室温 → 过滤，调整溶液 PH 值，转移溶液到容量瓶中，DI 水定容 → 滴加显色剂，调整溶液 PH 值至酸性 → 将溶液转移到吸收池中，UV－VIS 测定 → 制作报告

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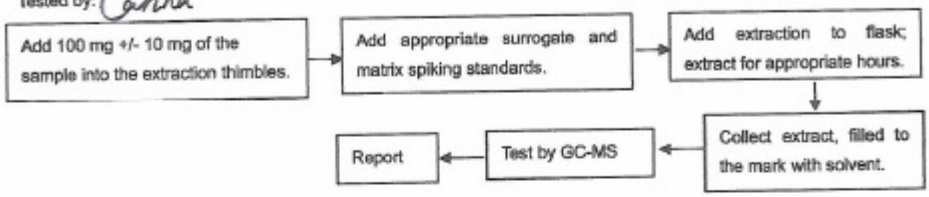
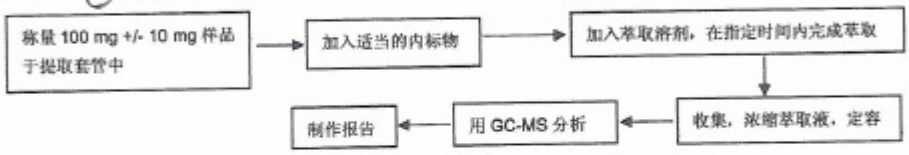
4. To Determine PBBs/PBDEs Content:

Tested by: Carina



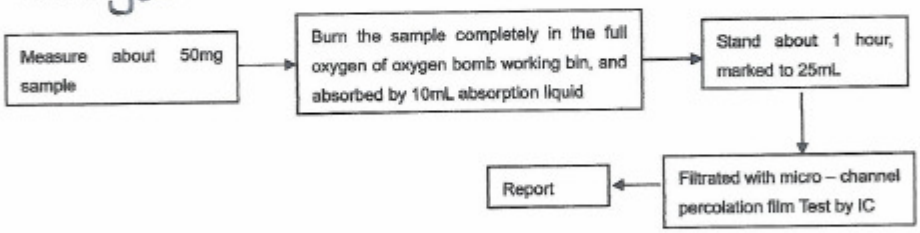
测定 PBBs&PBDEs 的含量

测试人员：Carina



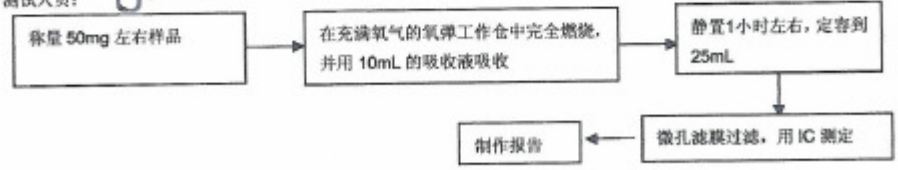
5. To Determine Fluorine, Chlorine, Bromine and Iodine Content:

Tested by: Jason



测定氟，氯，溴，碘含量

测试人员：Jason



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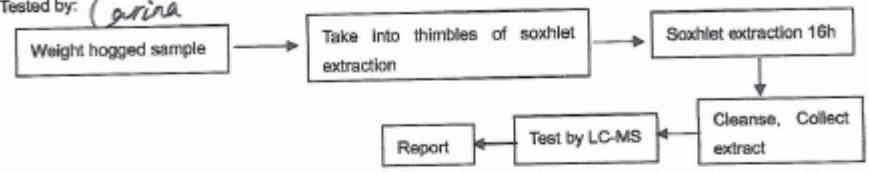
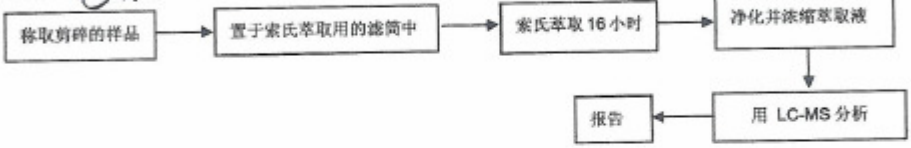
6. To Determine PFOS Content:

Tested by: Carina



测定 PFOS 的含量:

测试人员: Carina



Test Results/ 测 试 结 果:

1)

Item/项目	Unit/单位	RoHS Limit/ RoHS 限值	Results/ 结果
Lead (Pb)/铅 (Pb)	mg/kg	1000	N.D.
Cadmium (Cd)/镉 (Cd)	mg/kg	100	N.D.
Mercury (Hg)/汞(Hg)	mg/kg	1000	N.D.
Chromium (CrⅥ)/六价铬(CrⅥ)	mg/kg	1000	N.D.

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Flame Retardants/阻燃剂	Unit/单位	RoHS Limit/ RoHS 限值	Results/ 结果
PBBs/多溴联苯	mg/kg	1000	N.D.
MonoBB/一溴联苯	mg/kg	/	N.D.
DiBB/二溴联苯	mg/kg	/	N.D.
TriBB/三溴联苯	mg/kg	/	N.D.
TetraBB/四溴联苯	mg/kg	/	N.D.
PentaBB/五溴联苯	mg/kg	/	N.D.
HexaBB/六溴联苯	mg/kg	/	N.D.
HeptaBB/七溴联苯	mg/kg	/	N.D.
OctaBB/八溴联苯	mg/kg	/	N.D.
NonaBB/九溴联苯	mg/kg	/	N.D.
DecaBB/十溴联苯	mg/kg	/	N.D.
PBDEs/多溴联苯醚	mg/kg	1000	N.D.
MonoBDE/一溴联苯醚	mg/kg	/	N.D.
DiBDE/二溴联苯醚	mg/kg	/	N.D.
TriBDE/三溴联苯醚	mg/kg	/	N.D.
TetraBDE/四溴联苯醚	mg/kg	/	N.D.
PentaBDE/五溴联苯醚	mg/kg	/	N.D.
HexaBDE/六溴联苯醚	mg/kg	/	N.D.
HeptaBDE/七溴联苯醚	mg/kg	/	N.D.
OctaBDE/八溴联苯醚	mg/kg	/	N.D.
NonaBDE/九溴联苯醚	mg/kg	/	N.D.
DecaBDE/十溴联苯醚	mg/kg	/	N.D.

2)

Item/项目	Unitc	Limit/限值	Resultsc
Fluorine (F)/氟 (F)	mg/kg	/	N.D.
Chlorine (Cl)/氯 (Cl)	mg/kg	900	N.D.
Bromine (Br)/溴 (Br)	mg/kg	900	N.D.
Iodine (I)/碘 (I)	mg/kg	/	N.D.
Total (Br+ Cl)/总计（氯+溴）	mg/kg	1500	N.D.

3)

Item/项目	Unit/项目	Limit/限值	Result/限值
Perfluorooctane Sulfonates (PFOS) 全氟辛烷磺酸（PFOS） PFOS – Acid PFOS – 酸类 PFOS – Metal Salt PFOS – 金属盐类	mg/kg	See note 见备注	N.D.

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TEST REPORT

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Note/备 注:

-The new RoHS directive 2011/65/EU, on Jul. 21, 2011 come into force, on Jan. 03, 2013 the formal implementation, Directive 2002/95/EC shall be repealed simultaneously.

- 欧盟新 RoHS 指令 2011/65/EU，于 2011 年 7 月 21 日生效，2013 年 1 月 3 日正式实施，指令 2002/95/EC 同时废止。
- Specimens, which requested to determine Lead, Cadmium and Mercury Content, have been dissolved completely.
- 对于检测铅、镉、汞的样品已完全溶解。
- Reference information: Directive (EU) No 757/2010
- 相关信息：(EU) No 757/2010 指令
- (i) May not be placed on the market or used as a substance or constituent of preparations in a concentration equal to or higher than 0.001% by mass.
- (i) 不可于市场销售全氟辛烷磺酸化合物，其在成品中的浓度不得相等或超过总体的 0.001%；
- (ii) May not be placed on the market in semi-finished products or articles, or parts thereof, if the concentration of PFOS is equal to or higher than 0.1% by mass calculated with reference to the mass of structurally or microstructurally distinct parts that contain PFOS or, for textiles or other coated materials, if the amount of PFOS is equal to or higher than 1μg/m^2 of the coated material.
- (ii) 不得销售全氟辛烷磺酸化合物浓度相等于或超过总体 0.1%的半制成品或半制成品的部件；在纺织品或其他涂层物料，全氟辛烷磺酸化合物含量必须少于每平方米 1 微克。
- mg/kg=ppm
- N.D.=not detected(<MQL)
- N.D. =未检出（<MQL）
- MQL=Method Quantitation Limit
- MQL=方法定量检测下限
- Photo is included
- 附相片

深圳市安储特检测技术有限公司昆山分公司
中国江苏省昆山市周市镇天营路北侧9号厂房
电话号码：86-512-5510 8808 公司网址：www.aovt.com
（请保注意印刷页的条款）

查询热线
86-512-5510 8000

AOV®

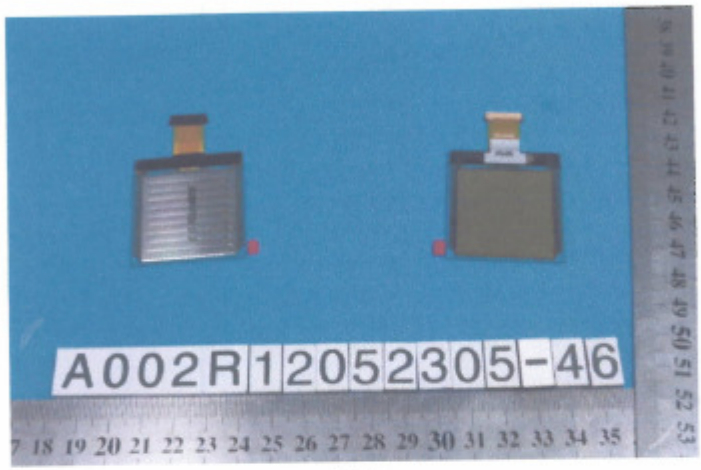
TEST REPORT

NO.: A002R12052305-46R01

Date: May. 28, 2012

Photograph of Sample

样 品 相 片



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End of Report

报告结束