

Specification for Approval

PRODUCT NAME: RGC16128064WR000
PRODUCT NO.: 9919405000

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2009. 04. 06	
X02	■ Modify FPC ■ Modify application circuit	2009. 04. 21	Page 5, 17 & 19
X03	■ Add single tape	2009. 06. 04	Page 4, 5 & 19
A01	■ Modify tape ■ Modify CIE specification ■ Add module part list ■ Add outgoing inspection provision ■ Add appendix of SGS report	2009. 09. 04	Page 4, 5, 6, 8, 9, 20, 21, 23, 24, 25, 26, 32, 33, 34, 35, 36, 37 & 38
A02	■ Modify definition of module thickness	2009. 09. 30	Page 5 & 20
A03	■ Add printing mark "W" on FPC	2010. 01. 08	Page 20

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1. SCOPE

This specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode
- Color : White
- Panel matrix : 128*64
- Driver IC : SSD1325
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.71mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial peripheral interface.
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 64 (H)	dot
2	Dot Size	0.255 (W) x 0.255 (H)	mm ²
3	Dot Pitch	0.285 (W) x 0.285 (H)	mm ²
4	Aperture Rate	80	%
5	Active Area	36.45 (W) x 18.21 (H)	mm ²
6	Panel Size	41.9 (W) x 28 (H)	mm ²
7*	Panel Thickness	1.42 ± 0.1	mm
8**	Module Size	41.9 (W) x 55.9 (H) x 1.845 (D)	mm ³
9	Diagonal A/A size	1.6	inch
10	Module Weight	4.04 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

** Module thickness includes panel, polarizer, protective film of polarizer, double sides tape and liner of double sides tape thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	$T_a = 25^{\circ}\text{C}$	IC maximum rating
Supply Voltage (V_{CC})	8	16	V	$T_a = 25^{\circ}\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^{\circ}\text{C}$		
Storage Temp	-40	85	$^{\circ}\text{C}$		
Humidity	-	85	%		
Life Time	10,000	-	Hrs	100 cd/m^2 , 50% checkerboard	Note (1)
Life Time	12,000	-	Hrs	80 cd/m^2 , 50% checkerboard	Note (2)
Life Time	16,000	-	Hrs	60 cd/m^2 , 50% checkerboard	Note (3)

Note:

(A) Under $V_{CC} = 15\text{V}$, $T_a = 25^{\circ}\text{C}$, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m^2 :

- Contrast setting : 0x45
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 80 cd/m^2 :

- Contrast setting : 0x37
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 60 cd/m^2 :

- Contrast setting : 0x29
- Frame rate : 105Hz
- Duty setting : 1/64

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

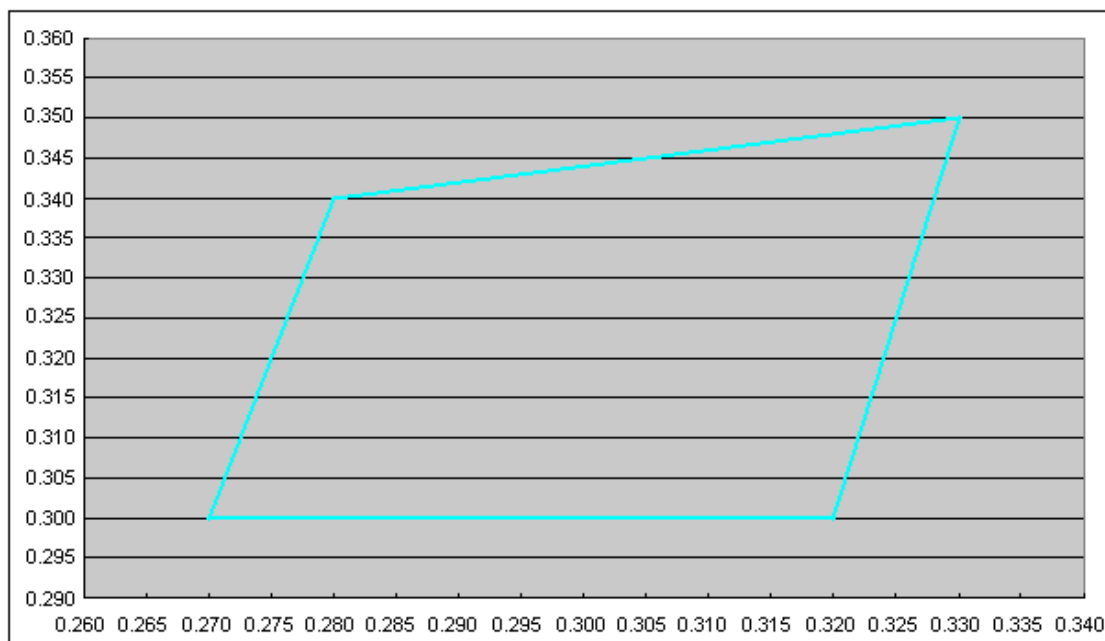
SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)	$T_a = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$	14.5	15	15.5	V
V_{DD}	Digital power supply	$T_a = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$	2.4	2.8	3.5	V
I_{DD}	Operating current for V_{DD} $V_{DD} = 2.7\text{V}$, $V_{CC} = 12\text{V}$, $I_{REF} = 10\text{uA}$ No panel attached, All Display ON	Contrast=7F	-	-	650	uA
I_{CC}	Operating current for V_{CC} $V_{DD} = 2.7\text{V}$, $V_{CC} = 12\text{V}$, $I_{REF} = 10\text{uA}$ No panel attached, All Display ON	Contrast=7F	-	700	-	uA
V_{IH}	Hi logic input level		$0.8^* V_{DD}$	-	V_{DD}	V
V_{IL}	Low logic input level		0	-	$0.2^* V_{DD}$	V
V_{OH}	Hi logic output level		$0.9^* V_{DD}$	-	V_{DD}	V
V_{OL}	Low logic output level		0	-	$0.1^* V_{DD}$	V
I_{SEG}	Segment on output current $V_{DD} = 2.7\text{V}$, $V_{CC} = 12\text{V}$, $I_{REF} = 10\text{uA}$, Display on, Segment pin under test is connected with a 20K resistive load to V_{SS}	Contrast=7F	270	300	370	uA
		Contrast=5F	-	225	-	uA
		Contrast=3F	-	150	-	uA
		Contrast=1F	-	75	-	uA

6.2 ELECTRO-OPTICAL CHARATERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		25	27	mA	All pixels on (1)
Standby mode current		3	4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		375	405	mW	All pixels on (1)
Standby mode power consumption		45	60	mW	Standby mode 10% pixels on (2)
Normal Luminance	60	80		cd/m ²	Display Average
Standby Luminance		10		cd/m ²	Display Average
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

PARAMETER	TRAPEZOID AREA				COMMENTS
CIE _x (White)	0.27	0.28	0.33	0.32	x, y (CIE 1931)
CIE _y (White)	0.30	0.34	0.35	0.30	



(1) Normal mode condition :

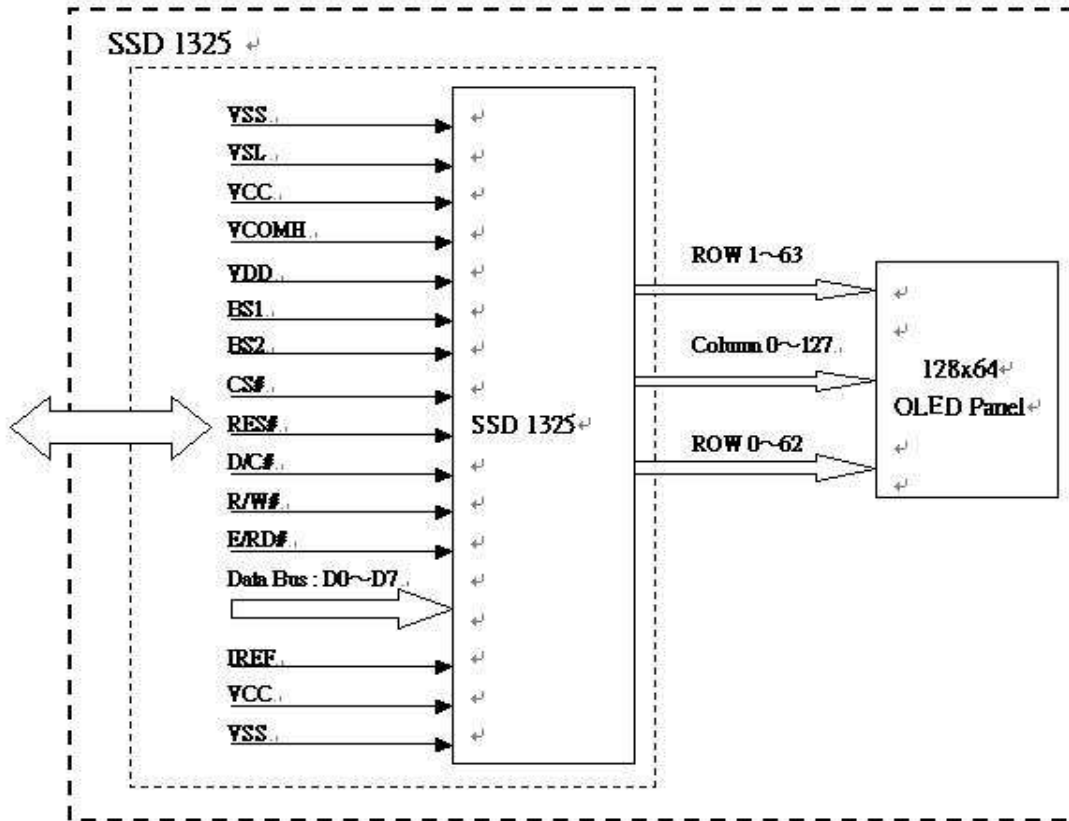
- Driving Voltage : 15V
- Contrast setting : 0x37
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x06
- Frame rate : 105Hz
- Duty setting : 1/64

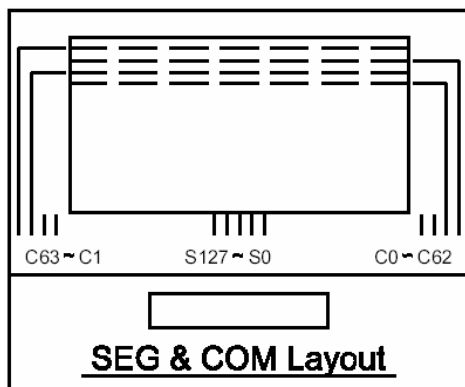
7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



RiTdisplay 128x64 OLED Module

7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	TYPE	Description
1	VSS	I	This is a ground pin.
2	VSL	O	This pin is the output pin for the voltage output low level for SEG signals. This pin can be kept NC or connected with a capacitor to VSS for stability.
3	VCC	I	Positive OLED high voltage power supply
4	VCOMH	O	The COM voltage reference pin, this pin should be connected to ground through a capacitor.
5	NC	I	No connection.
6	VDD	I	Voltage power supply for logic
7	BS1	-	Interface select pin
8	BS2	-	Interface select pin
9	CS#	I	Chip select pin. The driver IC will be selected When CS pin is active low.
10	RES#	I	Hardware reset signal
11	D/C#	I	Data/Command control pin. When it pulled high, the input at D0-D7 is treated as display data. When it pulled low, the input at D0-D7 is transferred to command register
12	R/W#	I	Write strobe signal and reads data at the low level
13	E(RD#)	I	Read strobe signal and reads data at the low level
14	D0	I/O	8-bit data bus
15	D1	I/O	8-bit data bus
16	D2	I/O	8-bit data bus
17	D3	I/O	8-bit data bus
18	D4	I/O	8-bit data bus
19	D5	I/O	8-bit data bus
20	D6	I/O	8-bit data bus
21	D7	I/O	8-bit data bus
22	IREF	I	The current reference input pin, this pin should be connected to ground through a resistor.
23	VCC	I	Positive OLED high voltage power supply
24	NC	I	No connection.
25	VSS	I	This is a ground pin.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to Table 3-7 for GDDRAM address map description)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
											(HEX)
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)
 (Display Startline=0)

Table 3– GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
											(HEX)
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]	
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]	
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)
 (Display Startline=0)

Table 4–GDDRAM address map showing Vertical Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		3F		3E			01		00		
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]	
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]	

COM Outputs Row Address (HEX)
 (Display Startline=0)

Table 5–GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)
 (Display Startline=10H)

Table 6–GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00										
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										

COM Outputs Row Address (HEX)
 (Display Startline=0)

Table 7–GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, ... , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH

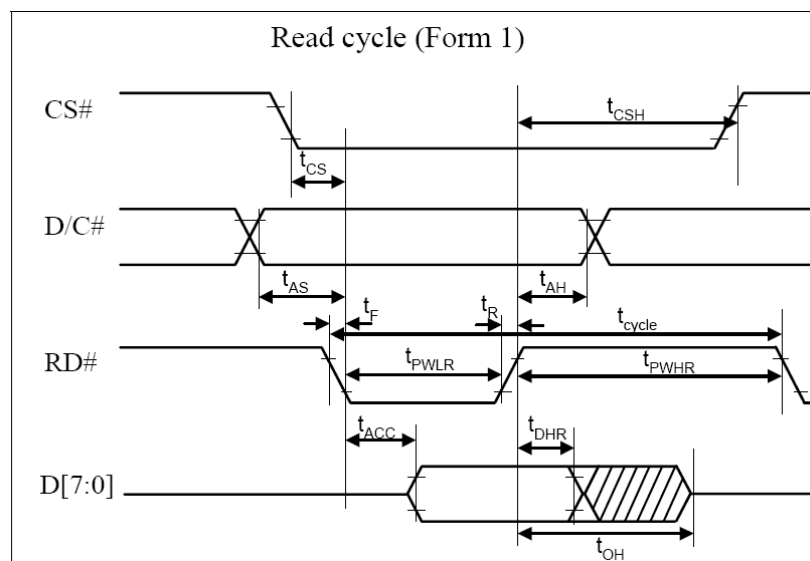
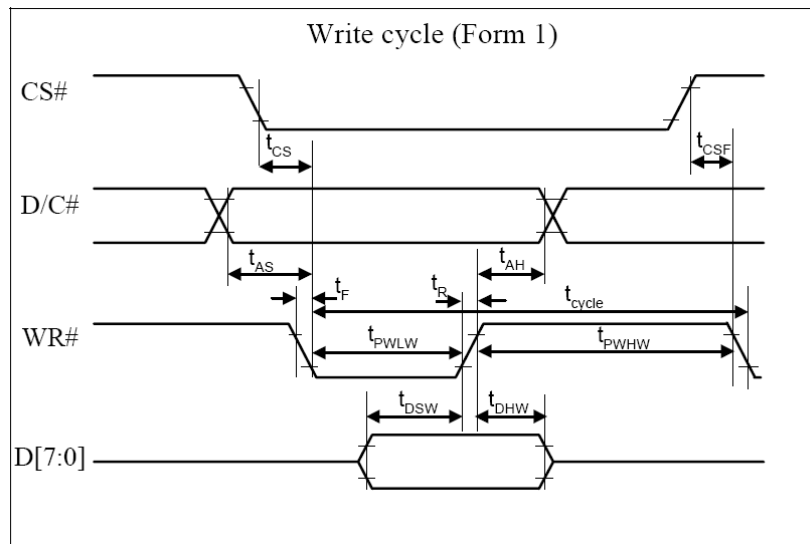
7.5 INTERFACE TIMING CHART

8080-Series MPU Parallel Interface Timing Characteristics

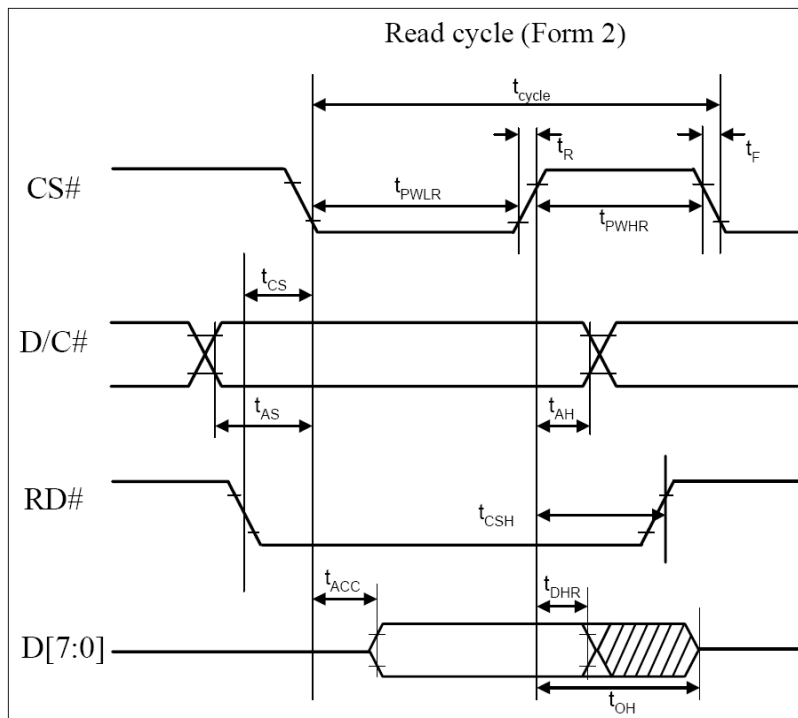
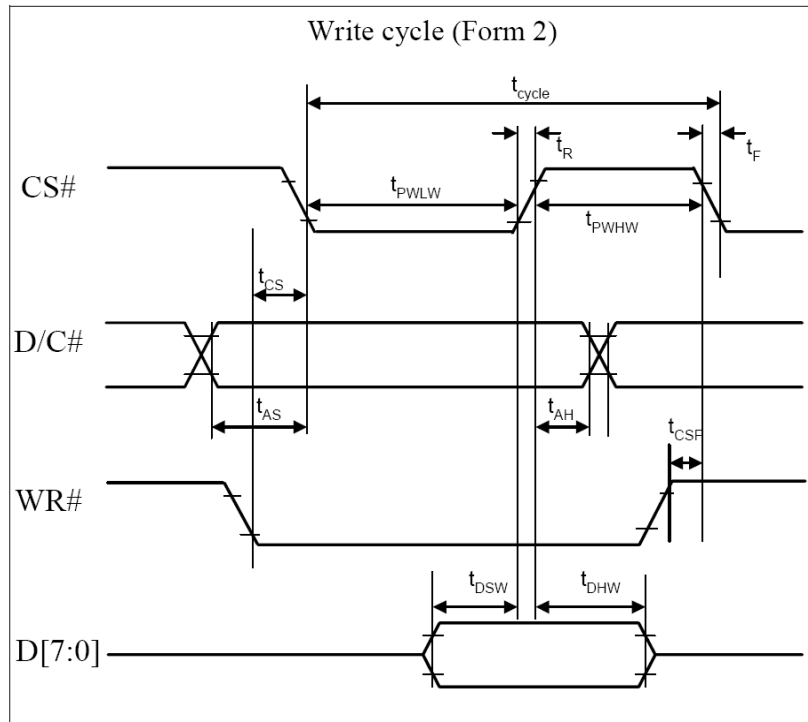
($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics (Form 1)



8080-series parallel interface characteristics (Form2)

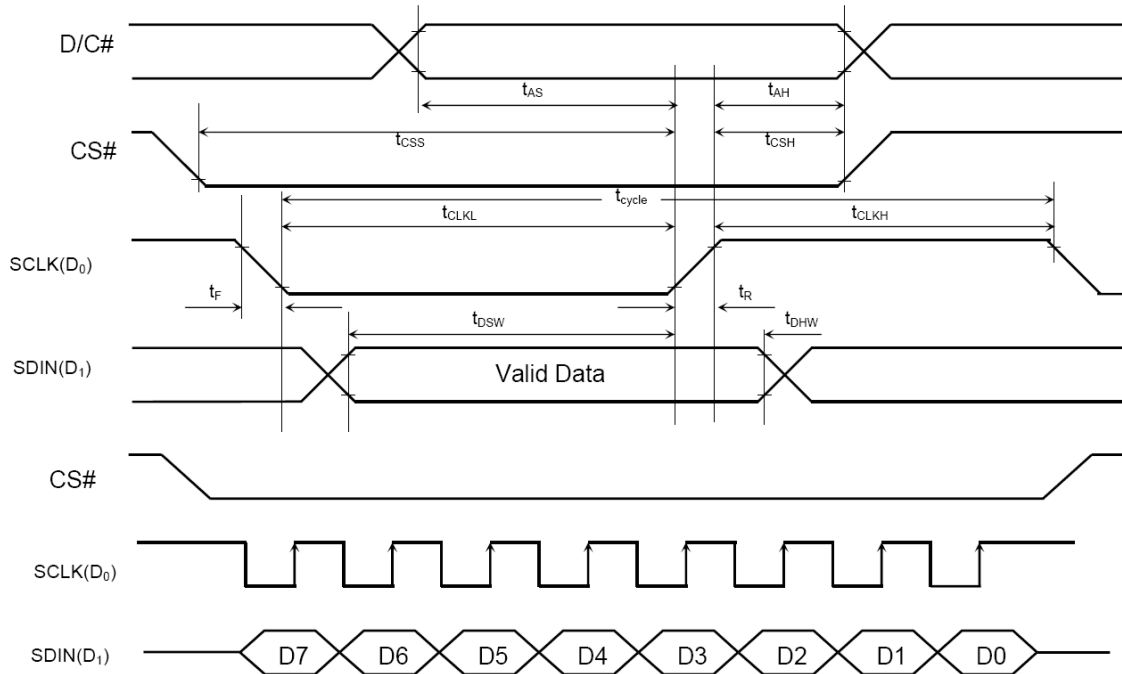


Serial Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial Interface Characteristics

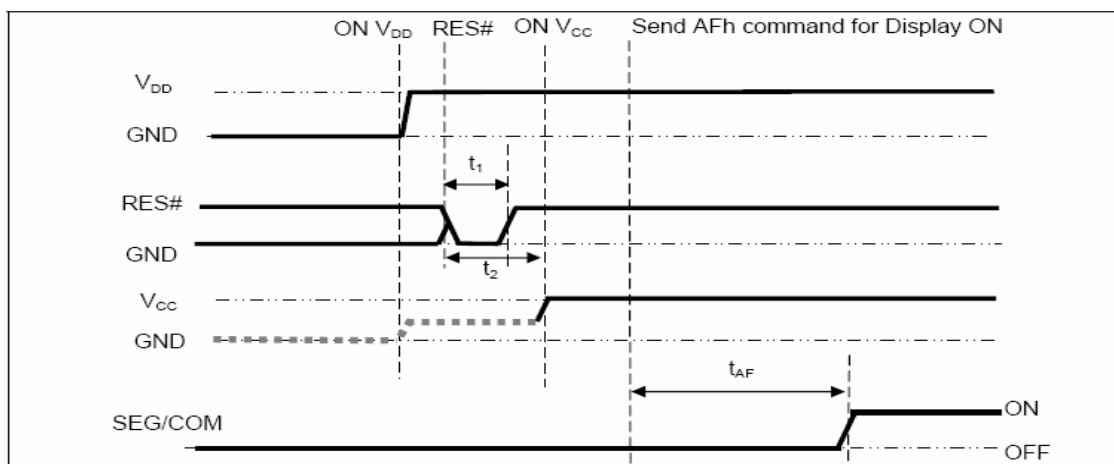


8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

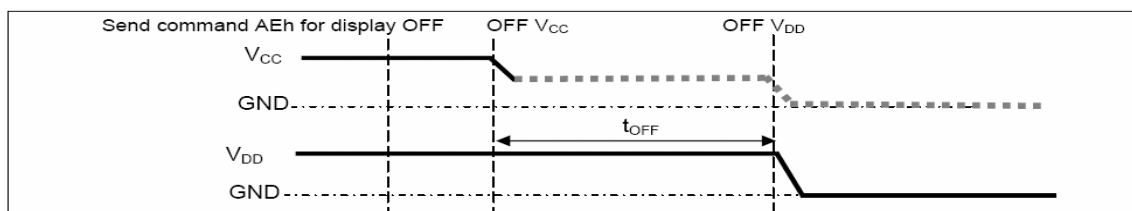
Power ON sequence:

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3 μ s(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3 μ s(t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF sequence:

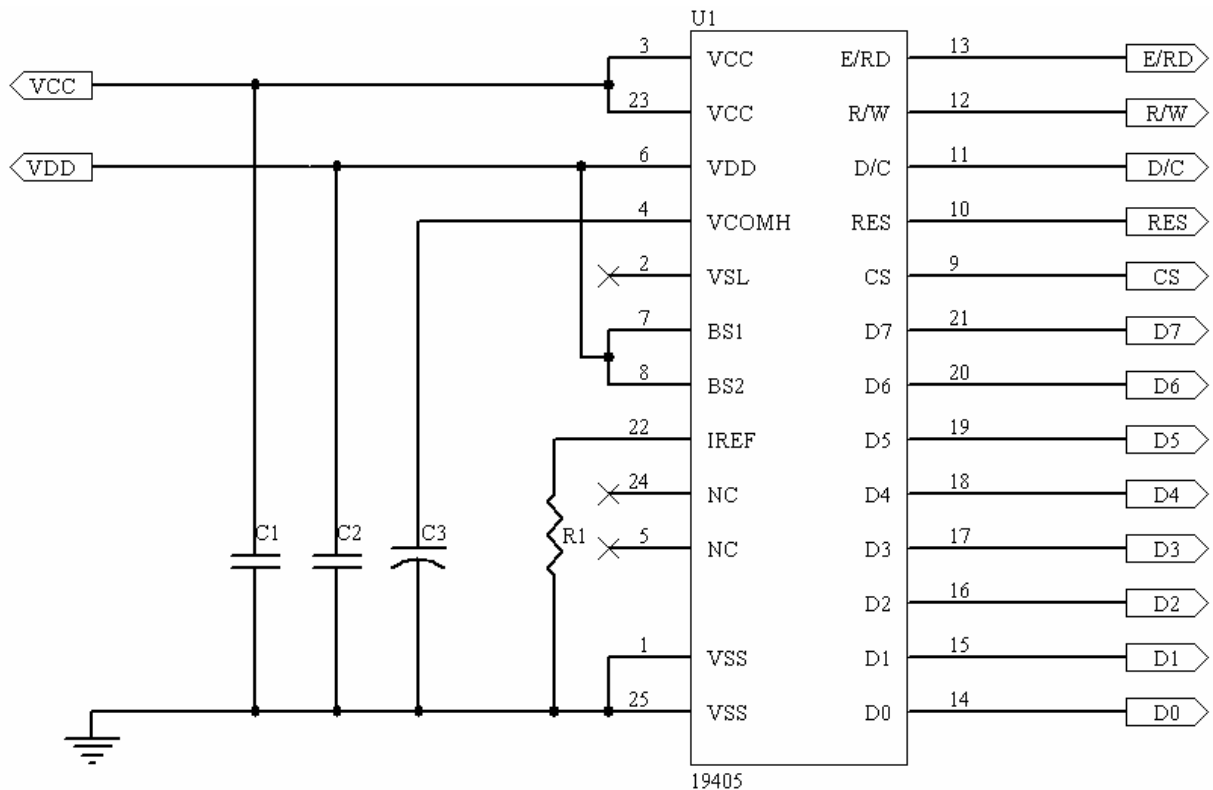
1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC}. (1), (2)
4. Wait for t_{OFF} . Power OFF V_{DD}. (where Minimum t_{OFF} =80ms, Typical t_{OFF} =100ms)



Note:

- (1) Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
- (2) V_{CC} should be kept float (disable) when it is OFF.
- (3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
- (4) The register values are reset after t_1 .
- (5) V_{DD} should not be Power OFF before V_{CC} Power OFF.

8.2 APPLICATION CIRCUIT



Recommend components :

C1: 2.2uF/25V (0805)

C2: 1uF/16V (0603)

C3: 4.7uF/35V (Tantalum type), or VISHAY (572D475X0025A2T)

R1: 1M ohm/1% (0603)

Notes: This circuit is for 8080 interfaces.

8.3 COMMAND TABLE

Refer to SSD1325 IC Spec.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions

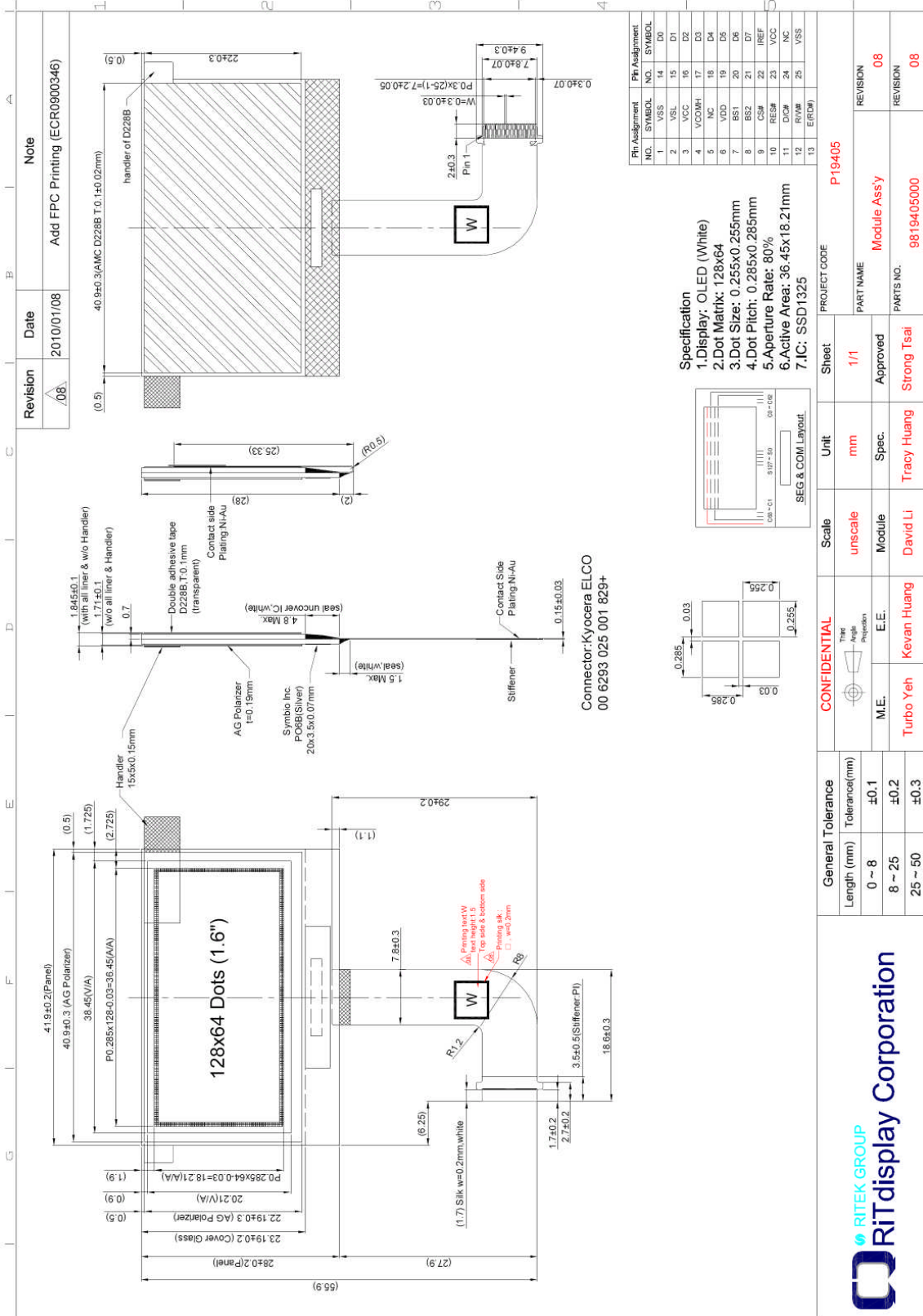
1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within $\pm 50\%$ of initial value.

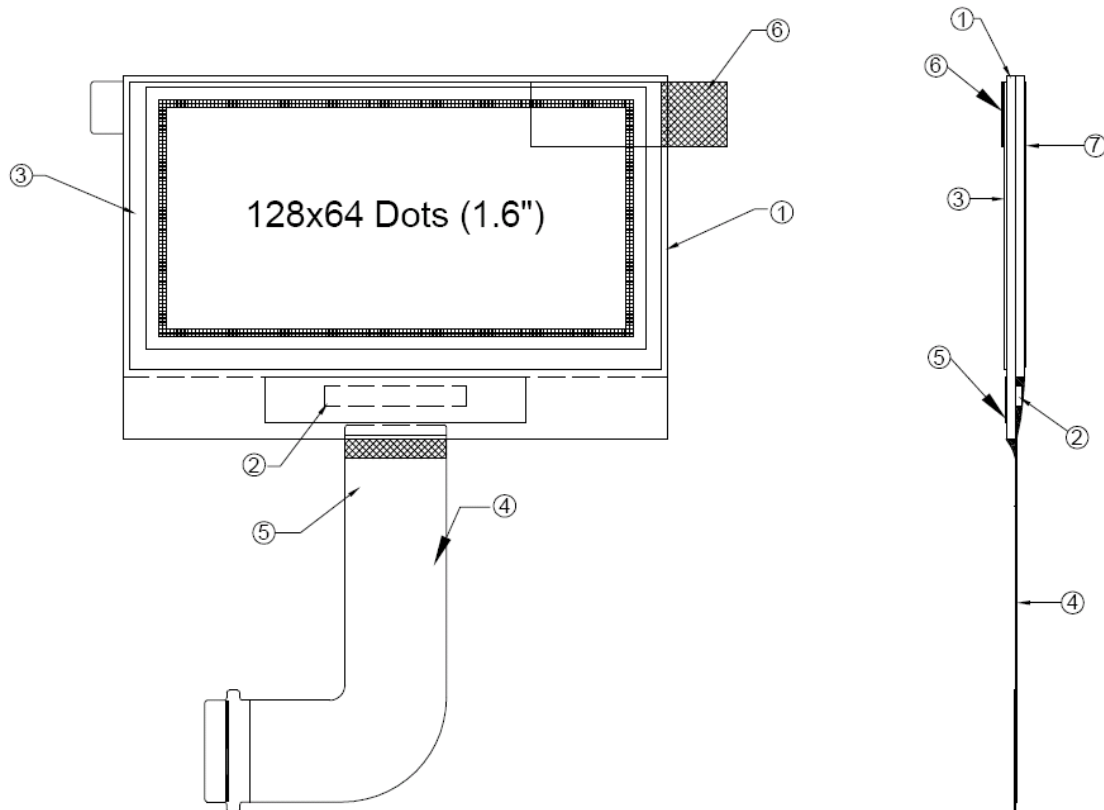
10. EXTERNAL DIMENSION

10.1 MODULE ASSEMBLY



10.2 MODULE PART LIST

Item	Parts Name	Description (Main spec)	Vender Name	Manufacture Name	Location of Production
1	Panel	Emitting component	RiTdisplay	RiTdisplay	Taiwan/Hsin Chu
1.1	-Substrate glass	Glass, 370*470*0.7mm	NSG	NSG	Japan/Yokkaichi
1.2	-Cover glass	Glass, 370*470*0.7mm	CIMELIA	CIMELIA	Taiwan/Miaoli
1.3	-UV gel	Nagase XNR5516	NAGASE	NAGASE	Japan/Tokyo
1.4	-Desiccant	OleDry	Futaba	Futaba	Japan/Chiba
2	IC	SSD1325Z	SOLOMON	SOLOMON	Taiwan/Hsin Chu
3	Polarizer	Circular Polarizer Middle 20.9*7*0.2mm	samsung	samsung	Korea/Suwon
4	FPC	FPC Film 25.7*7.8mm,Ni-Au	Zhuhai Soft win	Zhuhai Soft win	China/Zhuhai
5	Shielding Tape	PO6B (Silver) 20X3.5X0.07mm	Symbio, Inc.	Symbio, Inc.	Taiwan/ Taoyuan
6	Handler	Handler 5X15X0.15	Alliance Material Co.,Ltd	Alliance Material Co.,Ltd	Taiwan/Hsin Chu
7	Double tape	double tape 40.9*22*0.1 , D228B	Alliance Material Co.,Ltd	Alliance Material Co.,Ltd	Taiwan/Hsin Chu



11. PACKING SPECIFICATION

	Revision	Date	Note
	01	2009/03/17	Packing Tray Instruction

① 9819405000
Module Assy For P19405
x20 pcs
Face up ,Rotate packing
顯示面朝上,旋轉放置

② 3008000208
Tray 330x270x8.7mm
T=0.7mm,PS,P19401

③ 3010000002
5G Silica Gel Desiccants
5G 矽膠乾燥劑

④ Vacuum Bag ONY/LDPE
480x285x90
真空包裝袋ONY/LDPE

⑤ 3003000016
Antistatic Bubble bag 440x(350+450)mm
抗靜電氣泡包裝袋

⑥ 3001000005
Pizza Box 345x285x88,
B corrugated

⑦ 3000000009
Carton 385x305x203mm

⑧ 3006000000
Label 標籤
Label x2 pcs

⑨ 3008000125
Tape 封箱膠帶

⑩ 3006000000
Label 標籤
Label x1 pcs

Vacuum packing : 4 sec
抽真空:4 秒

Rotate stack
旋轉堆疊

ITEM	PART No.	DESC	QTY
	9819405000		1
1	9819405000	Module Assy For P19405	640
2	3008000208	Tray 330x270x8.7 T:0.7mm PS P19401	34
3	3010000002	5G Silica Gel Desiccants	8
4	3003000016	Vacuum Bag ONY/LDPE 480x285x90	2
5	3003000016	Antistatic Bubble bag 440x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88,B corrugated	2
7	3000000009	Carton 385x305x203mm	1
8	3006000000	Label	3
9	3006000125	Tape, W=48mm, L=910cm	

CONFIDENTIAL		PROJECT CODE	P 19405	
M.E.	E.E.	PART NAME	Packing Tray Instruction	
Valerie Lo	Kevan Huang	PARTS NO.	9919405000	
Valerie Lo	Tracy Huang	REVISION	01	
Kevan Huang	Strong Tsai	REVISION	01	

	General Tolerance	Scale	Unit	Sheet	PROJECT CODE
Length (mm)	Tolerance(mm)	1:3.5	mm	1/1	P 19405
0 - 8	±0.1			Approved	
8 - 25	±0.2			Spec.	
25 - 50	±0.3			Module	
				Valerie Lo	
				Kevan Huang	
				Tracy Huang	
				Strong Tsai	

RITEK GROUP
RiTdisplay Corporation

12. OUTGOING INSPECTION PROVISION

SAMPLING METHOD

- (1) MIL-STD-105E/inspection level II/normal inspection/single sample inspection
- (2) AQL: Major 0.65; Minor 1.0

INSPECTION CONDITION

The inspection and measurement are performed under the following conditions, unless otherwise specified.

Temperature: 25±5°C

Humidity: 50±10%R.H.

Pressure: 860~1060hPa (mbar)

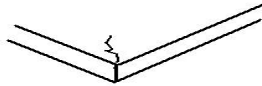
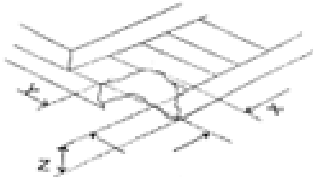
Distance between the panel and eyes of the inspector ≥ 30cm

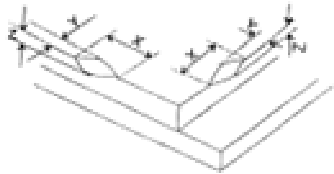
SPECIFICATION FOR QUALITY CHECK

i. DEFECT CLASSIFICATION

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
Major Defect	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension out of specification	
Minor Defect	1. Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2. Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot 、 Bright spot 、dust	
	4. Film	(1) Damage	
		(2) Foreign material	

ii. OUTGOING SPECIFICATION

Item	Description	Criterion	AQL															
I. Panel	1. Glass scratch	<table border="1"> <thead> <tr> <th>Width (mm) W</th> <th>Length (mm) L</th> <th>number of pieces permitted</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.03$</td> <td>Ignore</td> <td>Ignore</td> </tr> <tr> <td>$0.03 < W \leq 0.05$</td> <td>$L \leq 3$</td> <td>3</td> </tr> <tr> <td>$0.05 < W$</td> <td>-----</td> <td>None</td> </tr> <tr> <td>beyond A.A.</td> <td>-----</td> <td>Ignore</td> </tr> </tbody> </table>	Width (mm) W	Length (mm) L	number of pieces permitted	$W \leq 0.03$	Ignore	Ignore	$0.03 < W \leq 0.05$	$L \leq 3$	3	$0.05 < W$	-----	None	beyond A.A.	-----	Ignore	Minor
	Width (mm) W	Length (mm) L	number of pieces permitted															
	$W \leq 0.03$	Ignore	Ignore															
$0.03 < W \leq 0.05$	$L \leq 3$	3																
$0.05 < W$	-----	None																
beyond A.A.	-----	Ignore																
2. Glass crack	<p>(1) Crack Propagation crack is not acceptable.</p> 	Major																
3. Glass chip	<p>(1) Chip on corner</p>  <table border="1"> <thead> <tr> <th>Width (mm) Y</th> <th>Length (mm) X</th> <th>Thickness (mm) Z</th> <th>number of pieces permitted (total)</th> </tr> </thead> <tbody> <tr> <td>$Y \leq 1.5$</td> <td>$X \leq 1.8$</td> <td>$Z \leq t$</td> <td>3</td> </tr> <tr> <td>$Y > 1.5$</td> <td>$X > 1.8$</td> <td>$Z \leq t$</td> <td>0</td> </tr> </tbody> </table>	Width (mm) Y	Length (mm) X	Thickness (mm) Z	number of pieces permitted (total)	$Y \leq 1.5$	$X \leq 1.8$	$Z \leq t$	3	$Y > 1.5$	$X > 1.8$	$Z \leq t$	0	Minor				
Width (mm) Y	Length (mm) X	Thickness (mm) Z	number of pieces permitted (total)															
$Y \leq 1.5$	$X \leq 1.8$	$Z \leq t$	3															
$Y > 1.5$	$X > 1.8$	$Z \leq t$	0															

Item	Description	Criteria	AQL															
I. Panel	3. Glass chip	(2) Chip on edge  <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>Width (mm) Y</th> <th>Length (mm) X</th> <th>Thickness (mm) Z</th> <th>number of pieces permitted (one side)</th> <th>number of pieces permitted (total)</th> </tr> </thead> <tbody> <tr> <td>$Y \leq 0.8$</td> <td>$X \leq 2.5$</td> <td>$Z \leq t$</td> <td>2</td> <td>6</td> </tr> <tr> <td>$Y > 0.8$</td> <td>$X > 2.5$</td> <td>$Z \leq t$</td> <td>0</td> <td>0</td> </tr> </tbody> </table>	Width (mm) Y	Length (mm) X	Thickness (mm) Z	number of pieces permitted (one side)	number of pieces permitted (total)	$Y \leq 0.8$	$X \leq 2.5$	$Z \leq t$	2	6	$Y > 0.8$	$X > 2.5$	$Z \leq t$	0	0	Minor
	Width (mm) Y	Length (mm) X	Thickness (mm) Z	number of pieces permitted (one side)	number of pieces permitted (total)													
	$Y \leq 0.8$	$X \leq 2.5$	$Z \leq t$	2	6													
$Y > 0.8$	$X > 2.5$	$Z \leq t$	0	0														
		(3) Raised on edge <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>Width (mm) Y</th> <th>Length (mm) X</th> <th>Thickness (mm) Z</th> <th>number of pieces permitted (one side)</th> <th>number of pieces permitted (total)</th> </tr> </thead> <tbody> <tr> <td>$Y \leq 0.15$</td> <td>$X \leq 2.5$</td> <td>$Z \leq t$</td> <td>2</td> <td>6</td> </tr> <tr> <td>$Y > 0.15$</td> <td>$X > 2.5$</td> <td>$Z \leq t$</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>Note:</p> <ol style="list-style-type: none"> t = glass thickness Chip on the corner extending into the ITO contact is not acceptable. Chip on the corner is not acceptable when it extends into the seal or makes the seal exposure. 	Width (mm) Y	Length (mm) X	Thickness (mm) Z	number of pieces permitted (one side)	number of pieces permitted (total)	$Y \leq 0.15$	$X \leq 2.5$	$Z \leq t$	2	6	$Y > 0.15$	$X > 2.5$	$Z \leq t$	0	0	Minor
Width (mm) Y	Length (mm) X	Thickness (mm) Z	number of pieces permitted (one side)	number of pieces permitted (total)														
$Y \leq 0.15$	$X \leq 2.5$	$Z \leq t$	2	6														
$Y > 0.15$	$X > 2.5$	$Z \leq t$	0	0														
	4. Dimension	Refer to the drawing of the spec	Major															
II. Polarizer	1. Scratch	Spot type in accordance with the criteria of "Item II-3. Polarizer bubble". Line type in accordance with the criteria of "Item I-1. Glass scratch".	Minor															
	2. Stains on surface	Stains cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor															
	3. Polarizer bubble	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2">(mm)</th> </tr> <tr> <th>Size</th> <th>number of pieces permitted</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.2$</td> <td>Ignore</td> </tr> <tr> <td>$0.2 < \Phi \leq 0.5$</td> <td>2</td> </tr> <tr> <td>$0.5 < \Phi$</td> <td>0</td> </tr> <tr> <td>beyond A.A.</td> <td>Ignore</td> </tr> </tbody> </table>	(mm)		Size	number of pieces permitted	$\Phi \leq 0.2$	Ignore	$0.2 < \Phi \leq 0.5$	2	$0.5 < \Phi$	0	beyond A.A.	Ignore	Minor			
(mm)																		
Size	number of pieces permitted																	
$\Phi \leq 0.2$	Ignore																	
$0.2 < \Phi \leq 0.5$	2																	
$0.5 < \Phi$	0																	
beyond A.A.	Ignore																	

Item	Description	Criteria	AQL																										
III. Displaying	1. Power consumption	The module operating current consumption should not go beyond the standard indicated in Product Specification	Major																										
	2. Pixel size	The tolerance of display pixel dimension should be within $\pm 25\%$ of specification.	Minor																										
	3. Color	Refer to the product specification.	Major																										
	4. Luminance	Refer to the product specification.	Major																										
	5. Dimming spot 、 Lighting spot 、 Dust	<p>1.</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>average diameter D:(mm)</th> <th>number of pieces permitted</th> </tr> </thead> <tbody> <tr> <td>$D \leq 0.1$</td> <td>Ignore</td> </tr> <tr> <td>$0.1 < D \leq 0.15$</td> <td>1</td> </tr> <tr> <td>$0.15 < D \leq 0.2$</td> <td>1</td> </tr> <tr> <td>$0.2 < D$</td> <td>0</td> </tr> <tr> <td>beyond A.A.</td> <td>Ignore</td> </tr> </tbody> </table> <p style="margin-left: 40px;">D=(long diameter + short diameter)/2. Pixel off is not allowed.</p> <p>2.</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>width(mm) W</th> <th>length(mm) L</th> <th>number of pieces permitted</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.03$</td> <td>Ignore</td> <td>Ignore</td> </tr> <tr> <td>$0.03 < W \leq 0.05$</td> <td>$L \leq 3$</td> <td>3</td> </tr> <tr> <td>$0.05 < W$</td> <td>-----</td> <td>None</td> </tr> <tr> <td>beyond A.A.</td> <td>-----</td> <td>Ignore</td> </tr> </tbody> </table>	average diameter D:(mm)	number of pieces permitted	$D \leq 0.1$	Ignore	$0.1 < D \leq 0.15$	1	$0.15 < D \leq 0.2$	1	$0.2 < D$	0	beyond A.A.	Ignore	width(mm) W	length(mm) L	number of pieces permitted	$W \leq 0.03$	Ignore	Ignore	$0.03 < W \leq 0.05$	$L \leq 3$	3	$0.05 < W$	-----	None	beyond A.A.	-----	Ignore
average diameter D:(mm)	number of pieces permitted																												
$D \leq 0.1$	Ignore																												
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$0.2 < D$	0																												
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width(mm) W	length(mm) L	number of pieces permitted																											
$W \leq 0.03$	Ignore	Ignore																											
$0.03 < W \leq 0.05$	$L \leq 3$	3																											
$0.05 < W$	-----	None																											
beyond A.A.	-----	Ignore																											
IV. Film	1. Dimension	Film dimension out of Spec.	Major																										
	2. Damage	Crack; deep scratch; deep fold; deep pressure mark or other damage is not acceptable.	Minor																										
	3. Foreign material	Conductive foreign material sticking to the leads, foreign material between film and glass are not acceptable.	Minor																										

13. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

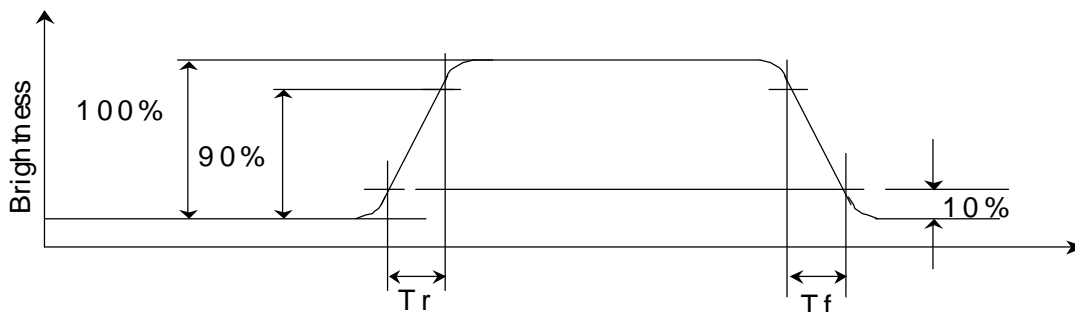


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

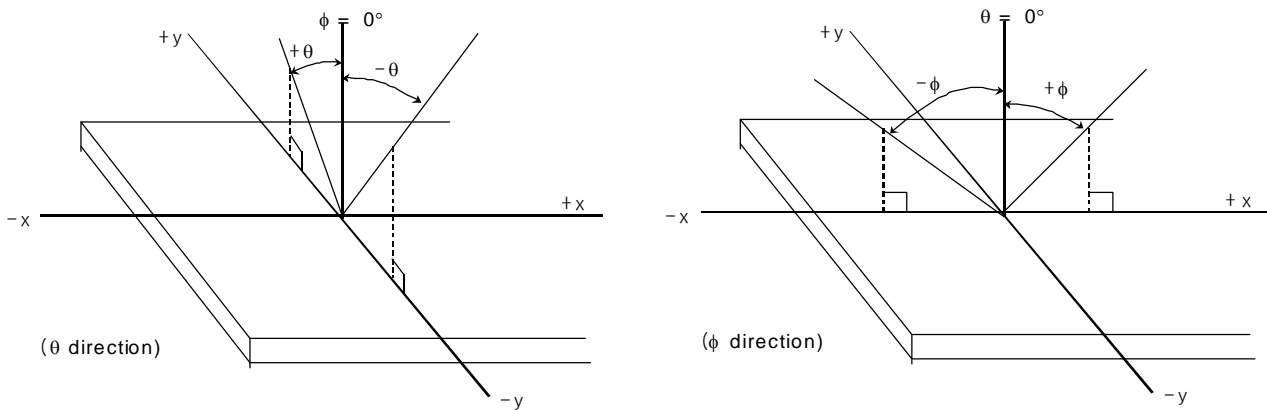
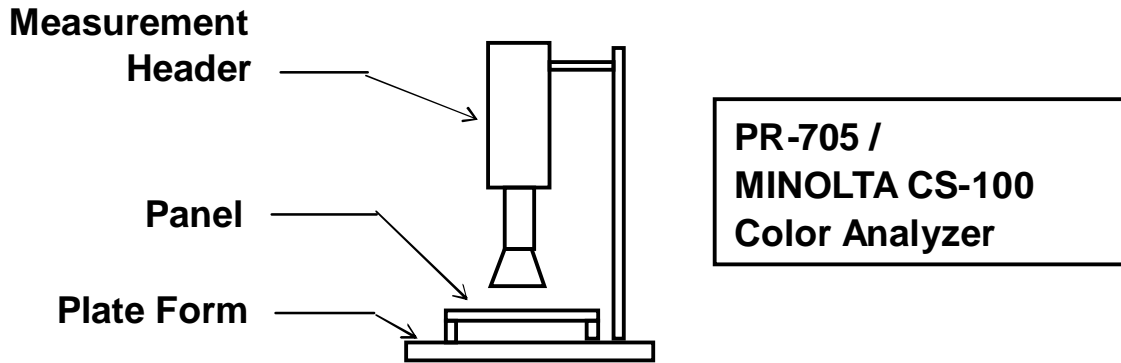


Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

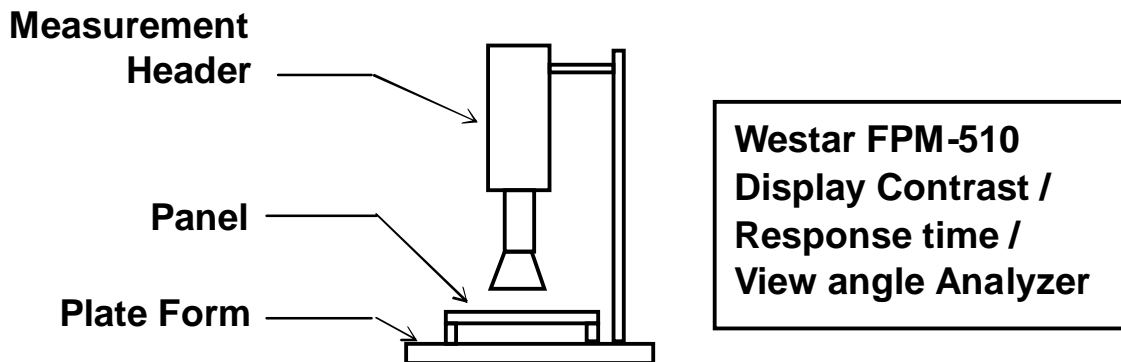
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

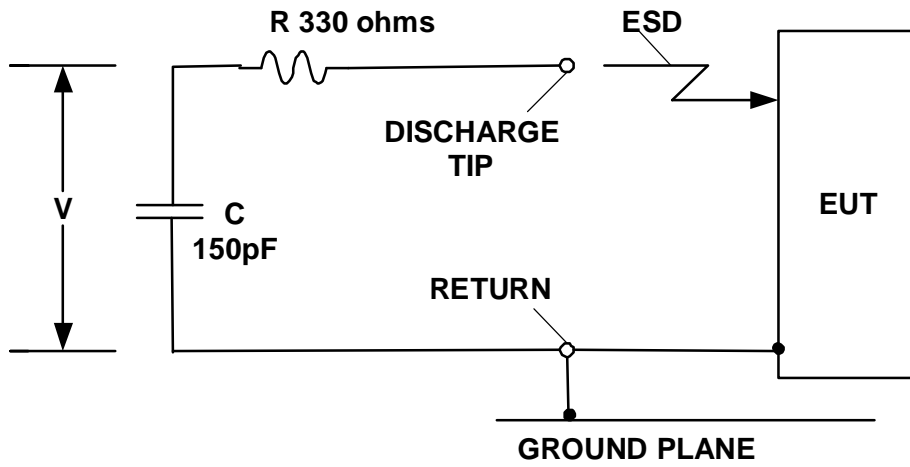


B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE





APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

APPENDIX 4: SGS REPORT






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請洽 SGS
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www.tw.sgs.com

測試報告
Test Report

群賢科技股份有限公司
RITDISPLAY CORPORATION
新竹縣湖口鄉新竹工業區光復北路12號
NO. 12, KUANFU N. ROAD, HSIN CHU INDUSTRIAL PARK, TAIWAN, 30316 R. O. C.


號碼(No.) : CE/2009/75827 日期(Date) : 2009/08/05 頁數(Page) : 1 of 7



以下測試樣品係由客戶送樣，且由客戶聲稱並經客戶確認如下 (The following samples was/were submitted and identified by/on behalf of the client as) :

樣品名稱(Sample Description)	: OLED MODULE
樣品型號(Style/Item No.)	: P19405 / P19408
收件日期(Sample Receiving Date)	: 2009/07/29
測試期間(Testing Period)	: 2009/07/29 TO 2009/08/05

測試結果(Test Results) : 請見下一頁 (Please refer to next pages).



Chenyu Kung / Operation Manager
Signed for and on behalf of
SGS TAIWAN LTD.
Chemical Laboratory – Taipei

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測試報告
Test Report

號碼(No.): CE/2009/75827 日期(Date): 2009/08/05 頁數(Page): 2 of 7

群賢科技股份有限公司
 RITDISPLAY CORPORATION
 新竹縣湖口鄉新竹工業區光復北路12號
 NO. 12, KUANGFU N. ROAD, HSIN CHU INDUSTRIAL PARK, TAIWAN, 30316 R. O. C.



測試結果(Test Results)

測試部位(PART NAME) NO.1 : 整體混測 (MIXED ALL PARTS)

測試項目 (Test Items)	單位 (Unit)	測試方法 (Method)	方法偵測 極限值 (MDL)	結果 (Result) ND.1
鎘 / Cadmium (Cd)	mg/kg	參考IEC 62321: 2008方法, 用感應耦合電漿原子發射光譜儀檢測。 / With reference to IEC 62321: 2008 and performed by ICP-AES.	2	n.d.
鉛 / Lead (Pb)	mg/kg	參考IEC 62321: 2008方法, 用感應耦合電漿原子發射光譜儀檢測。 / With reference to IEC 62321: 2008 and performed by ICP-AES.	2	n.d.
汞 / Mercury (Hg)	mg/kg	參考IEC 62321: 2008方法, 用感應耦合電漿原子發射光譜儀檢測。 / With reference to IEC 62321: 2008 and performed by ICP-AES.	2	n.d.
六價鉻 / Hexavalent Chromium Cr(VI) by alkaline extraction	mg/kg	參考IEC 62321: 2008方法, 用UV-VIS 檢測。 / With reference to IEC 62321: 2008 and performed by UV-VIS.	2	n.d.
鹵素(氯) / Halogen-Chlorine (Cl) (CAS No.: 022537-15-1)	mg/kg	參考BS EN 14582:2007, 以離子層析儀分析。 / With reference to BS EN 14582:2007. Analysis was performed by IC.	50	n.d.
鹵素(溴) / Halogen-Bromine (Br) (CAS No.: 010097-32-2)	mg/kg	參考BS EN 14582:2007, 以離子層析儀分析。 / With reference to BS EN 14582:2007. Analysis was performed by IC.	50	n.d.

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測試報告
Test Report

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錸寶科技股份有限公司
 RITDISPLAY CORPORATION
 新竹縣湖口鄉新竹工業區光復北路12號
 NO. 12, KUANFU N. ROAD, HSIN CHU INDUSTRIAL PARK, TAIWAN, 30316 R. O. C.



測試項目 (Test Items)	單位 (Unit)	測試方法 (Method)	方法偵測 極限值 (MDL)	結果 (Result)
多溴聯苯總和 / Sum of PBBs	mg/kg	參考IEC 62321: 2008方法, 以氣相層析儀/質譜儀檢測。 / With reference to IEC 62321: 2008 and performed by GC/MS.	-	n.d.
一溴聯苯 / Monobromobiphenyl			5	n.d.
二溴聯苯 / Dibromobiphenyl			5	n.d.
三溴聯苯 / Tribromobiphenyl			5	n.d.
四溴聯苯 / Tetrabromobiphenyl			5	n.d.
五溴聯苯 / Pentabromobiphenyl			5	n.d.
六溴聯苯 / Hexabromobiphenyl			5	n.d.
七溴聯苯 / Heptabromobiphenyl			5	n.d.
八溴聯苯 / Octabromobiphenyl			5	n.d.
九溴聯苯 / Nonabromobiphenyl			5	n.d.
十溴聯苯 / Decabromobiphenyl			5	n.d.
多溴聯苯醚總和 / Sum of PBDEs			-	n.d.
一溴聯苯醚 / Monobromodiphenyl ether			5	n.d.
二溴聯苯醚 / Dibromodiphenyl ether			5	n.d.
三溴聯苯醚 / Tribromodiphenyl ether			5	n.d.
四溴聯苯醚 / Tetrabromodiphenyl ether			5	n.d.
五溴聯苯醚 / Pentabromodiphenyl ether			5	n.d.
六溴聯苯醚 / Hexabromodiphenyl ether			5	n.d.
七溴聯苯醚 / Heptabromodiphenyl ether			5	n.d.
八溴聯苯醚 / Octabromodiphenyl ether			5	n.d.
九溴聯苯醚 / Nonabromodiphenyl ether	5	n.d.		
十溴聯苯醚 / Decabromodiphenyl ether	5	n.d.		

備註(Note) :

1. mg/kg = ppm ; 0.1wt% = 1000ppm
2. n.d. = Not Detected (未檢出)
3. MDL = Method Detection Limit (方法偵測極限值)
4. "-" = Not Regulated (無規格值)
5. 樣品的測試是基於申請人要求混合測試, 報告中的混合測試結果不代表其中個別單一材質的含量。
 (The samples was/were analyzed on behalf of the applicant as mixing sample in one testing.
 The above results was/were only given as the informality value.)

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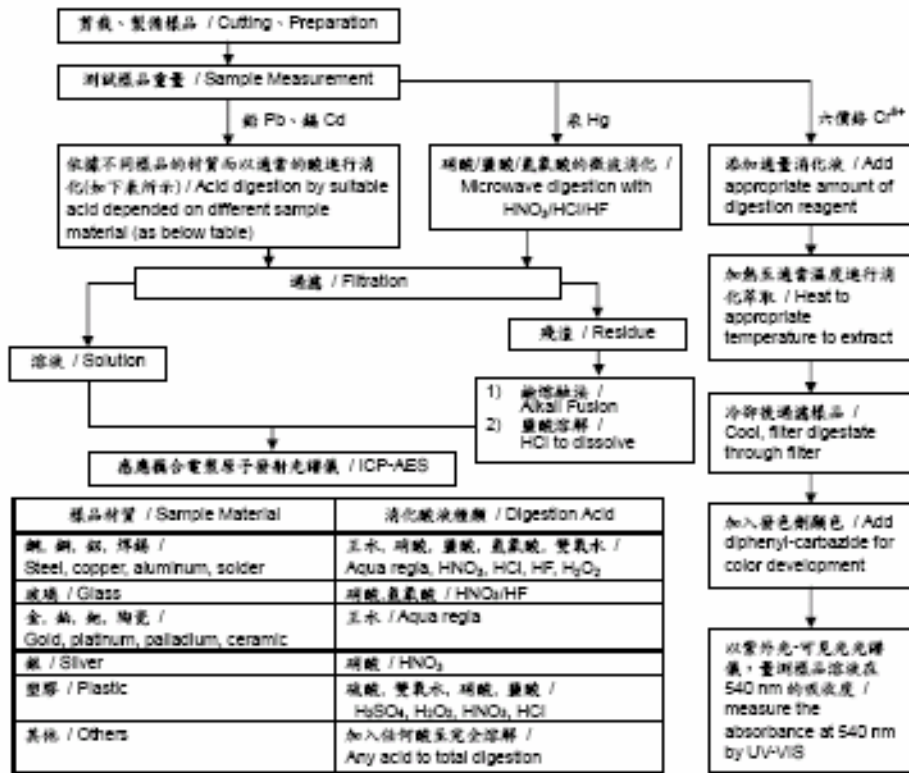


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- 1) 根據以下的流程圖之條件，樣品已完全溶解。(六價鉻測試方法除外) / These samples were dissolved totally by pre-conditioning method according to below flow chart. (Cr⁶⁺ test method excluded)
- 2) 測試人員：楊登偉 / Name of the person who made measurement: Climgreat Yang
- 3) 測試負責人：張德興 / Name of the person in charge of measurement: Troy Chang



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鹵素分析流程圖 / Analytical flow chart of halogen content

- 1) 測試人員：陳立倫 / Name of the person who made measurement: Alan Chen
- 2) 測試負責人：張啓興 / Name of the person in charge of measurement: Troy Chang



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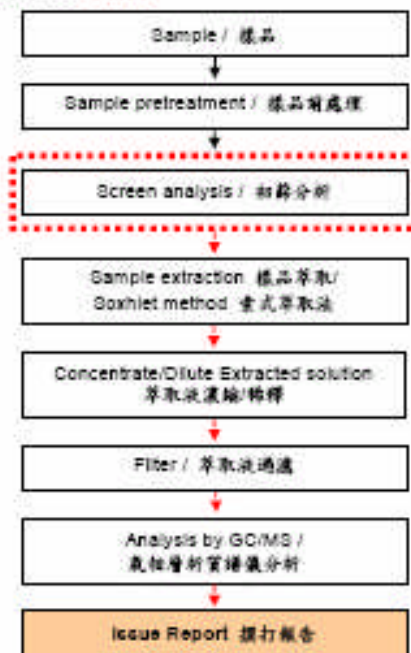
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多溴聯苯/多溴聯苯醚分析流程圖 / PBB/PBDE analytical FLOW CHART

- 1) 測試人員：翁賜彬 / Name of the person who made measurement: Roman Wong
 - 2) 測試負責人：陳新智 / Name of the person in charge of measurement: Shinjyh Chen
- 初次測試程序 / First testing process ———→
- 選擇性轉換程序 / Optional screen process→
- 確認程序 / Confirmation process - - - ->



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**** 報告結尾(End of Report) ****

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