SGM8433-2
Low-Distortion, Dual-Power Operational Amplifier with Integrated Protection for Resolver Drive

GENERAL DESCRIPTION

The SGM8433-2 is a dual-power, high performance operational amplifier with integrated protection, which is specifically designed for applications involving resolvers. The device features high gain-bandwidth product and high slew rate. It also offers a continuous high output current drive. These characteristics make the device highly suitable for providing the requisite low-distortion, high-level differential excitation essential for activating the primary coil of a resolver. The device integrates over-temperature and current-limit protection to improve the robustness of overall system, particularly in scenarios where analog signals are transmitted through wires that may be vulnerable to errors.

The SGM8433-2 fits in a small package and features low thermal resistance, which permit the transfer of high currents to loads while saving space on the circuit board. The SGM8433-2's enhanced gain-bandwidth feature enables its use as a filter component, while driving high output current. This advantage allows for a more compact design in the resolver drive signal chain by minimizing the overall footprint required. The compact design of the SGM8433-2 stands out as a significant benefit for its integration into industrial systems.

The SGM8433-2 is available in a Green TSSOP-14B (Exposed Pad) package. It is specified over the extended industrial temperature range (-40℃ to +125℃).

FEATURES

- **Wide Supply Voltage Range: 4.5V to 24V**
- **Gain-Bandwidth Product: 12MHz**
- **Slew Rate: 35V/μs**
- **Functional-Safety Feature**
- **Over-Temperature Protection**
- **Current-Limit Protection**
- **Shutdown Mode for Applications with Low I_Q**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TSSOP-14B (Exposed Pad) Package**

APPLICATIONS

Exciting Signal Driver of Resolver Primary Coil
Motor Control System
Servo Control System

SIMPLIFIED SCHEMATIC

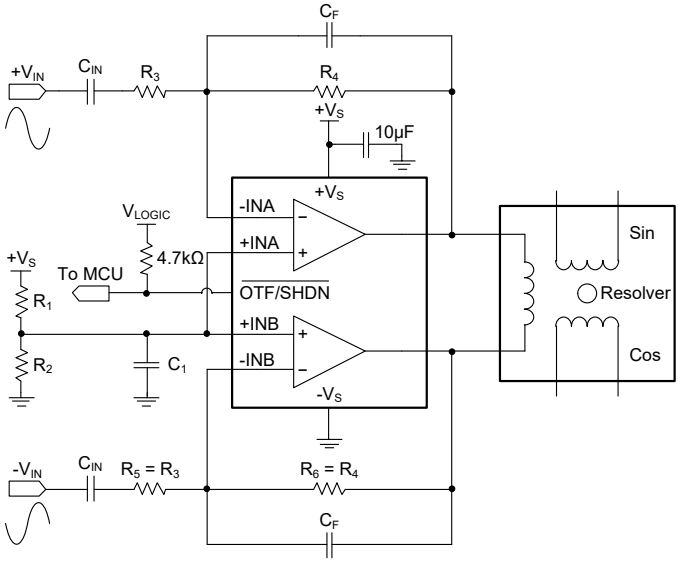


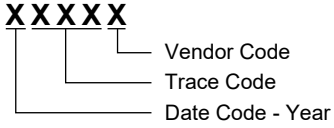
Figure 1. Simplified Schematic for Differential Input

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8433-2	TSSOP-14B (Exposed Pad)	-40℃ to +125℃	SGM8433-2XPTS14G/TR	SGM84332 XPTS14 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_S
- Single Supply 26V
- Dual Supply ..... ±13V

Signal Input Voltage Terminals
- Common Mode ..... $(-V_S)$ - 0.5V to $(+V_S)$ + 0.7V
- Differential ..... $(+V_S)$ - $(-V_S)$ + 0.2V

$\overline{OTF/SHDN}$ Pin Voltage Range, $V_{\overline{OTF/SHDN}}$
- Common Mode ..... 0V to 5.5V

Output Short-Circuit Current (1) ..... Continuous

Package Thermal Resistance
- TSSOP-14B (Exposed Pad), θ_{JA} ..... 41.9℃/W
- TSSOP-14B (Exposed Pad), θ_{JB} ..... 20.9℃/W
- TSSOP-14B (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 41.3℃/W
- TSSOP-14B (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 4.3℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (2) (3)
- HBM ..... ±8000V
- CDM ..... ±1000V

NOTES:

1. Each package contains one amplifier, which can be shorted to ground.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_S
- Single Supply ..... 4.5V to 24V
- Dual Supply ..... ±2.25V to ±12V

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

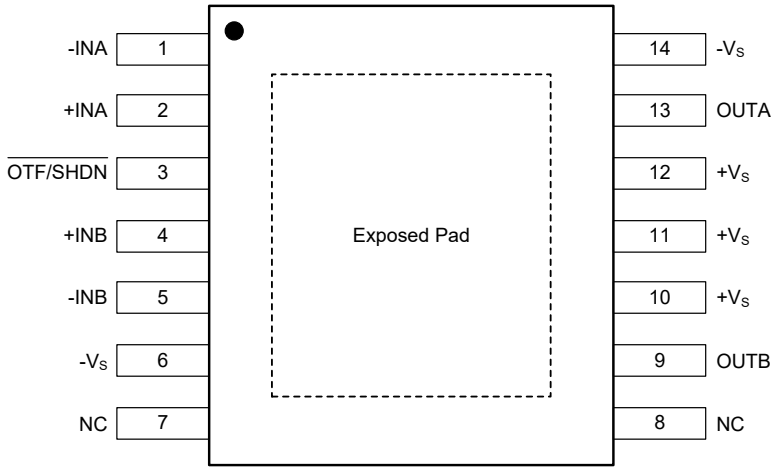
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-14B (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	-INA	I	Inverting Input of Amplifier A.
2	+INA	I	Non-Inverting Input of Amplifier A.
3	$\overline{\text{OTF/SHDN}}$	I/O	Over-Temperature Flag and Shutdown. When the $\overline{\text{OTF/SHDN}}$ pin is high (> V_{IH_OTF}), the operational amplifier is operating. When the $\overline{\text{OTF/SHDN}}$ pin is low (< V_{IL_OTF}), the operational amplifier is in shutdown mode (low I_Q state).
4	+INB	I	Non-Inverting Input of Amplifier B.
5	-INB	I	Inverting Input of Amplifier B.
6, 14	$-V_S$	—	Negative Supply. The dual negative supply points must be used and interconnected on the circuit board.
7, 8	NC	—	Not Connected.
9	OUTB	O	Output of Amplifier B.
10, 11, 12	$+V_S$	—	Positive Supply.
13	OUTA	O	Output of Amplifier A.
Exposed Pad	Exposed Pad	—	The exposed pad can be connected to $-V_S$ or left floating. Connect it to $-V_S$ plane to maximize thermal performance. Ensure that the exposed pad is exclusively connected to the $-V_S$ pin and not to any other pins.

ELECTRICAL CHARACTERISTICS

(V_S = 4.5V to 24V, V_{CM} = V_{OUT} = V_S/2, and R_L = 10kΩ connected to V_S/2, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics								
Input Offset Voltage		V_{OS}		+25℃		±1	±6	mV
				Full			±7	
Input Offset Voltage Drift		$\Delta V_{OS}/\Delta T$		Full		±5	±20	μV/℃
Input Bias Current		I_B		+25℃		±20	±300	pA
				Full			±15	nA
Input Offset Current		I_{OS}		+25℃		±20	±300	pA
				Full			±5	nA
Input Common Mode Voltage Range		V_{CM}		+25℃	$(-V_S)$ - 0.2		$(+V_S)$ + 0.2	V
Common Mode Rejection Ratio		CMRR	V_S = 4.5V, V_{CM} = $(-V_S)$ - 0.2V to $(+V_S)$ + 0.2V	+25℃	71	90		dB
				Full	68			
			V_S = 4.5V, V_{CM} = $(-V_S)$ + 2.5V to $(+V_S)$ + 0.2V	+25℃	89	112		
				Full	86			
			V_S = 24V, V_{CM} = $(-V_S)$ - 0.2V to $(+V_S)$ + 0.2V	+25℃	84	102		
				Full	81			
			V_S = 24V, V_{CM} = $(-V_S)$ + 2.5V to $(+V_S)$ + 0.2V	+25℃	109	126		
				Full	104			
Input Impedance	Differential	Z_{ID}		+25℃		20 || 0.8		MΩ || pF
	Common Mode	Z_{IC}		+25℃		0.5 || 8		GΩ || pF
Open-Loop Voltage Gain		A_{OL}	V_S = 4.5V, $(-V_S)$ + 0.5V < V_{OUT} < $(+V_S)$ - 0.5V	+25℃	94	120		dB
				Full	90			
			V_S = 4.5V, $(-V_S)$ + 1.5V < V_{OUT} < $(+V_S)$ - 1.5V, R_L = 225Ω	+25℃	86	110		
				Full	83			
			V_S = 24V, $(-V_S)$ + 0.5V < V_{OUT} < $(+V_S)$ - 0.5V	+25℃	109	134		
				Full	106			
			V_S = 24V, $(-V_S)$ + 1.5V < V_{OUT} < $(+V_S)$ - 1.5V, R_L = 225Ω	+25℃	107	128		
				Full	103			
Output Characteristics								
Output Voltage Swing from Rail			I_{OUT} = ±5mA	+25℃		20	30	mV
				Full			35	
Output Short-Circuit Current		I_{SC}	Sinking	+25℃	280	400	510	mA
			Sourcing	+25℃	230	360	500	
Power Supply								
Operating Voltage Range		V_S		Full	4.5		24	V
Power Supply Rejection Ratio		PSRR	V_S = ±2.25V to ±12V	+25℃	104	126		dB
				Full	100			
Total Quiescent Current		I_Q	I_{OUT} = 0A	Full		5	7.5	mA

ELECTRICAL CHARACTERISTICS (continued)

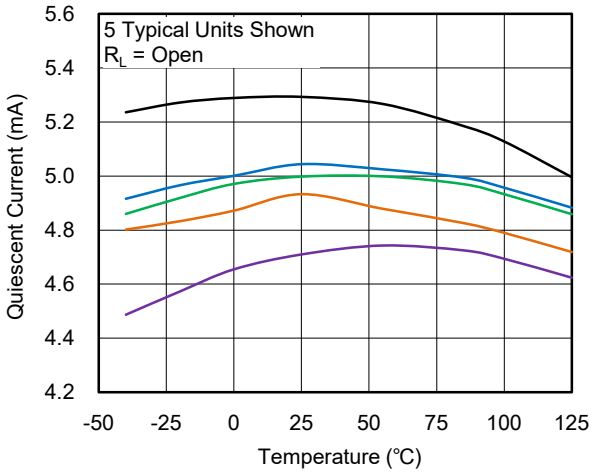
(V_S = 4.5V to 24V, V_{CM} = V_{OUT} = V_S/2, and R_L = 10kΩ connected to V_S/2, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Dynamic Performance							
Gain-Bandwidth Product	GBP		+25℃		12		MHz
Slew Rate	SR	V_S = 4.5V, 4V step, G = +1	+25℃		20		V/μs
		V_S = 24V, 10V step, G = +1	+25℃		35		
Settling Time to 0.1%	t_S	V_S = 24V, 10V step, G = +1, C_L = 10pF	+25℃		0.6		μs
		V_S = 24V, 10V step, G = -1, C_L = 10pF	+25℃		0.6		
Overload Recovery Time	ORT	V_{IN} × G > V_S	+25℃		0.1		μs
Total Harmonic Distortion + Noise	THD+N	V_S = 15V, V_{OUT} = 10V_{P-P}, G = -1, f = 10kHz, R_L = 100Ω	+25℃		100		dB
Channel Separation		f = 10kHz	+25℃		110		dB
Noise							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		5		μV_{RMS}
Input Voltage Noise Density	e_n	f = 1kHz	+25℃		60		$nV/\sqrt{Hz}$
		f = 100kHz	+25℃		20		
Input Current Noise Density	i_n	f = 1kHz	+25℃		4		$fA/\sqrt{Hz}$
Enable							
Enable High Input Voltage	V_{IH_OTF}		+25℃	1.2			V
Enable Low Input Voltage	V_{IL_OTF}		+25℃			0.5	V
Enable Hysteresis		V_S = 4.5V	+25℃		120		mV
		V_S = 24V	+25℃		180		
Enable Start-Up Time	$t_{\overline{OTF/SHDN}}$		+25℃		3		μs
Shutdown Current	I_{SD}	$V_{\overline{OTF/SHDN}}$ = 0V	+25℃		50	80	μA
Thermal Protection							
Thermal Shutdown					170		℃
Thermal Shutdown Recovery					150		℃

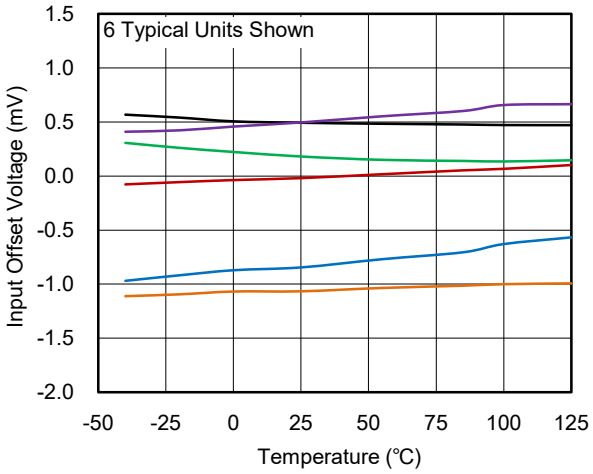
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = 24V, V_{CM} = V_S/2 and R_L = 10kΩ, unless otherwise noted.

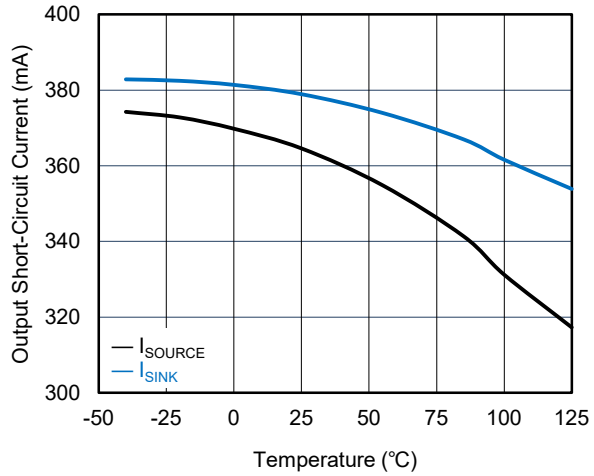
Quiescent Current vs. Temperature



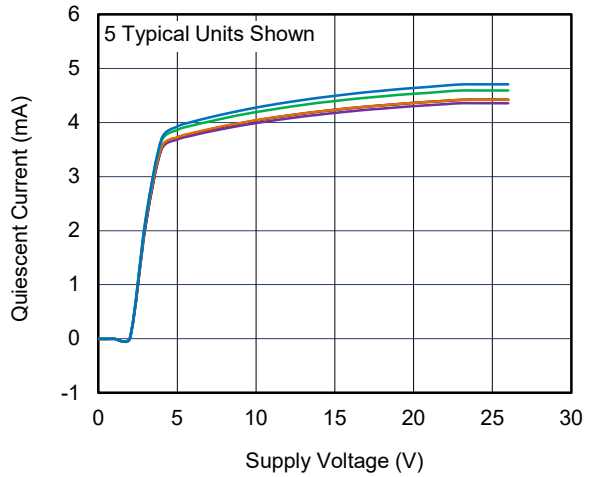
Input Offset Voltage vs. Temperature



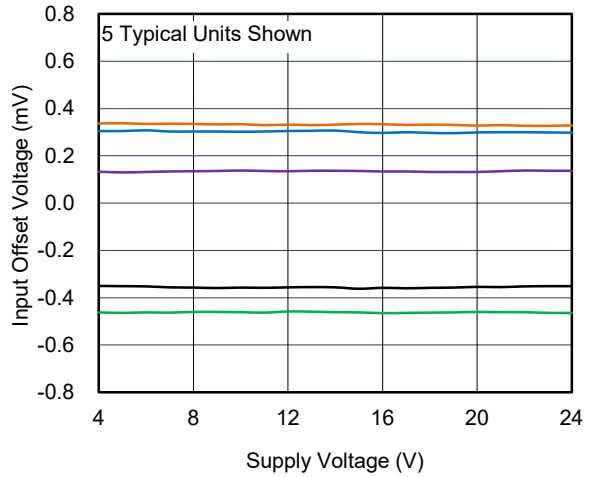
Output Short-Circuit Current vs. Temperature



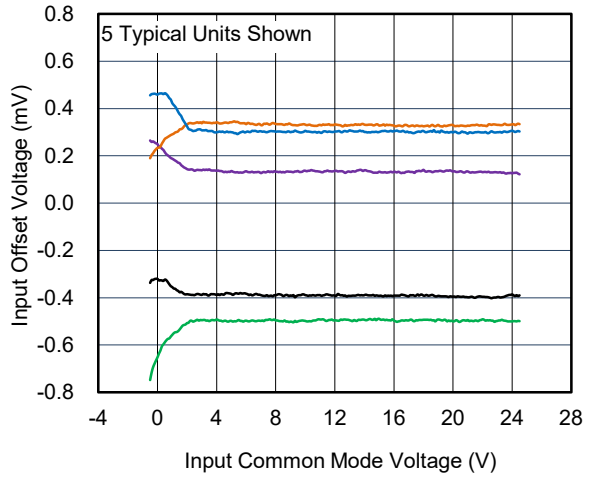
Quiescent Current vs. Supply Voltage



Input Offset Voltage vs. Supply Voltage



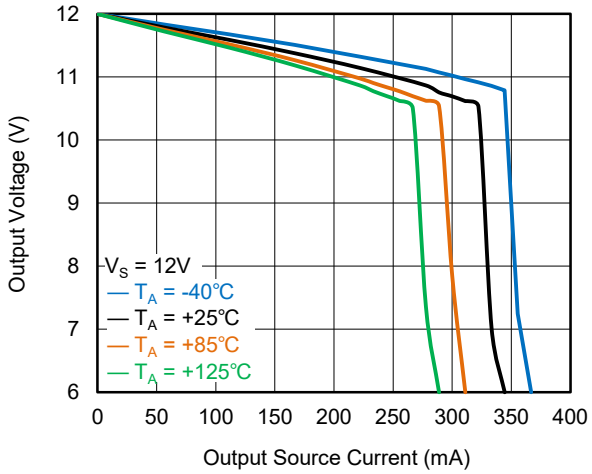
Input Offset Voltage vs. Input Common Mode Voltage



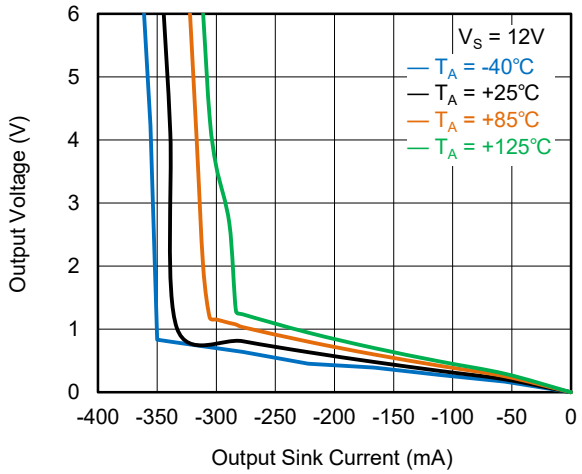
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 24V, V_{CM} = V_S/2 and R_L = 10kΩ, unless otherwise noted.

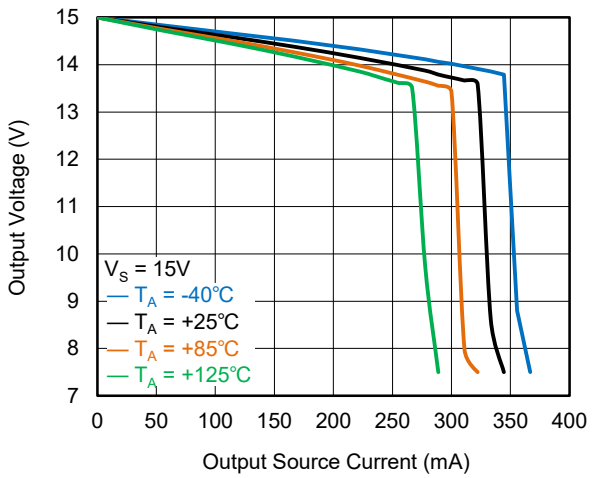
Output Voltage Swing vs. Output Source Current



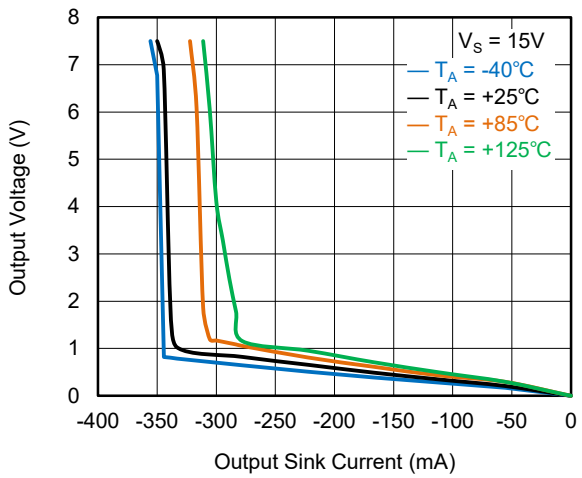
Output Voltage Swing vs. Output Sink Current



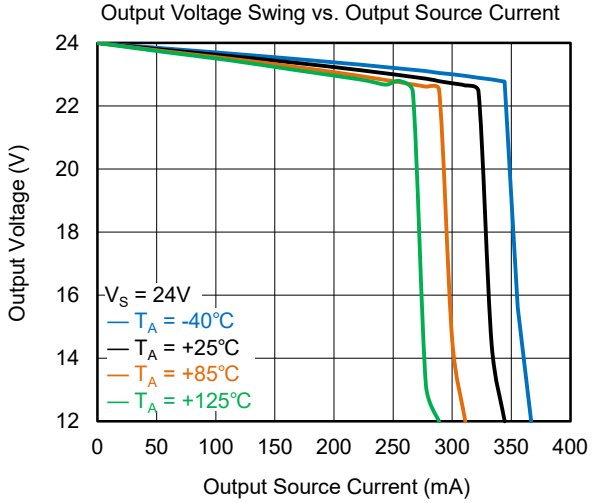
Output Voltage Swing vs. Output Source Current



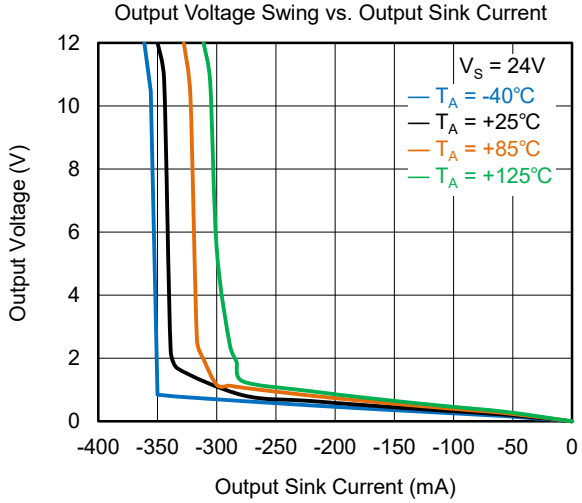
Output Voltage Swing vs. Output Sink Current



Output Voltage Swing vs. Output Source Current



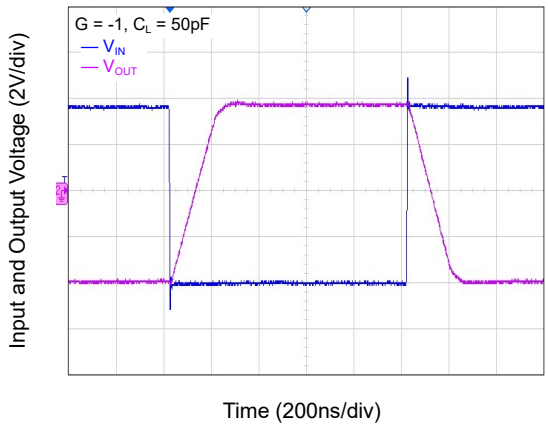
Output Voltage Swing vs. Output Sink Current



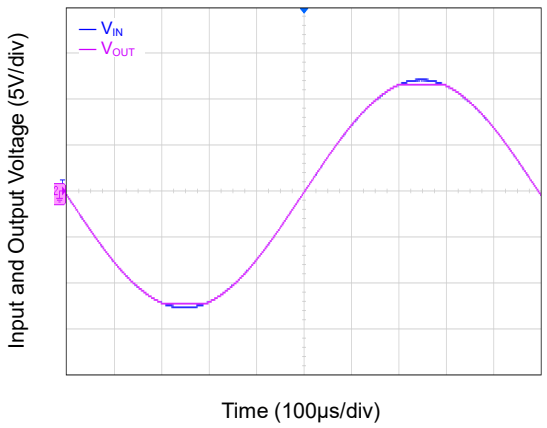
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 24V, V_{CM} = V_S/2 and R_L = 10kΩ, unless otherwise noted.

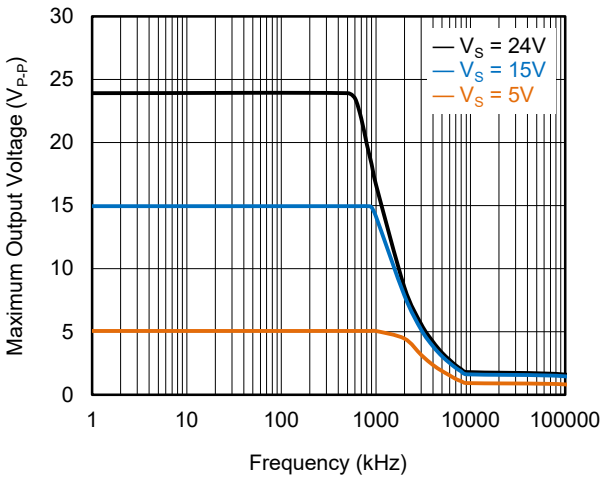
Large-Signal Step Response



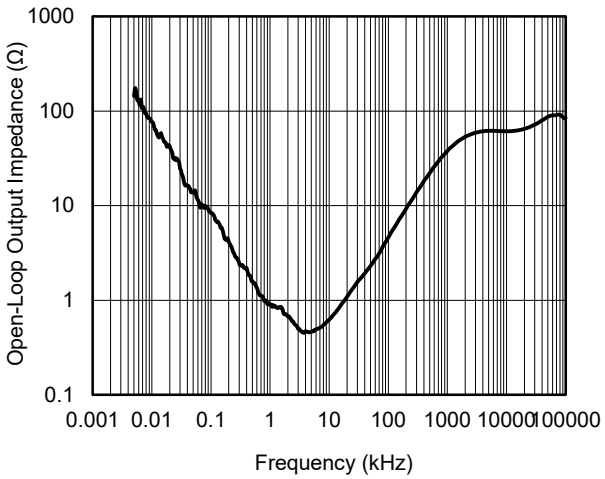
No Phase Reversal



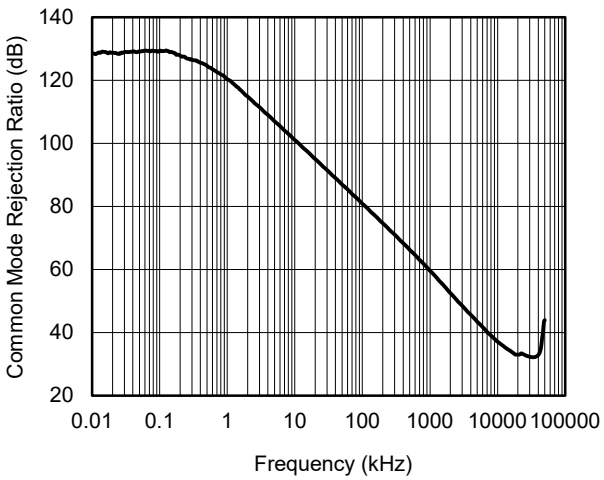
Maximum Output Voltage vs. Frequency



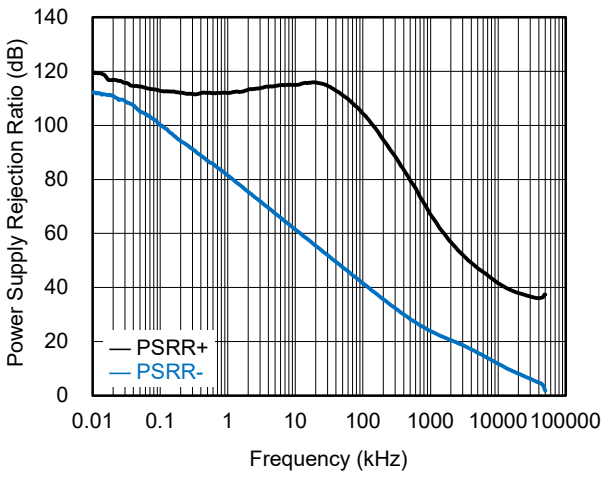
Open-Loop Output Impedance vs. Frequency



CMRR vs. Frequency



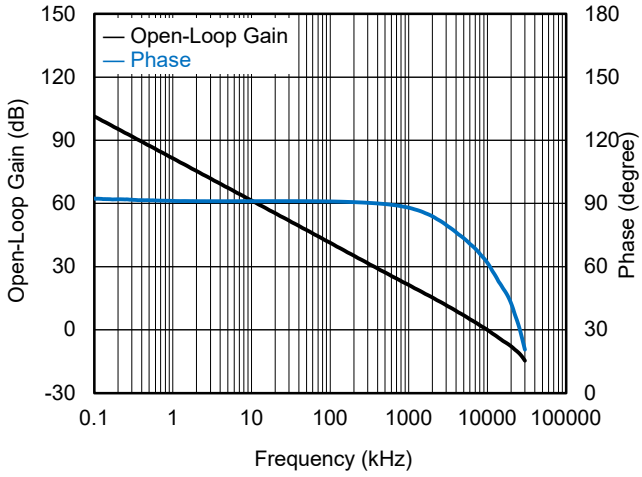
PSRR vs. Frequency



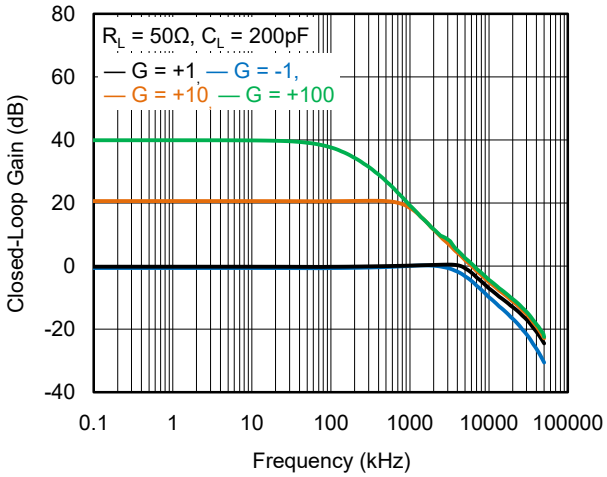
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 24V, V_{CM} = V_S/2 and R_L = 10kΩ, unless otherwise noted.

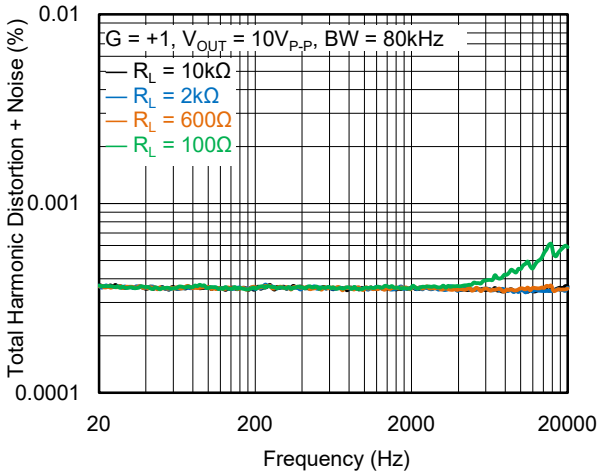
Open-Loop Gain and Phase vs. Frequency



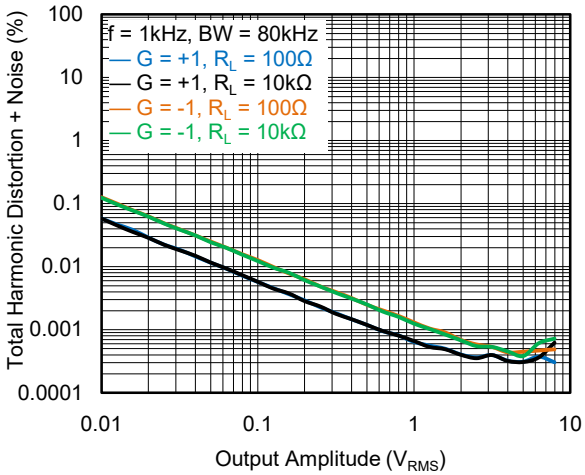
Closed-Loop Gain vs. Frequency



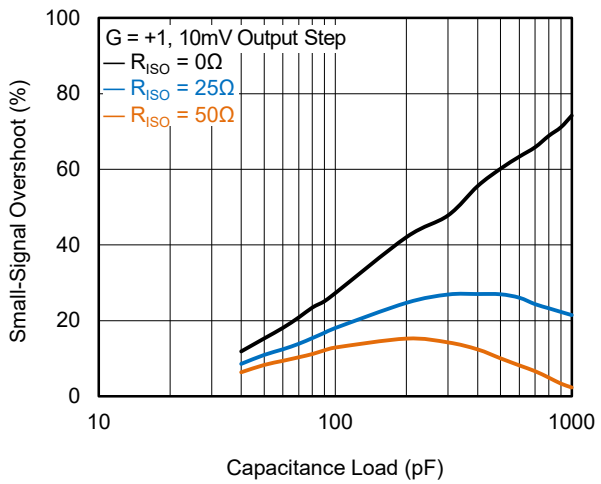
THD+N vs. Frequency



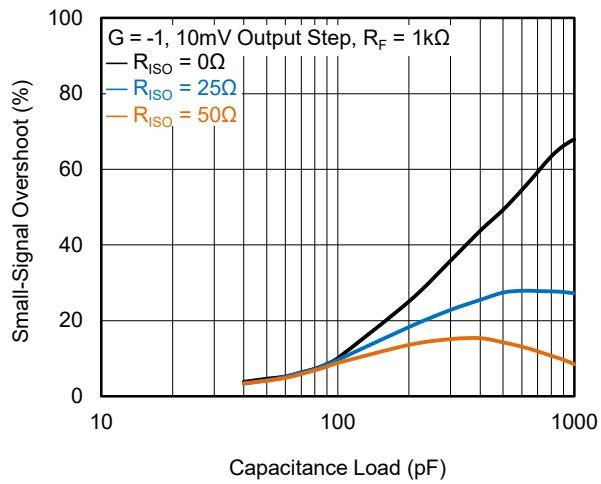
THD+N vs. Output Amplitude



Small-Signal Overshoot vs. Capacitive Load



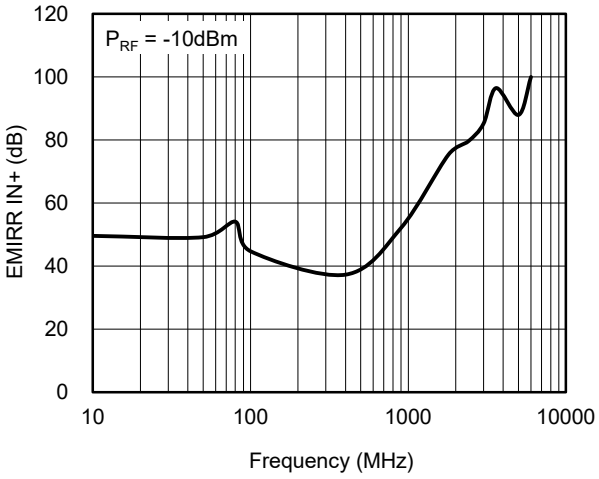
Small-Signal Overshoot vs. Capacitive Load



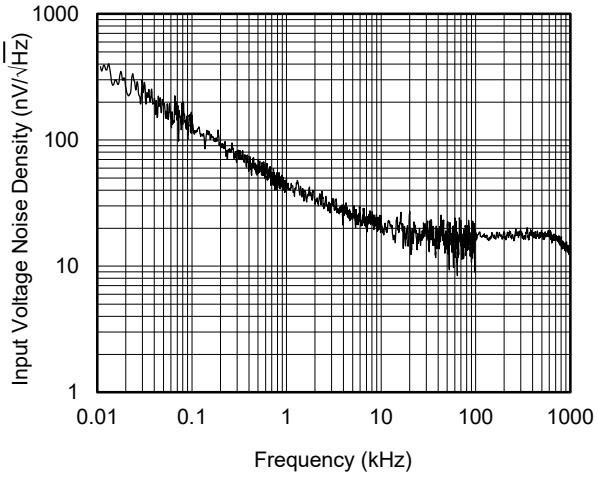
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 24V, V_{CM} = V_S/2 and R_L = 10kΩ, unless otherwise noted.

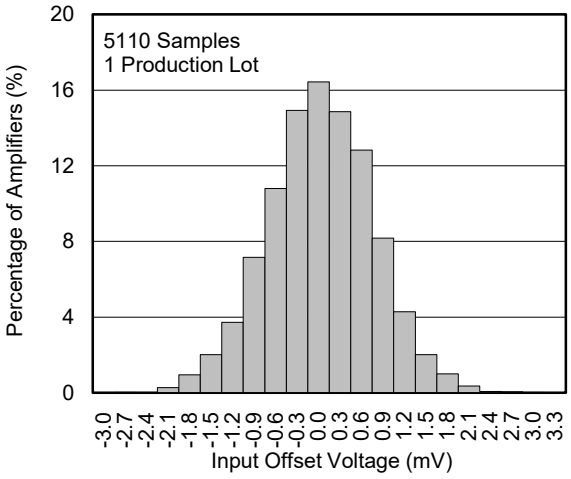
EMIRR IN+ vs. Frequency



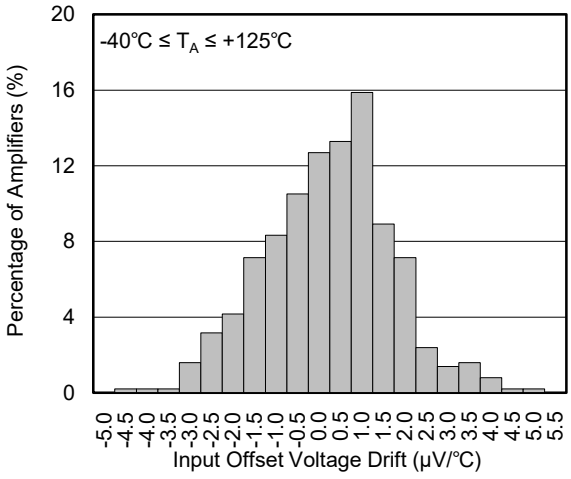
Input Voltage Noise Density vs. Frequency



Input Offset Voltage Production Distribution



Input Offset Voltage Drift Distribution



FUNCTIONAL BLOCK DIAGRAM

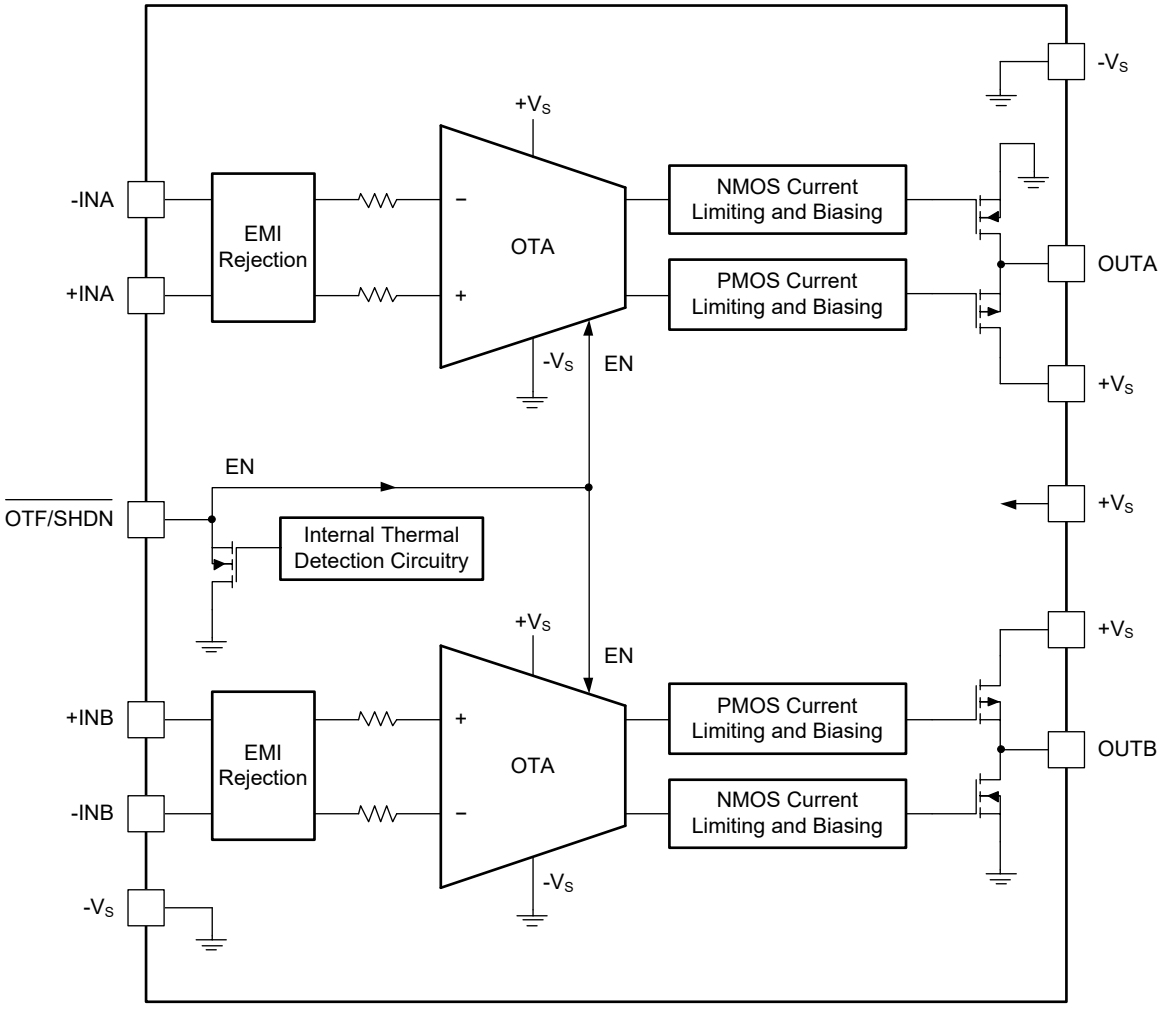


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM8433-2 is a high performance operational amplifier that supports dual-power supply, rail-to-rail input and output, and has high output current drive capability. The device also comes with shutdown control, over-temperature and current-limit protection functions, which is specifically designed for applications involving resolvers.

Input and Output Range

The SGM8433-2 supports rail-to-rail input and output. The input common mode range is from ($-V_S$) - 0.2V to ($+V_S$) + 0.2V. To achieve normal output performance in application, it is necessary to ensure that the input signal does not exceed this specification. If the input signal exceeds the limit, it can cause distortion and nonlinearities; in severe cases, it can lead to the device damage.

The SGM8433-2 has high current output capability and low output voltage swing from rail. The typical output voltage swing from rail is 20mV under the condition of ±5mA output current. This makes the SGM8433-2 suitable for applications that require low output voltage swing from rail.

Over-Temperature and Shutdown Function

The SGM8433-2 is designed with over-temperature protection and a shutdown control ($\overline{\text{OTF/SHDN}}$) pin. This pin is a dual function pin. When the $\overline{\text{OTF/SHDN}}$ pin is pulled low, the SGM8433-2 enters shutdown mode, and the device's quiescent current is as low as 50μA (typical value at +25℃). In shutdown mode, all output pins of the operational amplifier maintain a high-impedance state. When the $\overline{\text{OTF/SHDN}}$ pin is pulled high, the SGM8433-2 is enabled, and the operational amplifier can operate normally.

The SGM8433-2 defaults to shutdown mode when the $\overline{\text{OTF/SHDN}}$ pin is floating, if users want to enable the device, the $\overline{\text{OTF/SHDN}}$ pin must be pulled high through an external pull-up resistor. Table 1 summarizes the control logic of the $\overline{\text{OTF/SHDN}}$ pin. In addition, it should be noted that the absolute maximum rating for the $\overline{\text{OTF/SHDN}}$ pin is 5.5V relative to $-V_S$ pin, so users should exercise caution when operating it.

Table 1. $\overline{\text{OTF/SHDN}}$ Shutdown Control

$\overline{\text{OTF/SHDN}}$ Pin	SGM8433-2 State
High (> V_{IH_OTF})	Enabled and Operating
Low (< V_{IL_OTF})	Shutdown Mode

The $\overline{\text{OTF/SHDN}}$ pin's another function is used to indicate over-temperature protection events. This pin defaults to being pulled high. When the over-temperature event occurs and the junction temperature of SGM8433-2 exceeds the limit value, the $\overline{\text{OTF/SHDN}}$ pin will actively become low and all outputs of the operational amplifier will enter a high-impedance state.

Thermal Shutdown

The SGM8433-2 design has a thermal shutdown (TSD) function. The device enters a shutdown state when the internal junction temperature exceeds the shutdown threshold of +170℃. In thermal shutdown mode, the output current is cut off, and the output pin remains in a high-impedance state. The SGM8433-2 has a thermal shutdown hysteresis temperature of 20℃. The device will automatically recover from TSD mode once the junction temperature drops to +150℃. In application, the SGM8433-2 should be operated at a junction temperature below +150℃, and the exposed pad should be connected to a larger ground plane to maximize thermal performance.

Current-Limit

The SGM8433-2 design has an output current-limit function that activates when overload events happen. The output source and sink current limits are 360mA (TYP) and 400mA (TYP), respectively. In application, the die temperature rises rapidly if the SGM8433-2 remains in current limitation for an extended period. This situation may cause the chip to enter thermal shutdown. Therefore, it is necessary for users to evaluate whether the SGM8433-2's output current can meet the normal operating requirements when designing circuits. It should be noted not to operate the equipment continuously under thermal hysteresis for a long time, as this behavior may cause irreversible damage to the device.

DETAILED DESCRIPTION (continued)

Input and Output Protection

The SGM8433-2 incorporates internal ESD protection circuits on both input and output pins, and equivalent input and output circuit is illustrated in the following figure.

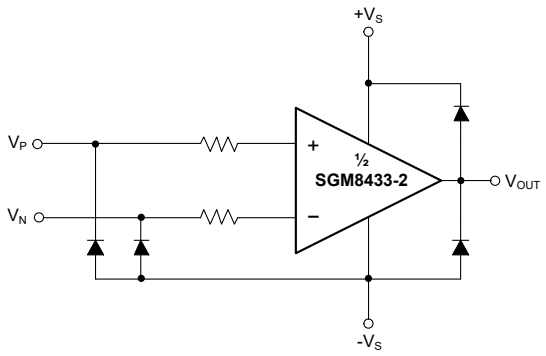


Figure 3. Equivalent Input and Output Circuit

For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power supply pins. Therefore, it is crucial to keep the input voltage below the maximum rating and limit the input current to less than 10mA.

In addition, the SGM8433-2 supports large differential voltage inputs within the power supply range, making it suitable for use as a comparator in some applications.

Capacitive Load and Stability

The SGM8433-2 is designed for driving the 100pF capacitive load with unity-gain stable. If greater capacitive load must be driven in application, the circuit in Figure 4 can be used. In this circuit, the IR drop voltage generated by R_{ISO} is compensated by feedback loop.

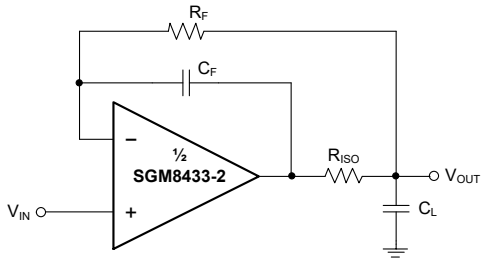


Figure 4. Circuit to Drive Heavy Capacitive Load

For the buffer circuit, another simpler compensation is shown in Figure 5. This method, called out-of-the-loop compensation, primarily uses a resistor to isolate the output pin and feedback network from the capacitive load. Functionally, it introduces a zero in the transfer function of the feedback network, which reduces the loop phase shift at higher frequencies. This method is effective, but the R_{ISO} will bring an IR drop voltage, so choosing an appropriate resistance value is crucial in actual applications. The selection of R_{ISO} can refer to the Small-Signal Overshoot vs. Capacitive Load.

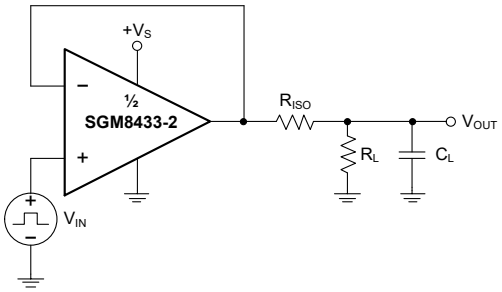


Figure 5. Circuit to Drive Capacitive Load

Power Supply Bypassing and Layout

Power supply pins are actually inputs to the amplifiers. Care must be taken to provide the amplifiers with a clean, low noise DC voltage source. Power supply bypassing is employed to provide a low-impedance path to ground for noise and undesired signals at all frequencies. This cannot be achieved with a single capacitor type; however, with a variety of capacitors in parallel, the bandwidth of power supply bypassing can be greatly extended. The bypass capacitors have two functions:

◆ Provide a low-impedance path for noise and undesired signals from the supply pins to ground.

◆ Provide local stored charge for fast switching conditions and minimize the voltage drop at the supply pins during transients. This is typically achieved with large electrolytic capacitors.

DETAILED DESCRIPTION (continued)

Good quality ceramic chip capacitors should be used and always kept as close as possible to the amplifier package. A parallel combination of a 0.1μF ceramic and a 10μF electrolytic capacitor covers a wide range of rejection for unwanted noise. The 10μF capacitor is less critical for high-frequency bypassing, and in most cases, one per supply line is sufficient. The values of capacitors are circuit-dependent and should be determined by the system's requirements.

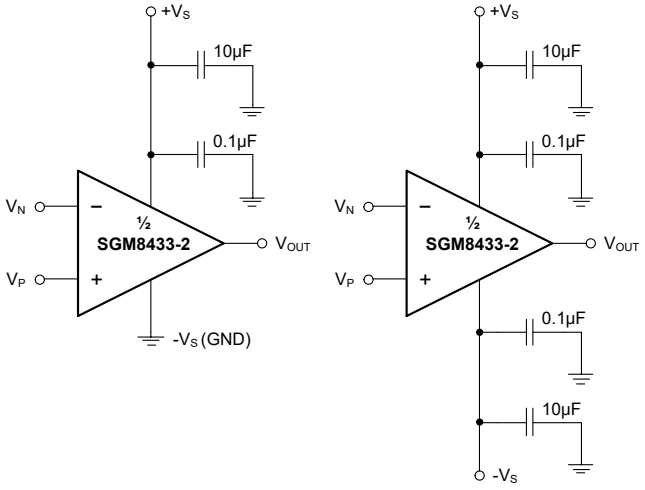


Figure 6. Amplifier with Bypass Capacitors

APPLICATION INFORMATION

The SGM8433-2 is a dual CMOS operational amplifier featuring rail-to-rail output, high voltage and high output drive. It operates within a wide voltage range of 4.5V to 24V, offers a high continuous output current of 230mA (MIN), and is available in a TSSOP-14B (Exposed Pad) package that provides efficient heat dissipation. These characteristics make the SGM8433-2 highly suitable for applications requiring both high operating voltage and high output current.

The SGM8433-2 has output current limit and thermal shutdown (TSD) functions. It can be flexibly applied to a resolver excitation circuit. The following chapter provides more detailed descriptions.

Resolver Excitation Circuit

The SGM8433-2's high continuous output current function makes it very suitable for resolver excitation circuit. Figure 7 shows the typical resolver excitation circuit using the SGM8433-2 and the SGM8212-1. This circuit includes two SGM8212-1s: one is used to provide a bias voltage buffer and the other is used as an inverting amplifier to obtain a signal with phase reversal.

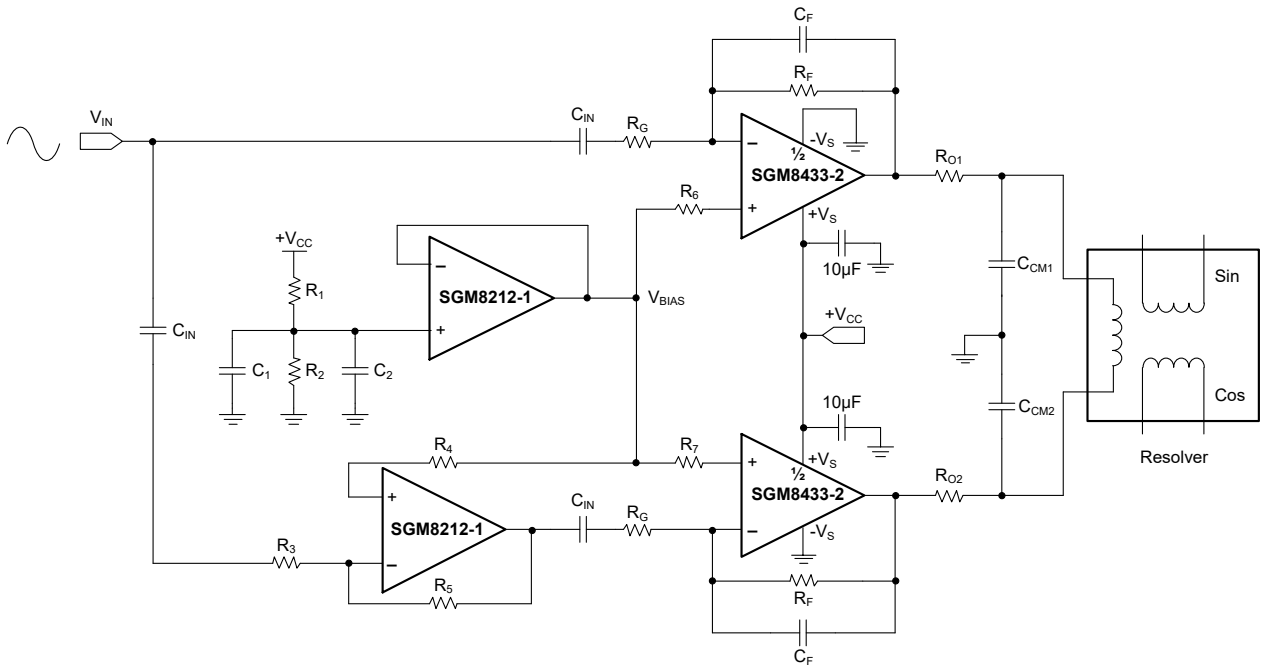


Figure 7. Resolver Excitation Circuit with SGM8212-1

APPLICATION INFORMATION (continued)

Figure 8 shows a simplified resolver excitation circuit without SGM8212-1. Its bias voltage is provided by a resistance voltage divider, and the input signal is a differential signal with a phase difference of 180 degrees.

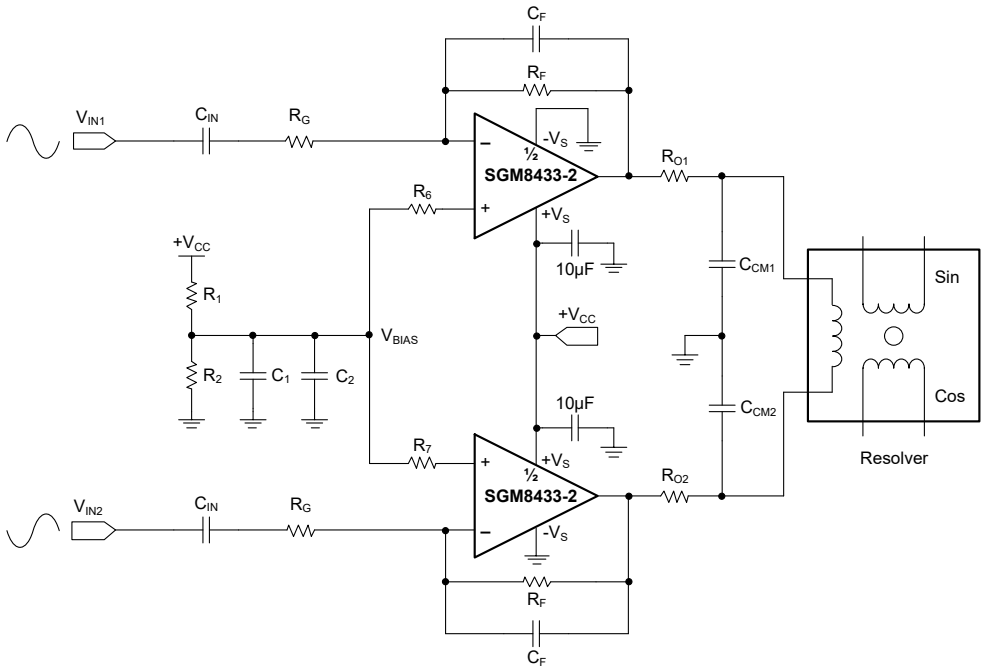


Figure 8. Simplified Resolver Excitation Circuit without SGM8212-1

Figure 9 shows a resolver excitation circuit with a pulse-width modulation (PWM) signal as the input. In this circuit, the SGM8212-1 is used as a buffer and provides the bias voltage. Two input PWM signals from the I/O pins of the microcontroller are filtered by a two-stage RC filter circuit and converted to a sine wave signal for use as an excitation input.

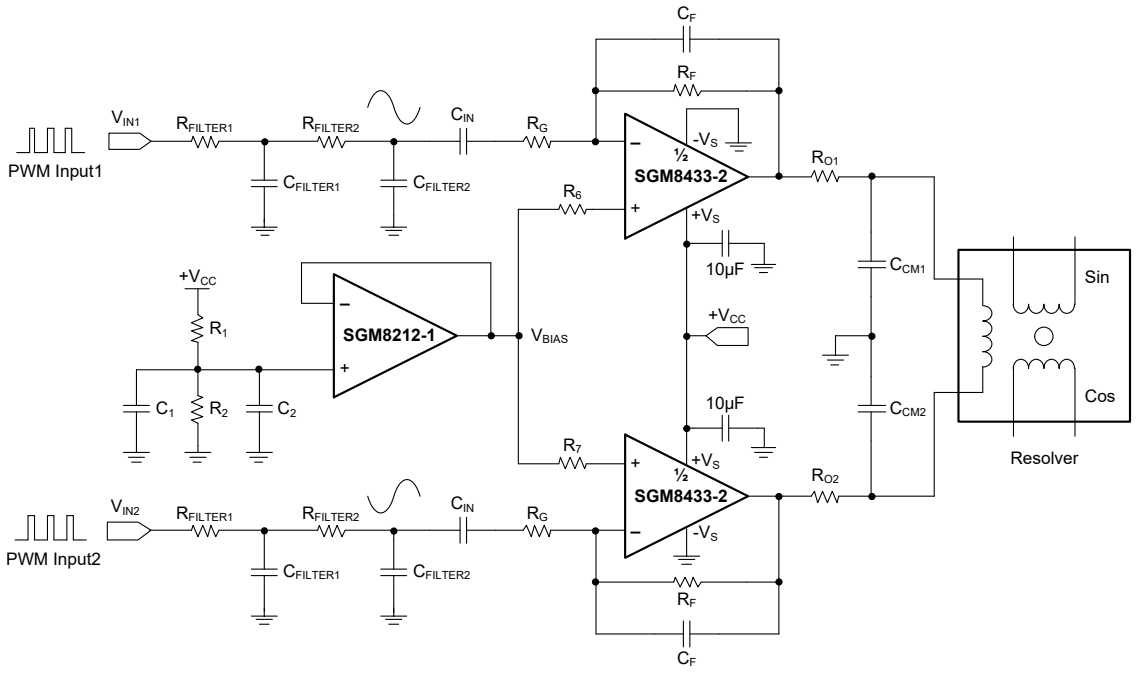


Figure 9. Resolver Excitation Circuit from PWM Input Signal

APPLICATION INFORMATION (continued)

Figure 10 shows the actual output waveform from a resolver excitation circuit, and the key circuit parameter design is shown in Table 2.

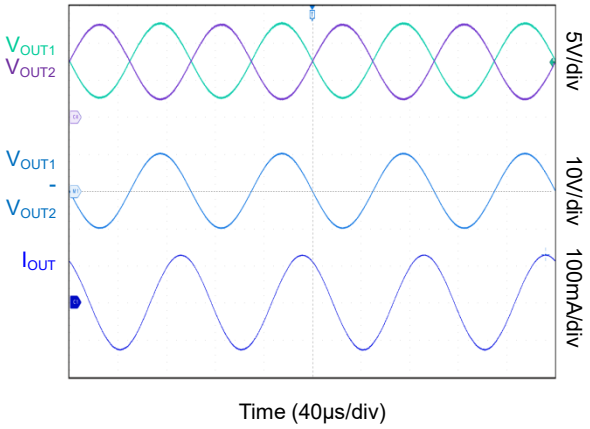


Figure 10. Actual Output Waveform from Resolver Excitation Circuit (+V_S = 15V, -V_S = 0V, f = 10kHz)

Table 2. Design Parameters

Design Parameter	Example Value
Ambient Temperature Range	-40℃ to +125℃
Supply Voltage	+15V
V_{BIAS}	+7.5V from SGM8212-1
R_O	0Ω
C_{CM}	No Connect
Gain	2.5V/V
Input Signal Frequency	10kHz
Resolver Excitation Input Voltage	$8V_{P-P}$
Resolver Excitation Output Voltage	$20V_{P-P}$
Output Current with Resolver Equivalent Circuit	$\pm130mA_{P-P}$

Figure 11 and Figure 12 respectively show the output voltage and the output current of the resolver excitation circuit.

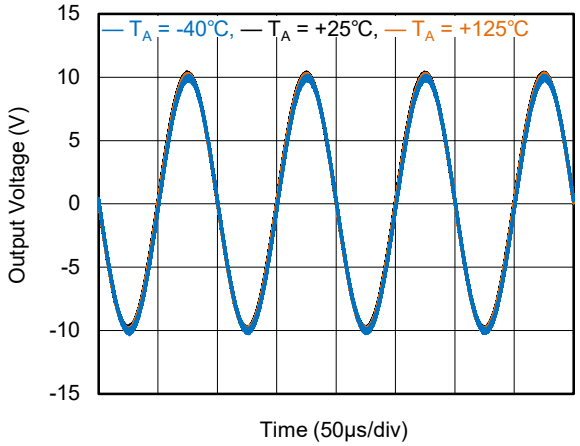


Figure 11. Output Voltage of Resolver Excitation Circuit

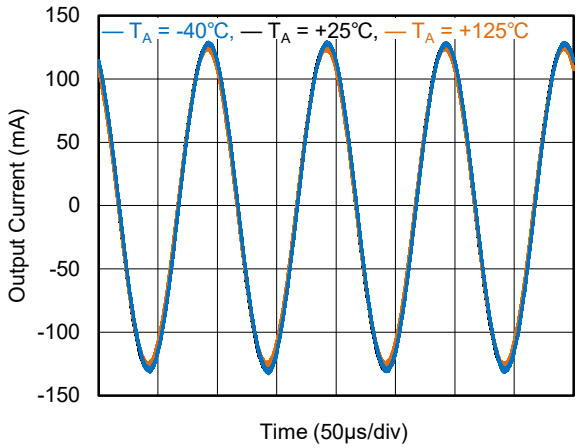


Figure 12. Output Current of Resolver Excitation Circuit

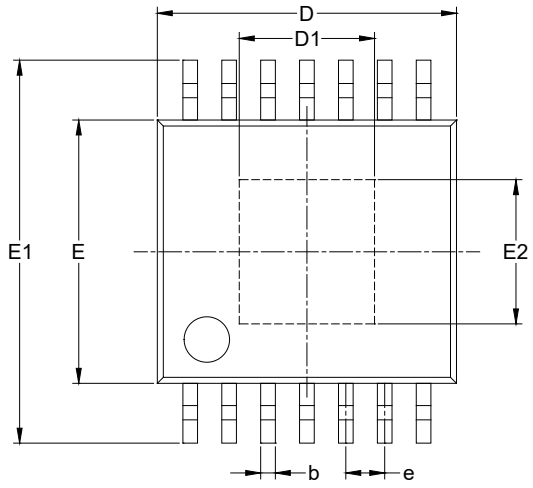
REVISION HISTORY

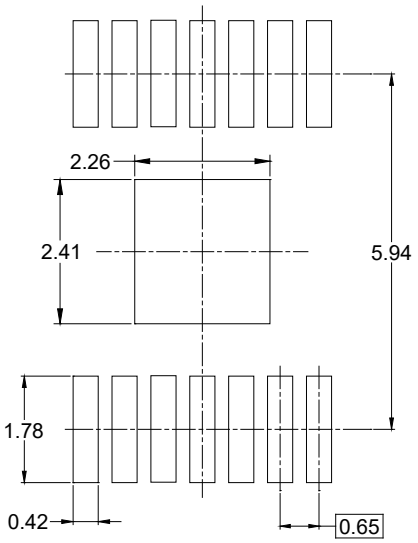
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

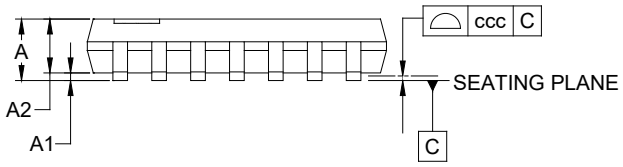
PACKAGE OUTLINE DIMENSIONS

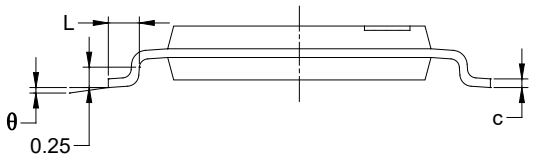
TSSOP-14B (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)



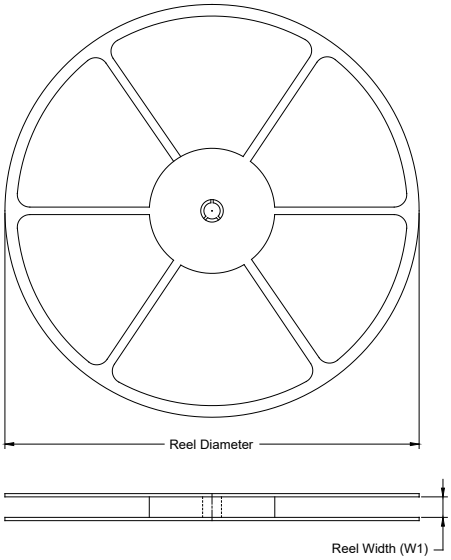


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.000	-	0.150
A2	0.800	-	1.150
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
D1	2.060	-	2.460
E	4.300		4.500
E1	6.200	-	6.600
E2	2.210	-	2.610
e	0.650 BSC		
L	0.450	-	0.750
θ	0°	-	8°
ccc	0.100		

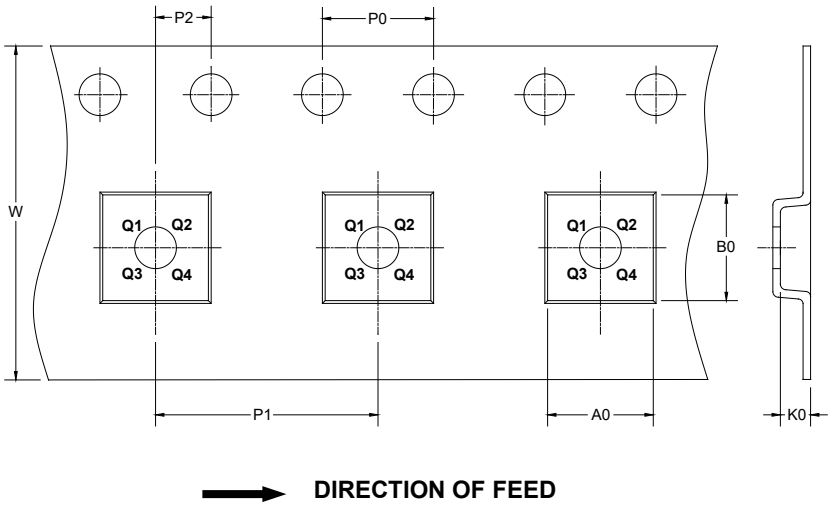
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



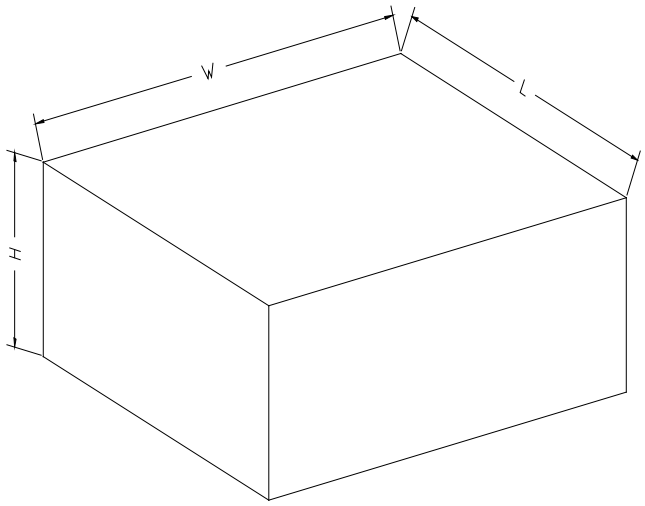
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14B (Exposed Pad)	13″	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002