SC81442, 36V/4A, High Efficiency Buck Converter

1 Descriptions

The SC81442 is a synchronous Buck converter with a wide input voltage range from 3V to 36V, providing 4A current capability options. The converter regulates the output voltage at customized voltage through setting the divider resistors. It also provides highly efficiency output current and fast loop response with current mode control.

The SC81442 is specifically designed for universal applications. The device integrates user-optional spread spectrum. The switching frequency can also be synchronized to external clock through multiplexing EN/SYNC pin. For fixed frequency parts, a power good function is available by the PG pin. For better thermal performance, SOP-8 package with a thermal pad is available. In addition, the device incorporates highly efficient PFM mode.

The SC81442 employs both peak current limit and valley current limit to help protect the device from overload as well as provides short-period heavy current capability. It also provides thermal shutdown, input UVLO, output short-circuit protection to enable systematical robust operation.

2 Features

- 3.5V to 36V start up input voltage, supporting 3.0V falling V_{IN}
- APFM mode at light load
- Spread-spectrum function for low EMI
- 400kHz, 1400kHz, and 2.1MHz can be selected
- The power good function to remove external supervisor or reset circuit is available
- Switching frequency can be synchronized between 200kHz and 2.2MHz by external clock
- Adjustable output voltage through FB pin
- ESOP package for better thermal performance
- Output OCL / SCP / OVP, TSD, and input UVLO protections
- Pin-to-Pin compatible with
  - SC81410 (Industrial, 36V/1A)
  - SC81420 (Industrial, 36V/2A)
  - SC81430 (Industrial, 36V/3A)

3 Applications

- General purpose wide VIN powers
- Factory and building automation systems:
- Industrial & Consumer applications

4 Device Information

ORDER NUMBER	OUTPUT VOLTAGE	MODE IN LIGHT LOAD	SPREAD SPECTRUM	PACKAGE	SWITCHING FREQUENCY	PG OR RT Function	Current Limit	BODY SIZE
SC81412SEER	Adjustable	APFM	Yes	ESOP-8	400k	PG	1A	5mm×4mm
SC81422SEER	Adjustable	APFM	Yes	ESOP-8	400k	PG	2A	5mm×4mm
SC81432SEER	Adjustable	APFM	Yes	ESOP-8	400k	PG	3A	5mm×4mm
SC81442SEER	Adjustable	APFM	Yes	ESOP-8	400k	PG	4A	5mm×4mm

5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Date	Page(s) changed	Changes Description
V0.1.6	2024/6/3		Initial version

6 Typical Application Circuit

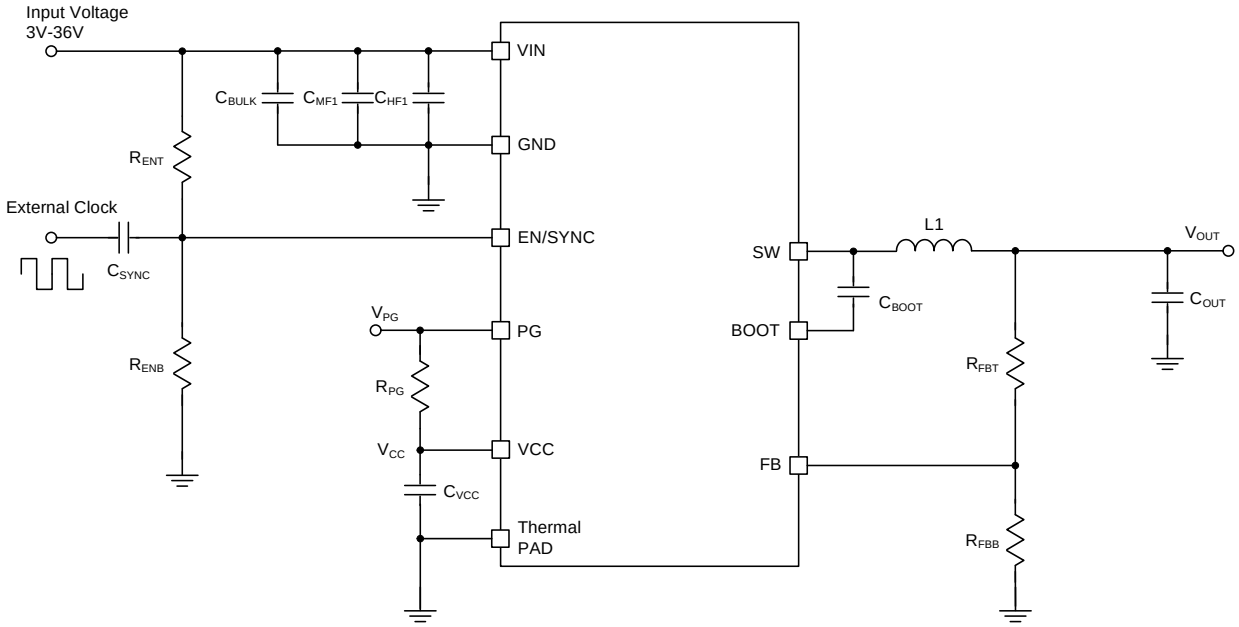
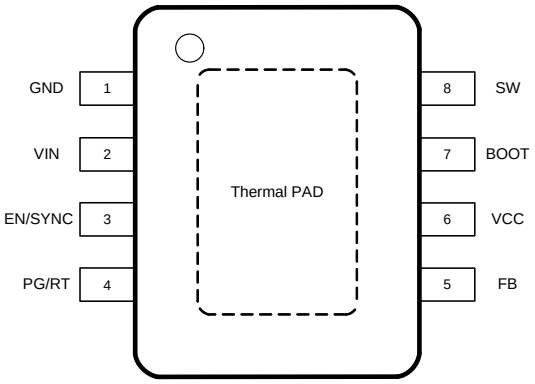


Figure 6-1. Typical Application Circuit of SC81442

7 Terminal Configuration and Functions

TOP VIEW (SOP-8)



SC81442

PIN TERMINAL		I/O	DESCRIPTION
PIN NUM	NAME		
1	GND	G	System ground. Connect a high-quality bypass capacitor or capacitors from this pin to VIN.
2	VIN	I	Input supply to the converter. Connecting a high-quality bypass capacitor or capacitors from this pin to GND is critical.
3	EN/SYNC	I	Precision enable input. High = on, Low = off. Can be used as an adjustable UVLO. Also functions as a synchronization input pin. Triggers on rising edge of external clock. A capacitor must be used to AC couple the synchronization signal to this pin. This pin cannot be floating and must be properly terminated.
4	PG	I/O	This pin acts as open-drain power-good status output. Pull this pin up to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault.
5	FB	I	Output voltage feedback input to the internal control loop. Connect to feedback divider tap point for adjustable output voltage. For fixed output voltage versions, connect FB directly to output.
6	VCC	O	Internal 5-V LDO output. Used as supply to internal control circuits. Connect a high-quality 1-μF capacitor from this pin to AGND. The VCC pin can be used as logic pull-up supply for PG flag.
7	BOOT	O	High-side driver upper supply rail. Connect a 100-nF capacitor between SW pin and BOOT. An internal diode connects BOOT to VCC and allows BOOT to charge while SW node is low.
8	SW	O	Switch node of the converter.
Thermal Pad		G	Thermal pad. This pin must be connected to a solid GND plane on PCB for better thermal performance and anti-noise performance.
I=Input, O=Output, G=Ground			

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals (2)	VIN to AGND, PGND	-0.3	42	V
	EN/SYNC to AGND, PGND	-0.3	42	V
	BOOT to SW	-0.3	5.5	V
	All other pins	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-40	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) (2)	-2500	2500	V
	Charged device model (CDM) (3)	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	3.0		36	V
V_{OUT}	Output voltage range	1		0.95×V_{IN}	V
F_{SW}	Switching Frequency Range		400		kHz
I_{OUT}	Output DC current range	0		4	A
T_J	Operating junction temperature	-40		150	°C
T_A	Operating ambient temperature range	-40		125	°C

8.4 Thermal Information

THERMAL RESISTANCE		QFN-12 3mm x 2mm	SOP-8 4mm x 5mm	UNIT
Θ_{JA}	Junction to ambient thermal resistance (Southchip EVM) (1)	65	40	°C/W
	Junction to ambient thermal resistance (JESD 51-7) (2)	75	45	°C/W
$\Theta_{JC(top)}$	Junction to case (top) resistance (2)	40	54	°C/W

(1) Measured on Southchip EVM (4-layer, 2-oz Cu per top and bottom layer and 1-oz Cu per inner layer).

(2) Simulated on JESD51-7, 4-layer PCB.

8.5 Electrical Characteristics

Minimum and maximum value is tested at T_J = -40°C to 150°C, V_{IN} = 13.5V. Typical value is tested at T_J = 25°C, V_{IN} = 13.5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		3.0		36	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising		3.3	3.5	V
		V_{IN} falling		2.78	3.0	V
I_Q	Quiescent current into the VIN pin	V_{FB} = 105%×V_{REF}		48		μA
I_{SD}	Shutdown current into the VIN pin	V_{EN} = 0V		2		μA
V_{CC}	Internal regulator output	6V ≤ V_{IN} ≤ 36V	4.75	5	5.25	V
V_{CC_UVLO}	V_{CC} under voltage lockout threshold	V_{CC} rising		2.2		V
		V_{CC} falling		2.0		V
EN						
V_{EN_VCC}	EN input level to turn on internal LDO		0.4			V
V_{EN_H}	EN input level to start switching	Rising threshold	1.14	1.19	1.25	V
V_{EN_HYS}	Enable threshold hysteresis			300		mV
t_{BLK}(1)	Blanking of EN after rising edges		10		35	μs
	Blanking of EN after falling edges		10		100	
SOFT START						
t_{SS}	Time for V_{REF} from 10% to 90%		3.0	4.5	6.0	ms
MOSFETS						
R_{DSON}	High-side MOSFET on resistance	SOP-8		85		mΩ
	Low-side MOSFET on resistance	SOP-8		65		mΩ
V_{BOOT_UVLO}	Voltage on BOOT pin compared to SW which will turn off high-side switch	V_{BOOT} falling		1.78		V
FEEDBACK						

V_{FB}	FB reference voltage	VIN = 3.5 - 36V, T_J = 25°C	0.995	1	1.005	V
		VIN = 3.5 - 36V	0.98	1	1.02	V
I_{FB}	Input current from FB to AGND			1		nA
CURRENT LIMIT						
I_{L-HS}	High side switch current limit		3.85	4.5	5.05	A
I_{L-LS}	Low side switch current limit		2.9	3.5	4.1	A
I_{PK_MIN}	Minimum peak inductor current	PFM mode		0.85		A
I_{L-ZC}	Zero-cross current limit. Current sourcing out of SW pin			0.10		A
I_{L-NEG}	Negative current limit in FPWM and SYNC Modes. Current sinking into SW pin			2		A
HICCUP MODE						
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage	Not included in soft start		40		%
T_{HICCUP_ON}	Hiccup on Timer			10		ms
T_{HICCUP_OFF}	Hiccup off Timer			80		ms
POWER GOOD						
$V_{PG\_OV\_R}$	PGOOD upper threshold - rising	% of VOUT setting	105	107	109	%
$V_{PG\_UV\_F}$	PGOOD lower threshold - falling	% of VOUT setting	92	94	96	%
V_{PG_HYS}	PGOOD hysteresis	% of VOUT setting		2		%
$V_{IN(PG\_VALID)}$	Input voltage for proper PGOOD function				2	V
$V_{PG(LOW)}$	Low level PGOOD output voltage	I_{SINK} = 1mA		0.1	0.3	V
I_{OV}	Discharge current at the SW node under OVP condition			1		mA
$t_{PGD\_DLY(rising)}$	Delay for the PGOOD signal from low to high			2		ms
$t_{PGD\_DCH(falling)}$	Deglitch time for PGOOD signal from high to low			50		μs
OSCILLATOR						
f_{SW}	Switching frequency	400kHz switching frequency setting	360	400	440	kHz
SPREAD SPECTRUM						
F_{SS}	Frequency span of spread spectrum operation - deviation from center frequency	Spread spectrum active	-11		11	%
F_{PSS}(1)	Spread spectrum pattern cycles			256		
PWM LIMITS						

t_{ON_MIN}	Minimum HS switch on time	SOP-8		65	108	ns
t_{ON_MAX}	Maximum HS switch on time			10		μs
t_{OFF_MIN}	Minimum LS switch on time			80	110	ns
SYNCHRONOUS CLOCK						
V_{EN_SYNC}	Minimum sync clock amplitude voltage necessary to sync using EN/SYNC pin				3.1	V
t_{SYNC_MIN}	Minimum sync clock pulse width				135	ns
t_{SYNC_R}	Maximum sync clock rising time		30			ns
t_{SYNC_F}	Maximum sync clock falling time		30			ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	T_J rising	150	165	175	°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

(1) Guarantee by Design

9 Functional Block Diagram

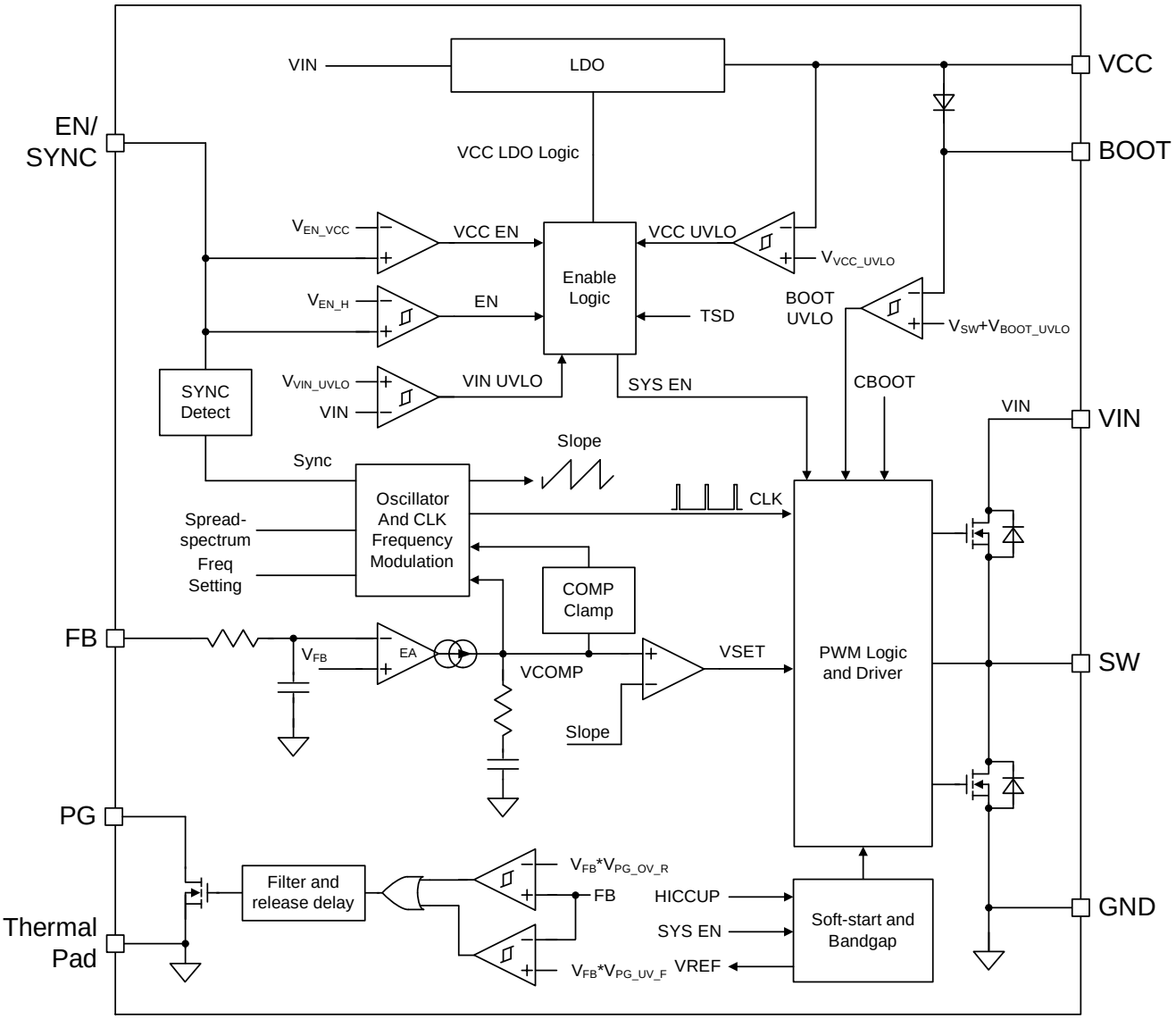


Figure 9-1. SC81442 Functional Block Diagram

10 Feature Description

10.1 Overview

SC81442 is a wide input, 4A, synchronous Buck converter for universal applications. Implementing peak-current mode control, SC81442 is able to operate over a wide range of conversion ratio with excellent line and load transient performance. In addition, internal slope compensation increases integration and helps maintain loop stability. The converter can also operate from 200kHz to 2.2MHz switching frequency with external clock synchronization capability. Device's input can vary from 36V down to 3V, resulting in device entering minimum-on time or minimum-off time operation. Through adaptively extending switching cycle, SC81442 can still maintain output voltage regulation.

The device benefits applications which have stringent requirement for low EMI. Although very high efficiency, DC/DC converters are naturally ideal EMI source. SC81442 is specifically designed to optimize EMI performance through different ways. Incorporating spread spectrum, SC81442 can distribute fundamental frequency evenly, which effectively reduces peak EMI.

The SC81442 implements full protections, including over current limit, short circuit protection, output over voltage protection and thermal shutdown. When device enters extreme over load condition so that output voltage is pulled low, hiccup mode is activated to further protect device. In order to save external components, device integrates compensation inside. In PFM mode, light load efficiency is optimized so that it has very low open load current consumption from input. External open-drain PGOOD can help eliminate the need of extra supervisor or sequencer devices.

The electrical specifications of SC81442 family are designed over junction temperature range from -40°C to 150°C.

10.2 VCC and Internal LDO Regulator

The VCC pin is the output of internal LDO regulator, used to supply power stage's drivers. The LDO charges BOOT capacitor while low side FET is ON. The nominal output voltage is 5V.

In order to further protect the device, VCC has UVLO circuit to prevent device from switching if its output voltage is too low. When VCC LDO's output voltage is above V_{CC_UVLO} rising threshold, VCC UVLO is released and relative circuits can be enabled. The UVLO threshold has 200mV hysteresis to provide robust protection.

10.3 AGND and Grounding

AGND is used as ground reference for internal analog circuitry, including feedback loop, control logic and VCC LDO. Keep AGND quiet is important.

10.4 FB and Output Voltage Setting

The output voltage can be adjusted externally through feedback divider network on FB pin, as what has been shown in **Figure 10-1**.

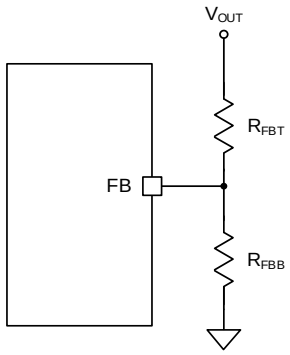


Figure 10-1 FB Configuration

The SC81442 uses 1V reference voltage for feedback. The FB pin voltage is compared with reference voltage and error voltage is used to help loop regulation. **Equation (1)** illustrates relationship between target DC output voltage V_{OUT}, R_{FBT} and R_{FBB}. R_{FBT} = 100kΩ is usually used for balance between noise immunity performance and current consumption on voltage divider.

$$1 = \frac{R_{FBB}}{R_{FBT} + R_{FBB}} \cdot V_{OUT} \quad (1)$$

10.5 PGOOD

The PGOOD function is implemented to eliminate external supervisor or sequencer devices, reducing solution size and BOM cost. Its output goes low when FB voltage is out of specified PGOOD window or device itself is disabled. There is a rising delay $t_{PGD\_DLY(rising)}$ before PGOOD is released (Output high = power OK). When there is a load/line transient, output voltage can experience excursion out of PGOOD window in a very short period. To prevent PGOOD's incorrect behavior, a glitch filter $t_{PGD\_DCH(falling)}$ is implemented.

10.6 EN/SYNC for Enable and Precise Input UVLO

EN/SYNC pin is multiplexed to be either precise enable or external clock synchronization. When it is used as precise

enable. Start-up and shutdown sequence can be controlled by pulling this pin high or low. Furthermore, precise enable threshold can help build user programmable input UVLO.

When EN pin's voltage is below V_{EN_VCC}, all internal circuitry is disabled and device stays at shutdown mode. The quiescent current is reduced as low as possible to 2 μA (typ.). Rising EN's voltage above V_{EN_VCC} enables internal VCC LDO but device has no switching. After EN rising above V_{EN_H}, the device initiates soft start-up and enters normal operation.

The EN/SYNC pin must be properly terminated and cannot be floating. EN/SYNC can be directly connected to V_{IN} for self-start-up for the simplest design. As shown in **Figure 10-2**, in order to build power up sequence and user programmable input UVLO, resistor dividers can be used to set appropriate threshold on EN/SYNC pin. The EN/SYNC has 300mV (typ.) hysteresis to help build robust enable or disable function. The EN/SYNC pin can also connect to an external I/O pin for systematical power sequence management.

Equation (2) can be used to calculate resistor values and **Equation (3)** can be used to calculate hysteresis after resistors are selected. V_{IN_R} is the input rising voltage for start-up and V_{IN_HYS} is the hysteresis.

$$R_{ENB} = R_{ENT} \cdot \frac{V_{EN\_H}}{V_{IN\_R} - V_{EN\_H}} \quad (2)$$

$$V_{IN\_HYS} = V_{EN\_HYS} \cdot \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (3)$$

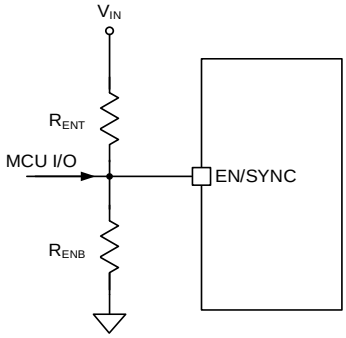


Figure 10-2 EN/SYNC Configuration for Precise Enable

10.7 EN/SYNC for Synchronization

The EN/SYNC pin can be used to synchronize internal oscillator to an external clock. As shown in **Figure 10-3**, internal oscillator is synchronized to the positive clock edge through C_{SYNC} AC coupling. This will prevent external clock when it is in idle state from interfering input UVLO.

The C_{SYNC}, R_{ENT} and R_{ENB} forms a high-pass filter in frequency domain seen from EN/SYNC pin. From demonstration of **Figure 10-4**, the cross-over frequency is determined by time constant τ, which is the product of C_{SYNC} and parallel resistance $R_{ENT}//R_{ENB}$. The cross-over frequency of the high-pass filter must be much lower than the external clock frequency. The recommended parallel resistance $R_{ENT}//R_{ENB}$ is 100kΩ. The AC coupling capacitor, C_{SYNC}, can be 1uF.

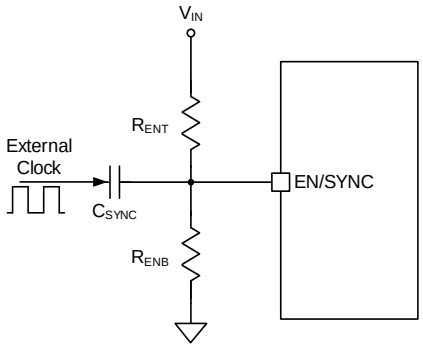


Figure 10-3 EN/SYNC Configuration for Clock Synchronization

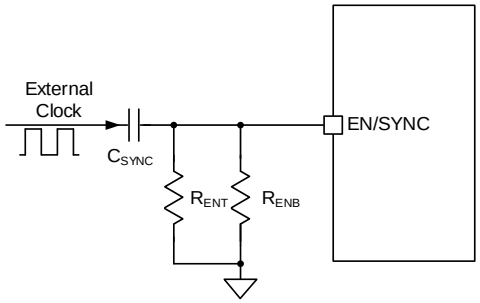


Figure 10-4 EN/SYNC High-pass Filter Demonstration

The device's synchronization frequency range is 200kHz to 2.2MHz. When synchronizing external clock, it should be noted that the R_T resistor needs to set free-run switching frequency equal or below the lowest synchronization clock frequency, as slope compensation is determined by the R_T value.

The amplitude of external clock needs to be higher than V_{EN_SYNC} to trigger internal synchronization pulse detector. An external clock with 3.3V or 5V amplitude can be used on EN/SYNC pin. Moreover, the minimum EN/SYNC rising pulse and falling pulse duration should be longer than $t_{SYNC,MIN}$, as what has been shown in **Figure 10-5**. Note that it is recommended to control rise/fall time of clock edge to be less than 30ns. Exerting external clock without meeting the requirements could deteriorate synchronization performance.

In order to prevent external clock from interfering the normal start-up, the clock must be off before start-up to allow proper sequencing. Exerting clock after PGOOD = high is recommended.

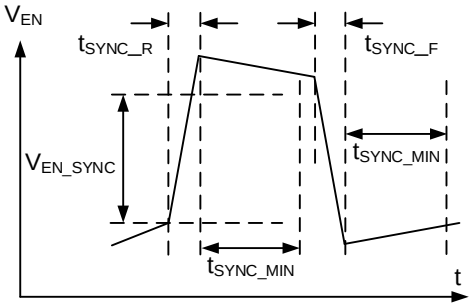


Figure 10-5 Typical EN/SYNC Waveform with External Clock

10.8 BOOT

The driver of high-side switch requires a voltage higher than V_{IN} to drive its gate. When low-side switch is ON, VCC charges C_{BOOT} through bootstrap diode. When low-side switch is OFF and high-side switch is turning on, C_{BOOT} boosts BOOT's voltage to SW+VCC and charge high-side switch gate.

In order to make proper high-side switch operation, if BOOT's voltage falls below $V_{SW}+V_{BOOT\_UVLO}$ when high-side switch is turning on, the high-side switch ON PWM will be ignored and low-side switch is turned on to charge C_{BOOT}. It is suggested to use a 0.1μF BOOT capacitor with 10V or higher voltage rating.

For SC81442, C_{BOOT} need to be connected to SW by the NC pin, which can help minimize the area of BOOT loop, and achieve good EMC performance.

10.9 Over Current Limit

SC81442 limits both inductor's peak current and valley current through cycle-by-cycle current limiting. Peak current limit is implemented by sensing the current in high-side switch after a short blanking time. Unlike normal peak current mode control, the peak current limit of high-side switch is not affected by loop slope compensation and remains constant I_{L-HS} over full operational duty cycle.

In terms of valley current limit, the low-side switch's current is sensed and limited. Before low-side switch is turned off, its current is compared with I_{L-LS}. If the current is higher than I_{L-LS}, the low-side switch's ON time is extended until LSFET's current is lower than I_{L-LS}. Then high-side switch is allowed to turn on per duty controlled by compensation loop.

10.10 Short Circuit Protection and Hiccup Mode

The hiccup mode is implemented when device is in extreme overload fault or outputs short circuit. The device enters hiccup mode when the following conditions are met for a hiccup on timer T_{HICCUP_ON}:

- Output voltage is below 0.4 (typ.) times nominal output voltage setting;
- The device is not in drop-out state.

In hiccup mode, device turns off both switches for time specified in T_{HICCUP_OFF}. After that, SC81442 tries to start up and ramp up output voltage. Hiccup mode helps decrease device's average die temperature under severe short circuit conditions. Refer to **Figure 10-6** for detailed waveform behavior when device is operating in hiccup mode.

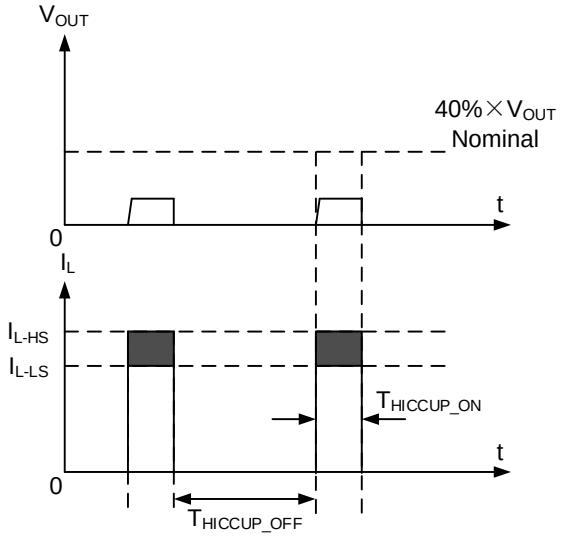


Figure 10-6 Hiccup Mode Operation

10.11 Soft-start and Recover from Dropout Operation or Over Current Limit

10.11.1 Soft-start

Soft-start is implemented to limit inrush current as a result of high output capacitance and helps build start-up sequence. After soft-start initiates, internal reference ramps up with a preset slew rate. Therefore, output voltage is controlled and ramped up with slew rate that is dependent on FB divider ratio.

Once soft-start is triggered or re-initiated, the internal reference is reset and ramping up. It takes t_{ss} for reference to ramp from 10% to 90% of its nominal value. The output voltage then follows reference to ramp up accordingly.

In order to prevent negative inductor current from pulling output voltage down at start-up, the device is automatically operating in diode emulation mode, in case output voltage is pre-biased. In diode emulation mode, low-side switch is turned off when its current trips to I_{L-ZC}. Refer to **Figure 10-7** for detailed operation demonstration.

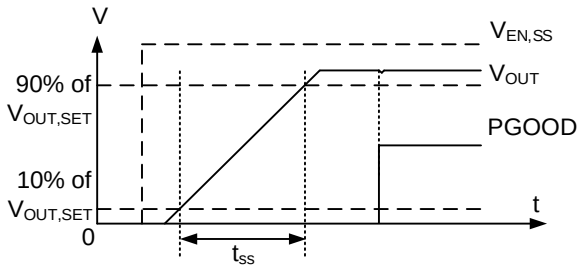


Figure 10-7 Soft-start With No Pre-bias

10.11.2 Recover from Dropout Operation or Over Current Limit

When device's output voltage drops a few percent because input voltage is not sufficient or over current limit is triggered, output voltage ramps up slowly with same slew rate as soft start if input voltage recovers or over current is released. This behavior is called recover from dropout operation or over current limit. The recover is different from normal soft start in following considerations:

- The reference voltage is set to the voltage that is needed to achieve the existing output voltage;
- Hiccup is allowed if device is operating in over current limit. The hiccup timer is disabled in dropout operation;
- FPWM is allowed. If output voltage is suddenly pulled high by another power supply, the device could pull down the output to the existing reference set voltage.

The **Figure 10-8** describes the behavior of the recover from dropout.

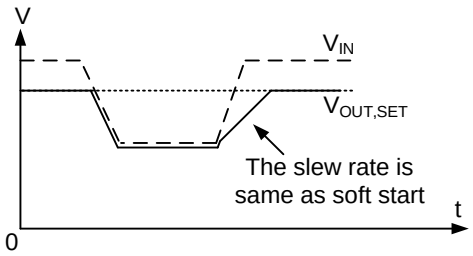


Figure 10-8 Recover from Dropout Operation

10.12 Spread Spectrum

Spread spectrum is a factory option for applications sensitive to EMI. Through implementing triangular spread spectrum, SC81442 is able to evenly distribute fundamental frequency and its harmonics. Therefore, peak emissions can be eliminated.

10.13 PFM Mode Operation

PFM mode is a factory option designed for applications which light load efficiency is important. In PFM mode, switching frequency varies with load. When load decreases, switching frequency also decreases to reduce switching loss.

In addition, device turns off low-side switch when its current triggers zero-cross current limit threshold I_{L-ZC}. This prevents inductor current from flowing reversely and improves efficiency further.

10.14 Thermal Shutdown

When device's junction temperature rises above 160°C (typ.), thermal shutdown occurs. In this state, device enters protection by turning off both FETs until die temperature decreases by the thermal shutdown hysteresis T_{SD_HYS}.

The thermal shutdown is a non-latching protection. If the fault persists the device will cycle into and out of thermal shutdown.

10.15 Minimum On/Off Time Operation

10.15.1 Minimum On Time Operation

The SC81442 family maintains output voltage in regulation even though input to output conversion ratio requires an on-time less than $T_{ON,MIN}$ under high switching frequency setting.

In applications which need on time lower than $T_{ON,MIN}$, high-side switch's on time is fixed to $T_{ON,MIN}$ Therefore, the actual switching frequency varies to adapt to required conversion ratio.

10.15.2 Minimum Off Time Operation (Dropout Operation)

The device can maintain output voltage stable when input is very close to output given high switching frequency setting.

In minimum off time operation, SC81442 keeps low-side switch's on time unchanged and is always $T_{OFF,MIN}$. Therefore, minimum off time is maintained and switching frequency varies with required conversion ratio.

Once input voltage drops when high-side switch's on time is extended to maximum on time $T_{ON,MAX}$, on time is not extended anymore. Consequently, output voltage tracks

below input voltage with a dropout voltage affected by input voltage, output voltage and load current.

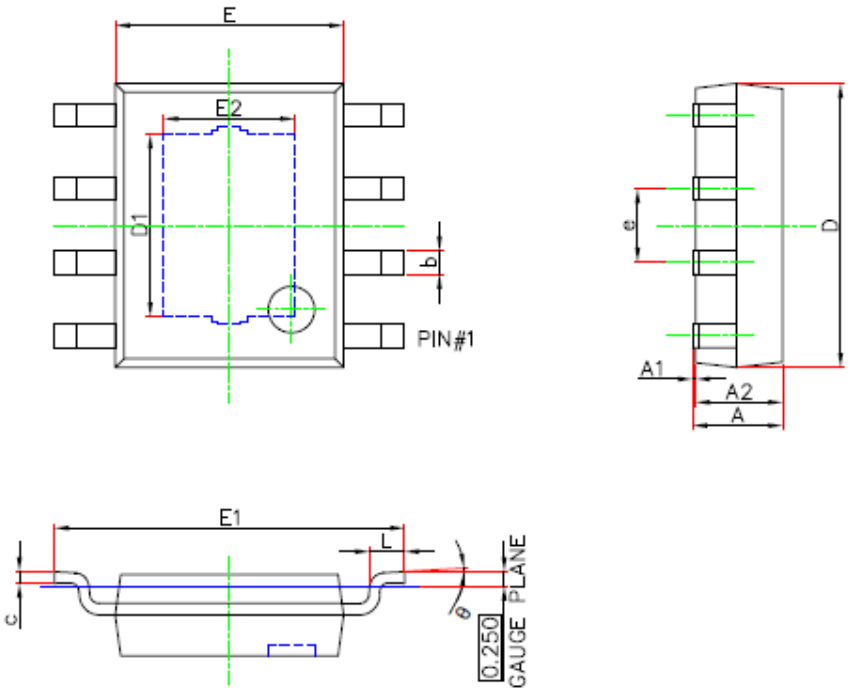
11 Layout Guide

The PCB layout is critical to get the optimal performance of DC-DC converter. A good PCB layout can improve the robustness and EMI performance of design. For SC81442, a buck converter, the loop consisting of power supply, input capacitors and power ground is the most important loop. Because this loop carries the input transient currents that cause the input voltage transient at input capacitors. Bad layout means larger trace inductance that can cause larger voltage transient. Generally, to reduce the PCB inductance, the area of this loop must be small, and the trace must be wide.

- Place the input capacitor or capacitors as close as possible input pin pairs.
- The VIN, VOUT, and GND paths must be wide and direct as possible to reduce any voltage drops on the input or output paths of the converter and maximizes efficiency.
- Layer of the PCB beneath the top layer with the IC must be a ground plane. This plane acts as a noise shield and a heat dissipation path. Using the layer directly next to the IC reduces the inclosed area in the input circulating current in the input loop, reducing inductance.
- Place C_{VCC} close to the VCC and AGND pins. This capacitor must be routed with short, wide traces to the VCC and GND pin.
- Place C_{BOOT} close to the BOOT pin, and use wide traces to rout them. It is important to reduce the exposed SW node area.
- Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.
- Place R_{FBB}, R_{FBT}, R_{FF}, and C_{FF}, if used, as close as possible to the device. The connections to FB and GND through RFBB must be short and close to those pins on the device. The connection to VOUT can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the converter.
- Connected the thermal pad to GND plane for proper heat sinking. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.

MECHANICAL DATA

SOP-8

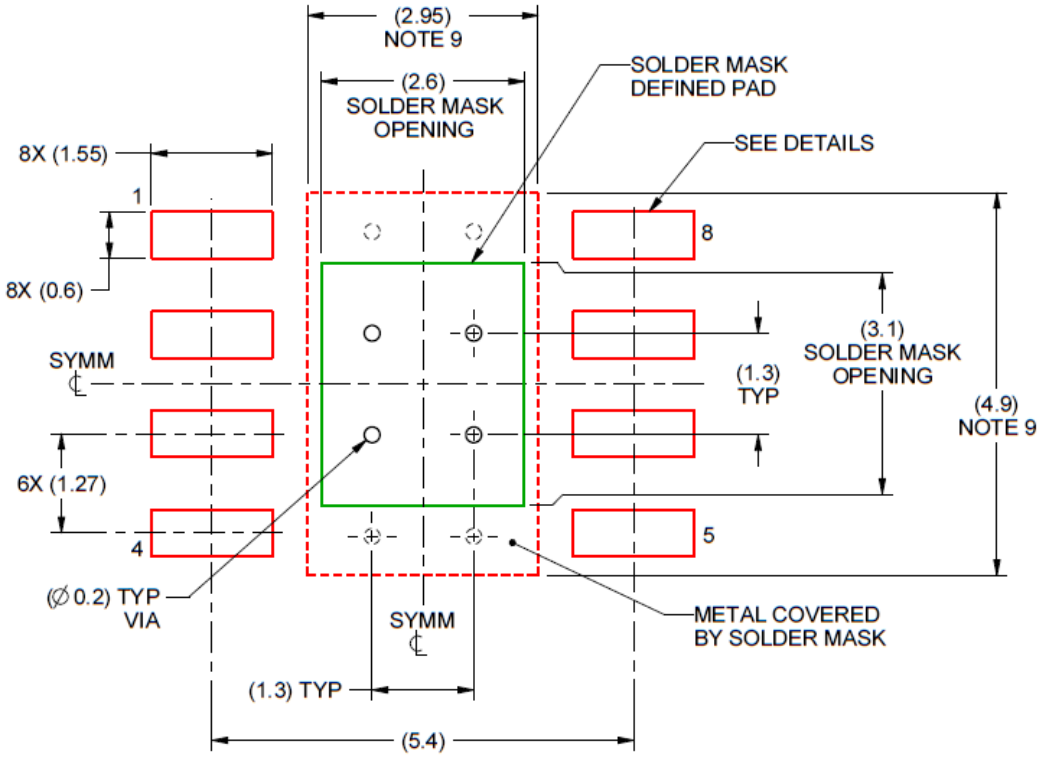


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

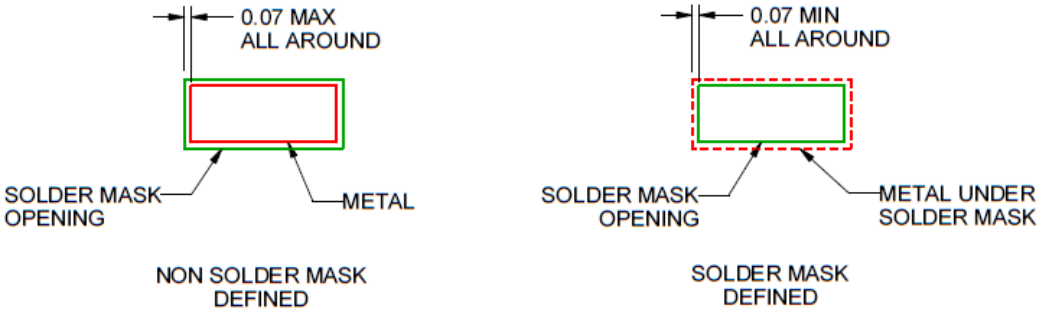
Unit: mm

RECOMMENDED FOOTPRINT

SOP-8



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS

Unit: mm

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