SC81440Q 36V/4A, Automotive Low I_Q Buck Converter

1 Descriptions

The SC81440Q is a synchronous Buck converter family with a wide input voltage from 3V to 36V. The SC81440Q regulates the output voltage at customized voltage by setting the divider resistors. It provides up to 4A of highly efficient output current with current mode control with fast loop response.

The SC81440Q is specifically designed for automotive applications. The device incorporates spread spectrum, QFN package, symmetrical pinout to optimize the EMI performance. Up to 2.2MHz switching frequency could help avoid noise sensitive frequency.

The SC81440Q employs peak current mode control scheme. The switching frequency could be synchronized to an external clock.

The SC81440Q offers output over-voltage protection, cycle-by-cycle peak current limit, output short circuit protection, and thermal shutdown protection.

The SC81440Q is available in 14-pin 4mm X 3.5mm QFN package.

2 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: T_A range: -40°C to 125 °C
- 3.5V to 36V start up input voltage, support 3.0V falling V_{IN}
- 2.5μA sleep mode quiescent current
- 200kHz to 2200kHz adjustable frequency, synchronized to external clock
- Adjustable output voltage through FB pin
- Frequency spread spectrum for low EMI
- Symmetric VIN pinout for low EMI
- Selectable option for PFM or FPWM mode
- Output OCL / SCP / OVP / TSD protection
- Pin-to-Pin compatible with
  - SC81460Q (Automotive, 36V/6A, adjustable F_{SW})
  - SC81480Q (Automotive, 36V/8A, adjustable F_{SW})
  - SC81440 (Industrial, 36V/4A, adjustable F_{SW})
  - SC81460 (Industrial, 36V/6A, adjustable F_{SW})
  - SC81480 (Industrial, 36V/8A, adjustable F_{SW})

3 Applications

- Automotive infotainment and cluster
- Automotive head unit
- Automotive ADAS

4 Device Information

ORDER NUMBER	OUTPUT VOLTAGE	MODE IN LIGHT LOAD	SPREAD SPECTRUM	PACKAGE	SWITCHING FREQUENCY	BODY SIZE
SC81440QQFSR	Adjustable	PFM (Auto Mode)	Yes	QFN-14	Adjustable	4mm×3.5mm×0.9mm
SC81440AQQFSR(1)	Adjustable	FPWM	Yes	QFN-14	Adjustable	4mm×3.5mm×0.9mm

(1) Contant SouthChip

5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Date	Page(s) changed	Changes Description
V1.0.7	2025/5	31	1. Add the layout user guide
V1.0.6	2024/12	6	2. Update VOUT range to 0.95 VIN
V1.0.5	2024/11	7, 8	1. Add low-side current limit spec for FPWM version. 2. Add thermal resister information.

6 Typical Application Circuit

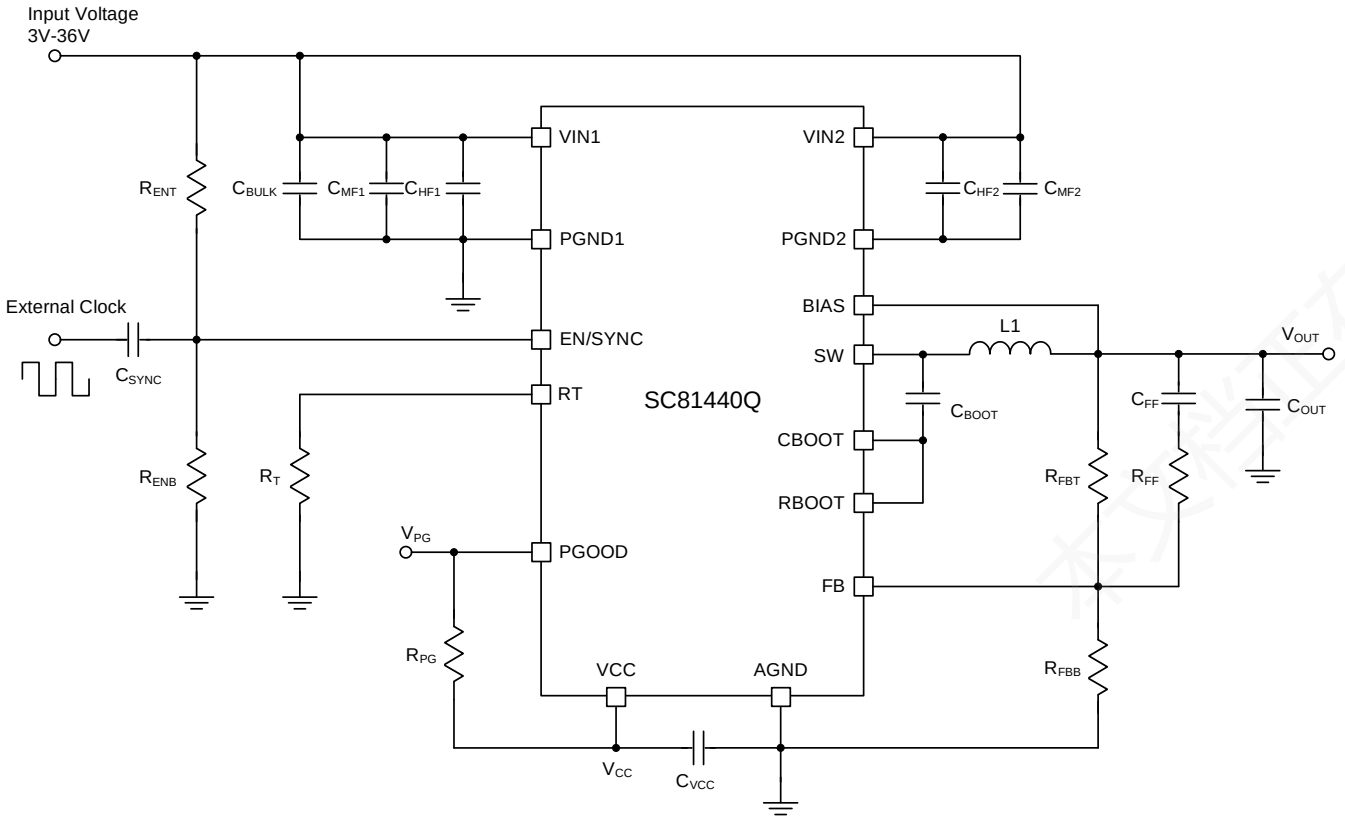
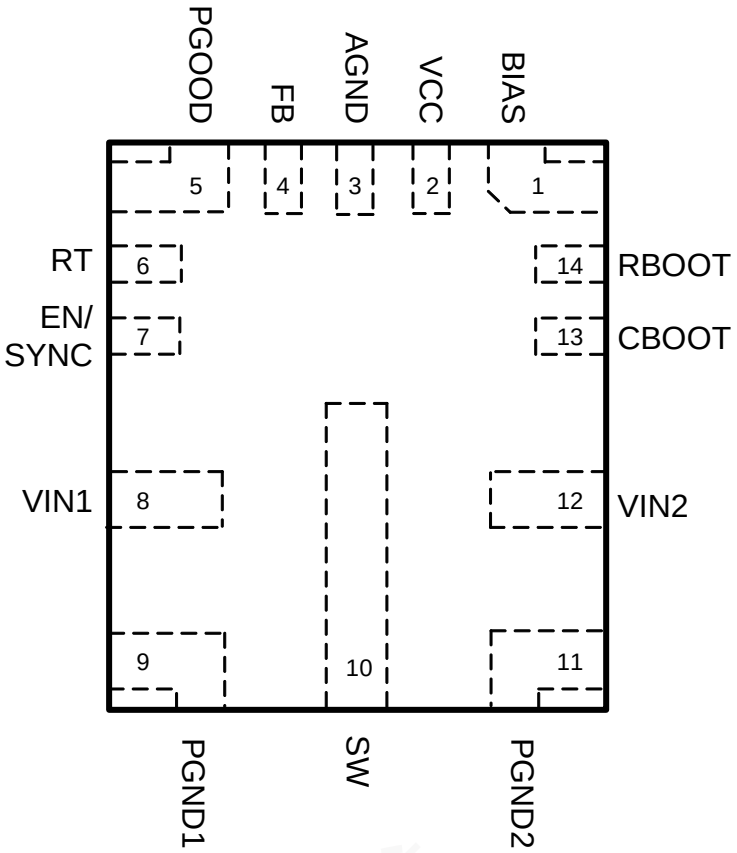


Figure 6-1. Typical Application Circuit

7 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	BIAS	I	Input to internal LDO. Connect to output voltage point to improve efficiency. Connect an optional high quality 0.1-μF to 1-μF capacitor from this pin to ground for improved noise immunity. If output voltage is above 12 V, connect this pin to ground.
2	VCC	O	Internal LDO output. Used as supply to internal control circuits. Connect a high-quality 1-μF capacitor from this pin to AGND.
3	AGND	G	Analog ground. Must connect AGND to both PGND1 and PGND2 on PCB.
4	FB	I	Output voltage feedback input to the internal control loop. Connect to feedback divider tap point for adjustable output voltage.
5	PGOOD	O	Open-drain power-good status output. Pull this pin up to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. PGOOD output is valid when EN = low, VIN > 2 V.
6	RT	I	Connect this pin to ground through a resistor to set switching frequency between 200 kHz and 2200 kHz.
7	EN/SYNC	I	Precision enable input. High = on, Low = off. Can be used as an adjustable UVLO. Also functions as a synchronization input pin. Triggers on rising edge of external clock. A capacitor must be used to AC couple the synchronization signal to this pin. This pin cannot be floating and must be properly terminated.
8	VIN1	I	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1.

9	PGND1	G	Power ground to internal low-side MOSFET. Connect to system ground. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
10	SW	O	Switch node of the converter.
11	PGND2	G	Power ground to internal low-side MOSFET. Connect to system ground. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
12	VIN2	I	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2.
13	CBOOT	I/O	High-side driver upper supply rail. Connect a 100-nF capacitor between SW pin and CBOOT. An internal diode connects CBOOT to VCC and allows CBOOT to charge while SW node is low.
14	RBOOT	I/O	Connect to CBOOT through a resistor with resistance from 0Ω to open to adjust SW node rising slew rate.

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C ~ 150°C (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN1, VIN2, EN/SYNC to AGND, PGND	-0.3	42	V
	SW to AGND, PGND	-0.3	VIN+0.3	V
	RBOOT, CBOOT to SW	-0.3	5.5	V
	RBOOT, CBOOT to AGND, PGND(3)	-0.3	47.5	V
	BIAS to AGND, PGND	-0.3	16	V
	PGND to AGND(4)	-1	2	V
	All other pins to AGND, PGND	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-40	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) Do not exceed SW pin's voltage rating.

(4) This specification applies to voltage durations of 100 ns or less. The maximum D.C. voltage should not exceed ± 0.3 V.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM)(2), per AEC Q100-002	-2000	2000	V
	Charged device model (CDM)(3), per AEC Q100-011	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	3.0		36	V
V_{OUT}	Output voltage range	1 (SC81440AQ)		$0.95\times V_{IN}$	V
		2.5 (SC81440Q)			
F_{SW}	Switching Frequency Range	200		2200	kHz
I_{OUT}	Output DC current range	0		4	A
T_J	Operating junction temperature	-40		150	°C
T_A	Operating ambient temperature range	-40		125	°C

8.4 Thermal Information

THERMAL RESISTANCE		QFN-14 (4mm x 3.5mm)	UNIT
$R_{\Theta JA}$	Junction to ambient thermal resistance (SC81440QEVM) (1)	24.1	°C/W
$R_{\Theta JA}$	Junction to ambient thermal resistance (JESD 51-7) (2)	56.5	°C/W
$R_{JC(top)}$	Junction to case (top) resistance (2)	24.9	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	17.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W

(1) Measured on SC81440QEVM. 4-layer, 2-oz Cu per top and bottom layer and 1-oz Cu per inner layer, evaluation board.

(2) Measured on JESD51-7, 4-layer PCB;

8.5 Electrical Characteristics

T_J = -40°C to 150°C, V_{IN} = 13.5V. Typical value is tested at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		3.0		36	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising		3.3	3.5	V
		V_{IN} falling		2.78	3.0	V
I_Q	Quiescent current into the VIN pin	V_{FB} = +5%, V_{BIAS} = 5V		2.5		μA
I_{SD}	Shutdown current into the VIN pin	V_{EN} = 0V		2		μA
V_{CC}	Internal regulator output	I_{VCC} = 50mA	3.1	3.3	3.5	V
V_{CC_UVLO}	V_{CC} under voltage lockout threshold	V_{CC} rising		2.2	2.32	V
		V_{CC} falling		2.0	2.12	V
EN						
V_{EN_VCC}	EN input level to turn on internal LDO		0.4			V
V_{EN_H}	EN input level to start switching	Rising threshold	1.14	1.19	1.25	V
V_{EN_HYS}	Enable threshold hysteresis			300		mV
t_{BLK}(1)	Blanking of EN after rising or falling edges		9.8		45	μs
SOFT START						
t_{SS}	Time for V_{REF} from 10% to 90%			4.5		ms
MOSFETS						
$R_{DS(on)}$	High-side MOSFET on resistance			35		mΩ
	Low-side MOSFET on resistance			20		mΩ
V_{BOOT_UVLO}	Voltage on CBOOT pin compared to SW which will turn off high-side switch	V_{CBOOT} falling		1.78		V

FEEDBACK						
V_{FB}	FB reference voltage	VIN = 3.5 - 36V, T_J = 25°C	0.995	1	1.005	V
		VIN = 3.5 - 36V	0.98	1	1.02	V
I_{FB}	Input current from FB to AGND			1		nA
CURRENT LIMIT						
I_{L-HS}	High side switch current limit		5.6	7	8.4	A
I_{L-LS}	Low side switch current limit	APFM Mode	4	5	6	A
		FPWM Mode	4	6	8	A
I_{L-ZC}	Zero-cross current limit. Current sourcing out of SW pin			0.25		A
I_{L-NEG}	Negative current limit in FPWM and SYNC Modes. Current sinking into SW pin			2		A
HICCUP						
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage	Not included in soft start		40		%
T_{HICCUP_ON}	Hiccup on Timer			10		ms
T_{HICCUP_OFF}	Hiccup off Timer			80		ms
POWER GOOD						
$V_{PG\_OV\_R}$	PGOOD upper threshold - rising	% of VOUT setting	105	107	109	%
$V_{PG\_UV\_F}$	PGOOD lower threshold - falling	% of VOUT setting	92	94	96	%
V_{PG_HYS}	PGOOD hysteresis	% of VOUT setting		2		%
$V_{IN(PG\_VALID)}$	Input voltage for proper PGOOD function		2.2			V
$V_{PG(LOW)}$	Low level PGOOD output voltage	I_{SINK} = 1mA		0.1	0.3	V
I_{OV}	Discharge current at the SW node under OVP condition			0.5		mA
$t_{PGD\_DLY(rising)}$	Delay for the PGOOD signal from low to high			2		ms
$t_{PGD\_DCH(falling)}$	Deglitch time for PGOOD signal from high to low			120		µs
OSCILLATOR						
f_{ADJ1}	Minimum adjustable frequency by R_T or SYNC	R_T = 66.5kΩ, 1%	170	200	230	kHz
f_{ADJ2}	Adjustable frequency by R_T or SYNC with 400kHz setting	R_T = 32.4kΩ, 1%	360	400	440	
f_{ADJ3}	Maximum adjustable frequency by R_T or SYNC	R_T = 5.2kΩ, 1%	1980	2200	2420	
f_{SYNC}	Synchronization Frequency Range		200		2200	kHz
SPREAD SPECTRUM						

F_{SS}	Frequency span of spread spectrum operation - deviation from center frequency	Spread spectrum active	-10		10	%
F_{PSS}(1)	Spread spectrum pattern cycles			128		
PWM LIMITS						
T_{ON_MIN}	Minimum HS switch on time			45	70	ns
T_{ON_MAX}	Maximum HS switch on time			10		μs
T_{OFF_MIN}	Minimum LS switch on time			80	110	ns
SYNCHRONOUS CLOCK						
V_{EN_SYNC}	Sync clock amplitude voltage threshold necessary to sync using EN/SYNC pin	V_{CC}=3.3V			2.95	V
t_{SYNC_MIN}	Minimum sync clock pulse width	V_{CC}=3.3V	120			ns
t_{SYNC_R}(1)	Maximum sync clock rising time				30	ns
t_{SYNC_F}(1)	Maximum sync clock falling time				30	ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	T_J rising	150	160	170	°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

(1) Guarantee by Design

8.6 Typical Characteristics

Unless otherwise specified, V_{IN} = 13.5 V and F_{SW} = 400 kHz.

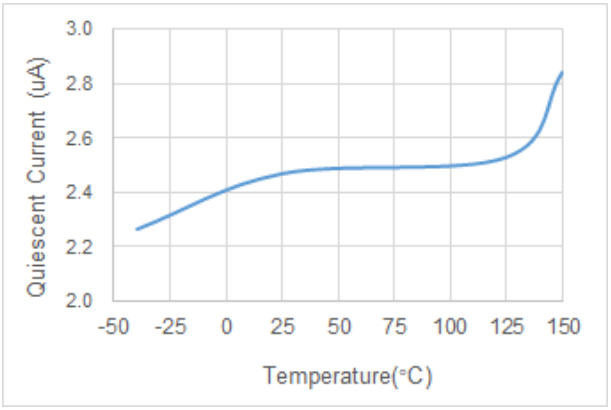


Figure 8-1 Non-Switching Input Supply Current

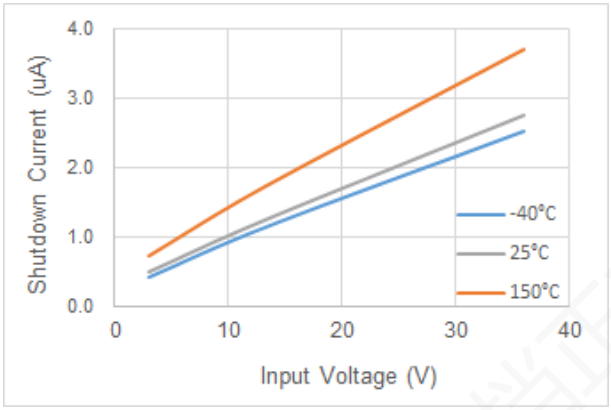


Figure 8-2. Shutdown Supply Current

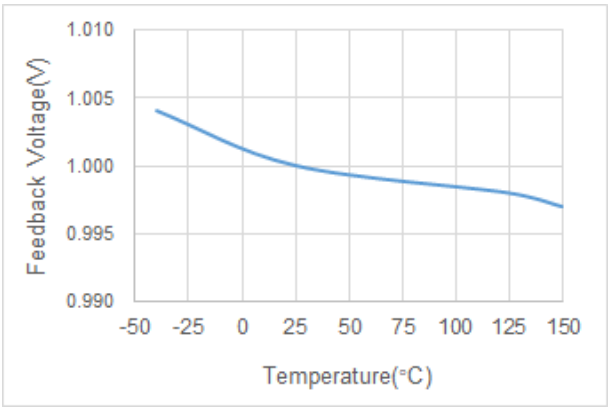


Figure 8-3. Feedback Voltage

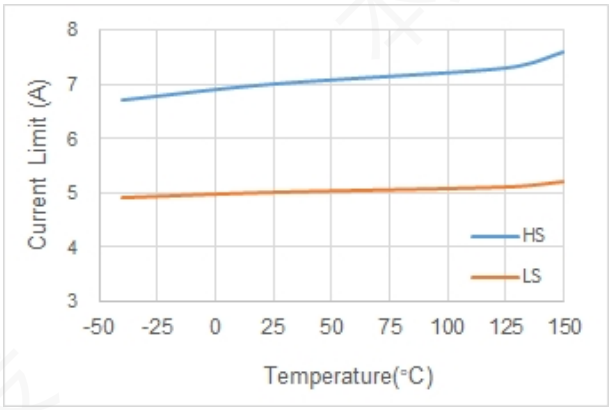


Figure 8-4. High-side and Low-side Current Limits

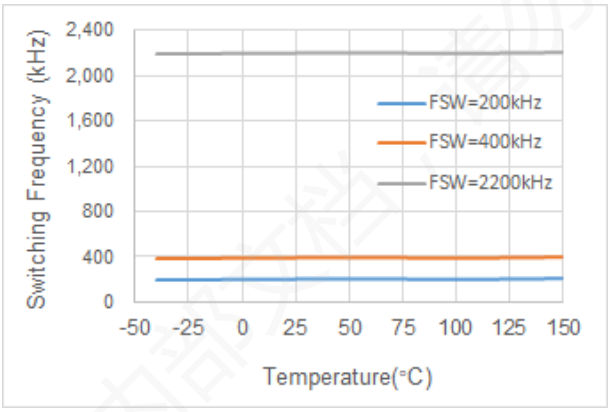


Figure 8-5. Switching Frequency Set by R_T Resistor

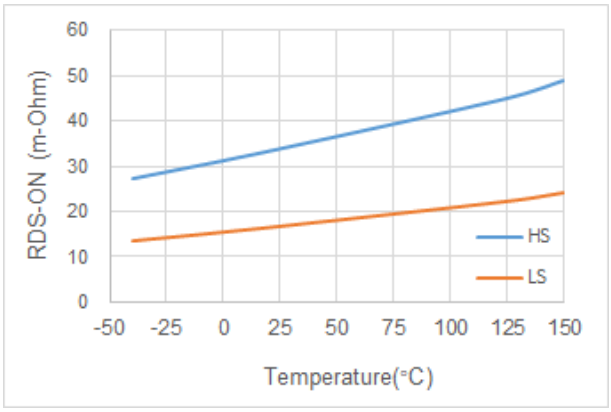


Figure 8-6. High-side and Low-side Switches R_{DS_ON}

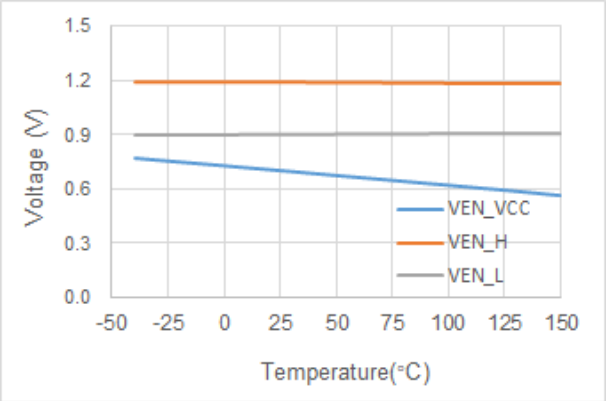


Figure 8-7. Enable Thresholds

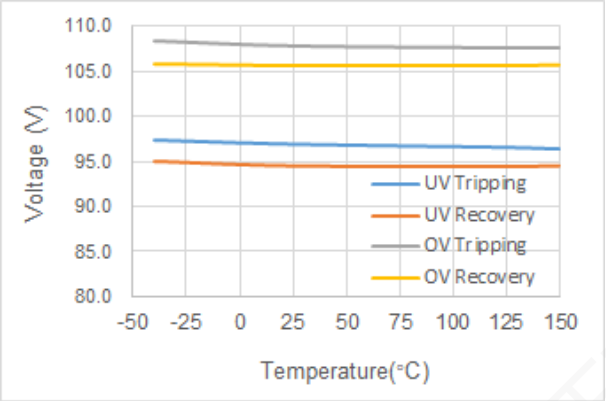


Figure 8-8. PGOOD Thresholds

9 Functional Block Diagram

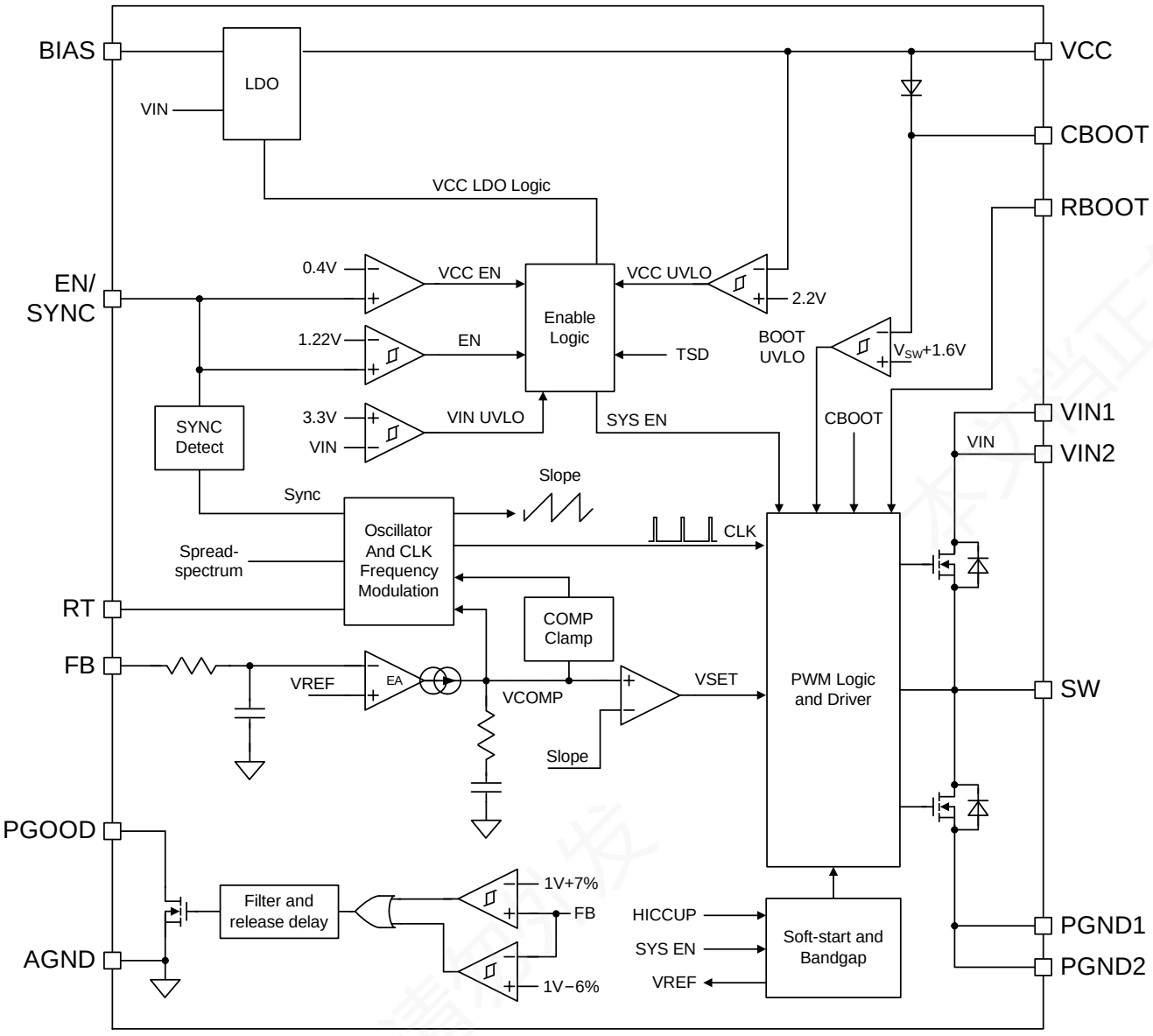


Figure 9-1. Functional Block Diagram

10 Feature Description

10.1 Overview

SC81440Q is a wide input, 4A, synchronous Buck converter for automotive applications. Implementing peak-current mode control, SC81440Q is able to operate over a wide range of conversion ratio with excellent line and load transient performance. In addition, internal slope compensation increases integration and helps maintain loop stability. The converter can also operate from 200kHz to 2.2MHz switching frequency with external clock synchronization capability. The wide range of adjustable switching frequency enables design flexibility for applications sensitive to noise around AM band. For automotive battery power application, device must sustain its output at extreme conditions like load dump and cranking. With TVS, device's input can vary from 36V down to 3V, resulting in device entering minimum-on time or minimum-off time operation. Through adaptively extending switching cycle, SC81440Q can still maintain output voltage regulation.

Automotive applications have stringent requirement for low EMI. Although very high efficiency, DC/DC converters are naturally ideal EMI source. SC81440Q is specifically designed to optimize EMI performance through different ways. Incorporating spread spectrum, SC81440Q can distribute fundamental frequency evenly, which effectively reduces peak EMI. Additionally, innovative symmetrical pinout reduces input parasitic inductance and QFN package minimize switching node ringing. Optional RBOOT resistor is also available to adjust switching node slew rate. These ways can help optimize EMI performance so that expensive EMI shielding equipment is not needed.

The SC81440Q implements full protections, including over current limit, short circuit protection, output over voltage protection and thermal shutdown. When device enters extreme over load condition so that output voltage is pulled low, hiccup mode is activated to further protect device. In order to save external components, device integrates compensation inside. Moreover, device provides optional PFM mode or FPWM mode. In PFM mode, light load efficiency is optimized so that it has very low open load current consumption from input. FPWM mode is available for applications in which small output voltage ripple is very critical. External open-drain PGOOD can help eliminate the need of extra supervisor or sequencer devices.

The SC81440Q family is AEC-Q100 qualified. The electrical specifications are designed over junction temperature range from -40°C to 150°C.

10.2 BIAS, VCC and Internal LDO Regulator

The VCC pin is the output of internal LDO regulator, used to supply power stage's drivers. The LDO charges CBOOT capacitor while low side FET is ON. The nominal output voltage is 3.3V. The BIAS pin is the input to the VCC LDO. This pin can be connected to output to further improve light load efficiency. If BIAS input is lower than 3.1V, VIN will be used to directly supply LDO.

When BIAS is not used or output voltage is above 12V, the BIAS pin should be short to GND.

In order to further protect the device, VCC has UVLO circuit to prevent device from switching if its output voltage is too low. When VCC LDO's output voltage is above V_{CC_UVLO} rising threshold, VCC UVLO is released and relative circuits can be enabled. The UVLO threshold has 200mV hysteresis to provide robust protection.

10.3 AGND and Grounding

AGND is used as ground reference for internal analog circuitry, including feedback loop, control logic and VCC LDO. Keep AGND quiet is important.

10.4 FB and Output Voltage Setting

The output voltage can be adjusted externally through feedback divider network on FB pin, as what has been shown in **Figure 10-1**.

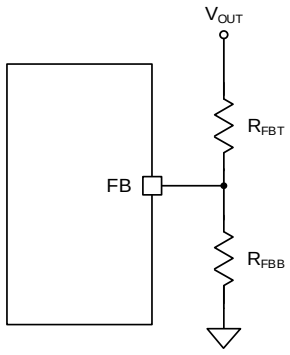


Figure 10-1 FB Configuration

The SC81440Q uses 1V reference voltage for feedback. The FB pin voltage is compared with reference voltage and error voltage is used to help loop regulation. **Equation (1)** illustrates relationship between target DC output voltage V_{OUT}, R_{FBT} and R_{FBB}. R_{FBT} = 100kΩ is usually used for balance between noise immunity performance and current consumption on voltage divider.

$$1 = \frac{R_{FBB}}{R_{FBT} + R_{FBB}} \cdot V_{OUT} \quad (1)$$

Feedforward network in **Figure 10-2** is optional to add an additional pole and zero in loop compensation. It needs to be parallel to R_{FBT}. The zero and pole's frequency introduced by feedforward network is demonstrated in **Equation (2)** and **Equation (3)**, respectively. From the **Equation (2) ~ (3)**, it can be told that feedforward zero f_{FFZ}'s frequency is always lower than pole f_{FFP}. Therefore, feedforward network can introduce additional phase lead and increase loop gain. This helps extend loop bandwidth so transient performance is improved.

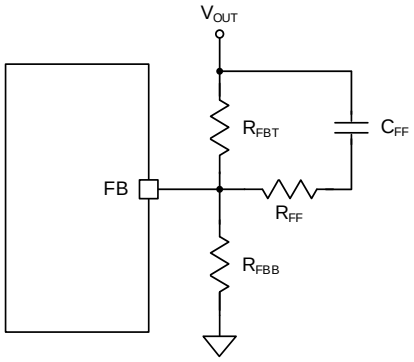


Figure 10-2 FB Configuration with Feedforward Network

$$f_{FFZ} = \frac{1}{2\pi(R_{FBT} + R_{FF})C_{FF}} \quad (2)$$

$$f_{FFP} = \frac{1}{2\pi(R_{FBT}//R_{FBB} + R_{FF})C_{FF}} \quad (3)$$

10.5 PGOOD

The PGOOD function is implemented to eliminate external supervisor or sequencer devices, reducing solution size and BOM cost. Its output goes low when FB voltage is out of specified PGOOD window or device itself is disabled. There is a rising delay $t_{PGD\_DLY(rising)}$ before PGOOD is released (Output high = power OK). When there is a load/line transient, output voltage can experience excursion out of PGOOD window in a very short period. To prevent PGOOD's incorrect behavior, a glitch filter $t_{PGD\_DCH(falling)}$ is implemented.

10.6 RT and Switching Frequency

A resistor from RT to AGND is needed to set target switching frequency. **Equation (4)** and **Figure 10-3** can be used to determine the resistance. If synchronization to an external clock is needed, do not apply the signal to RT pin. Instead, EN/SYNC can be used for external clock synchronization.

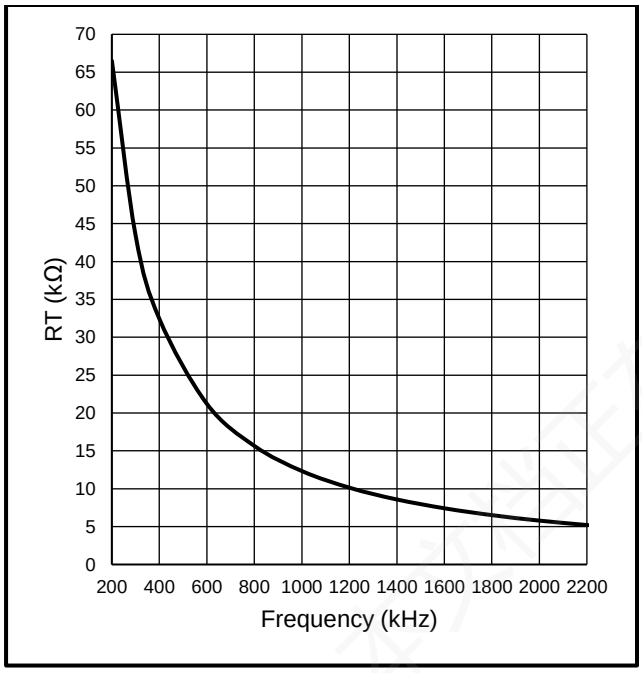


Figure 10-3 RT and Switching Frequency Relationship

$$R_T(k\Omega) = 1.8711 \times 10^4 \times F_{SW}(kHz)^{-1.062} \quad (4)$$

10.7 EN/SYNC for Enable and Precise Input UVLO

EN/SYNC pin is multiplexed to be either precise enable or external clock synchronization. When it is used as precise enable. Start-up and shutdown sequence can be controlled by pulling this pin high or low. Furthermore, precise enable threshold can help build user programmable input UVLO.

When EN pin's voltage is below V_{EN_VCC}, all internal circuitry is disabled and device stays at shutdown mode. The quiescent current is reduced as low as possible to 2 μA (typ.). Rising EN's voltage above V_{EN_VCC} enables internal VCC LDO but device has no switching. After EN rising above V_{EN_H}, the device initiates soft start-up and enters normal operation.

The EN/SYNC pin must be properly terminated and cannot be floating. EN/SYNC can be directly connected to V_{IN} for self-start-up for the simplest design. As shown in **Figure 10-4**, in order to build power up sequence and user programmable input UVLO, resistor dividers can be used to set appropriate threshold on EN/SYNC pin. The EN/SYNC has 300mV (typ.) hysteresis to help build robust enable or disable function. The EN/SYNC pin can also connect to an external I/O pin for systematical power sequence management.

Equation (5) can be used to calculate resistor values and **Equation (6)** can be used to calculate hysteresis after resistors are selected. V_{IN_R} is the input rising voltage for start-up and V_{IN_HYS} is the hysteresis.

$$R_{ENB} = R_{ENT} \cdot \frac{V_{EN\_H}}{V_{IN\_R} - V_{EN\_H}} \quad (5)$$

$$V_{IN\_HYS} = V_{EN\_HYS} \cdot \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (6)$$

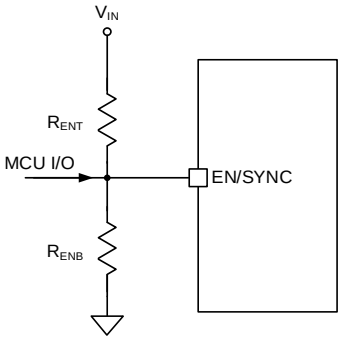


Figure 10-4 EN/SYNC Configuration for Precise Enable

10.8 EN/SYNC for Synchronization

The EN/SYNC pin can be used to synchronize internal oscillator to an external clock. As shown in **Figure 10-5**, internal oscillator is synchronized to the positive clock edge through C_{SYNC} AC coupling. This will prevent external clock when it is in idle state from interfering input UVLO.

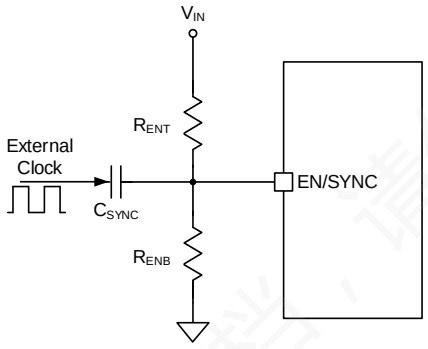


Figure 10-5 EN/SYNC Configuration for Clock Synchronization

The C_{SYNC}, R_{ENT} and R_{ENB} forms a high-pass filter in frequency domain seen from EN/SYNC pin. From demonstration of **Figure 10-6**, the cross-over frequency is determined by time constant τ, which is the product of C_{SYNC} and parallel resistance $R_{ENT}//R_{ENB}$. The cross-over frequency of the high-pass filter must be much lower than the external clock frequency. The recommended parallel resistance $R_{ENT}//R_{ENB}$ is 100kΩ. The AC coupling capacitor, C_{SYNC}, can be 1 μF.

The device's synchronization frequency range is 200kHz to 2.2MHz. When synchronizing external clock, it should be noted that the R_T resistor needs to set free-run switching frequency equal or below the lowest synchronization clock frequency, as slope compensation is determined by the R_T value.

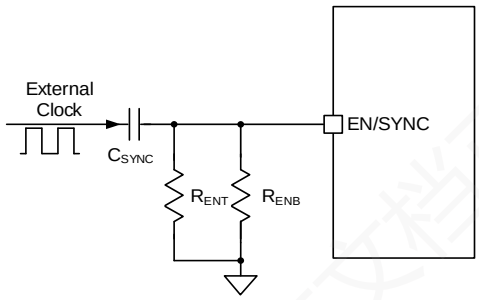


Figure 10-6 EN/SYNC High-pass Filter Demonstration

The amplitude of external clock needs to be higher than V_{EN_SYNC} to trigger internal synchronization pulse detector. An external clock with 3.3V or 5V amplitude can be used on EN/SYNC pin. Moreover, the minimum EN/SYNC rising pulse and falling pulse duration should be longer than $t_{SYNC,MIN}$, as what has been shown in **Figure 10-7**. Note that it is recommended to control rise/fall time of clock edge to be less than 30ns. Exerting external clock without meeting the requirements could deteriorate synchronization performance.

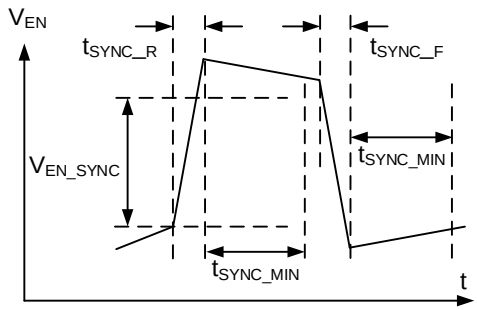


Figure 10-7 Typical EN/SYNC Waveform with External Clock

In order to prevent external clock from interfering the normal start-up, the clock must be off before start-up to allow proper sequencing. Exerting clock after PGOOD = high is recommended.

10.9 CBOOT and RBOOT

The driver of high-side switch requires a voltage higher than V_{IN} to drive its gate. When low-side switch is ON, VCC charges C_{BOOT} through bootstrap diode. When low-side

switch is OFF and high-side switch is turning on, C_{BOOT} boosts CBOOT's voltage to SW+VCC and charge high-side switch gate.

There is a separate RBOOT pin to provide flexibility of optimized EMI with respect to efficiency. Separating current drawn from CBOOT pin, RBOOT allows control of SW rising slew rate without slowing down charge of VCC to C_{BOOT}. When RBOOT is open, SW rise slew rate is setting slowest. This benefits EMI performance but sacrifices efficiency. However, when RBOOT is short to CBOOT, SW rise slew rate is setting fastest. Therefore, switching loss is reduced and efficiency is optimized.

In order to make proper high-side switch operation, if CBOOT's voltage falls below $V_{SW}+V_{BOOT\_UVLO}$ when high-side switch is turning on, the high-side switch ON PWM will be ignored and low-side switch is turned on to charge C_{BOOT}. It is suggested to use a 0.1μF BOOT capacitor with 10V or higher voltage rating.

10.10 Over Current Limit

SC81440Q limits both inductor's peak current and valley current through cycle-by-cycle current limiting. Peak current limit is implemented by sensing the current in high-side switch after a short blanking time.

In terms of valley current limit, the low-side switch's current is sensed and limited. Before low-side switch is turned off, its current is compared with I_{L-LS}. If the current is higher than I_{L-LS}, the low-side switch's ON time is extended until LSFET's current is lower than I_{L-LS}. Then high-side switch is allowed to turn on per duty controlled by compensation loop.

10.11 Short Circuit Protection and Hiccup Mode

The hiccup mode is implemented when device is in extreme overload fault or outputs short circuit. The device enters hiccup mode when the following conditions are met for a hiccup on timer T_{HICCUP_ON}:

- Output voltage is below 0.4 (typ.) times nominal output voltage setting;
- The device is not in drop-out state.

In hiccup mode, device turns off both switches for time specified in T_{HICCUP_OFF}. After that, SC81440Q tries to start up and ramp up output voltage. Hiccup mode helps decrease device's average die temperature under severe short circuit conditions. Refer to **Figure 10-8** for detailed waveform behavior when device is operating in hiccup mode.

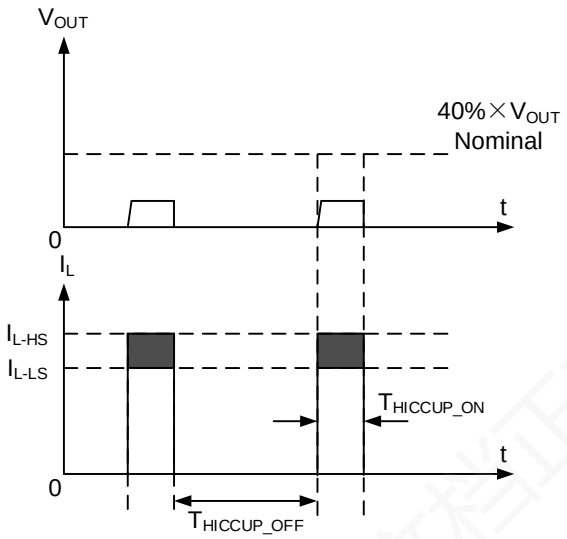


Figure 10-8 Hiccup Mode Operation

10.12 Soft-start and Recover from Dropout Operation or Over Current Limit

10.12.1 Soft-start

Soft-start is implemented to limit inrush current as a result of high output capacitance and helps build start-up sequence. After soft-start initiates, internal reference ramps up with a preset slew rate. Therefore, output voltage is controlled and ramped up with slew rate that is dependent on FB divider ratio.

Once soft-start is triggered or re-initiated, the internal reference is reset and ramping up. It takes t_{ss} for reference to ramp from 10% to 90% of its nominal value. The output voltage then follows reference to ramp up accordingly.

In order to prevent negative inductor current from pulling output voltage down at start-up, the device is automatically operating in diode emulation mode, in case output voltage is pre-biased. In diode emulation mode, low-side switch is turned off when its current trips to I_{L-ZC}. Refer to **Figure 10-9** for detailed operation demonstration.

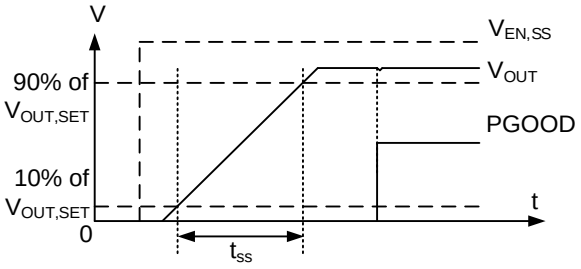


Figure 10-9 Soft-start With No Pre-bias

10.12.2 Recover from Dropout Operation or Over Current Limit

When device's output voltage drops a few percent because input voltage is not sufficient or over current limit is triggered, output voltage ramps up slowly with same slew rate as soft start if input voltage recovers or over current is released. This behavior is called recover from dropout operation or over current limit. The recover is different from normal soft start in following considerations:

- The reference voltage is set to the voltage that is needed to achieve the existing output voltage;
- Hiccup is allowed if device is operating in over current limit. The hiccup timer is disabled in dropout operation;
- FPWM is allowed. If output voltage is suddenly pulled high by another power supply, the device could pull down the output to the existing reference set voltage.

The **Figure 10-10** describes the behavior of the recover from dropout.

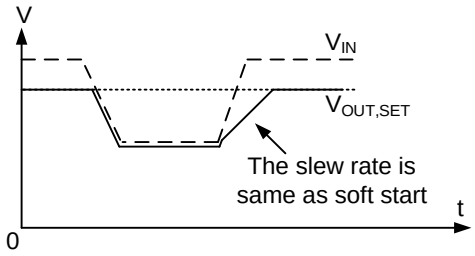


Figure 10-10 Recover from Dropout Operation

10.13 Spread Spectrum

Spread spectrum is a factory option for applications sensitive to EMI. Through implementing triangular spread spectrum, SC81440Q is able to evenly distribute fundamental frequency and its harmonics. Therefore, peak emissions can be eliminated.

10.14 PFM Mode Operation

PFM mode is a factory option designed for applications which light load efficiency is important. In PFM mode, switching frequency varies with load. When load decreases, switching frequency also decreases to reduce switching loss.

In addition, device turns off low-side switch when its current triggers zero-cross current limit threshold I_{L-ZC}. This prevents inductor current from flowing reversely and improves efficiency further.

10.15 Thermal Shutdown

When device's junction temperature rises above 160°C (typ.), thermal shutdown occurs. In this state, device enters protection by turning off both FETs until die temperature decreases by the thermal shutdown hysteresis T_{SD_HYS}.

The thermal shutdown is a non-latching protection. If the fault persists the device will cycle into and out of thermal shutdown.

10.16 Minimum On/Off Time Operation

10.16.1 Minimum On Time Operation

The SC81440Q family maintains output voltage in regulation even though input to output conversion ratio requires an on-time less than $T_{ON,MIN}$ under high switching frequency setting.

In applications which need on time lower than $T_{ON,MIN}$, high-side switch's on time is fixed to $T_{ON,MIN}$ Therefore, the actual switching frequency varies to adapt to required conversion ratio.

10.16.2 Minimum Off Time Operation (Dropout Operation)

The device can maintain output voltage stable when input is very close to output given high switching frequency setting.

In minimum off time operation, SC81440Q keeps low-side switch's on time unchanged and is always $T_{OFF,MIN}$. Therefore, minimum off time is maintained and switching frequency varies with required conversion ratio.

Once input voltage drops when high-side switch's on time is extended to maximum on time $T_{ON,MAX}$, on time is not extended anymore. Consequently, output voltage tracks below input voltage with a dropout voltage affected by input voltage, output voltage and load current.

11 Application Information

The SC81440Q step-down DC-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 4A. The following design procedure can be used to select components for the SC81440Q. **Figure 6-1** shows a typical application circuit for the SC81440Q. This device is designed to function with a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, **Table 11-1** provides typical component values for some of the common configurations.

Table 11-1. Typical External Component Values

PARAMETER	VALUE			
F_{SW} (kHz)	2100	400	2100	400
V_{OUT} (V)	3.3	3.3	5	5
L (μH)	1	4.7	1.5	4.7
C_{OUT} (rated)	3*22μF	4*22μF	2*22μF	3*22μF
R_{FBT} (kΩ)	100	100	100	100
R_{FBB} (kΩ)	43.2	43.2	24.9	24.9
C_{BOOT} (μF)	0.1	0.1	0.1	0.1
R_{BOOT} (Ω)	0	0	0	0
C_{VCC} (μF)	1	1	1	1
C_{FF} (pF)	68	68	68	68
R_{FF} (kΩ)	1	1	1	1

11.1 Design Requirements

Table 11-2 provides the parameters for the detailed design procedure example:

Table 11-2. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	13.5V (5V to 36V)
Input voltage for constant F_{SW}	8V to 18V
Output voltage	5V
Maximum output current	4A
Switching frequency	400 kHz

11.2 Detailed Design Procedure

The following design procedure applies to **Figure 6-1** and **Table 11-2**.

11.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows for the use of smaller inductors and output capacitors, hence, a more compact design.

When choosing operating frequency, the most important consideration is thermal limitations. **Figure 11-1** shows how much output current can be supported at specific ambient temperature and switching frequency. Note that power dissipation is layout dependent, so thermal resistance in any design will be different from the estimates used to generate **Figure 11-2**, which is based on a 55 mm x 60 mm, 4-layer EVM PCB design, SC81440QEVM.

Two other considerations are what maximum and minimum input voltage the part must maintain its frequency setting. Since the SC81440Q adjusts its frequency under conditions in which minimum on-time or minimum off time is applied.

If foldback is undesirable at high input voltage, then use **Equation 7**:

$$F_{SW} \le \frac{V_{OUT}}{V_{IN}(\mathrm{MAX2}) \cdot t_{ON\_MIN}(\mathrm{MAX})} \quad (7)$$

If foldback at low input voltage is a concern, use **Equation 8**:

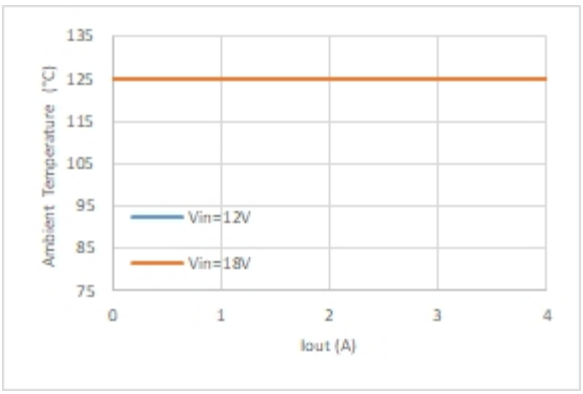
$$F_{SW} \le \frac{V_{INeff}(\mathrm{MIN2}) - V_{OUT}}{V_{INeff}(\mathrm{MIN2}) \cdot t_{OFF\_MIN}(\mathrm{MAX})} \quad (8)$$

where:

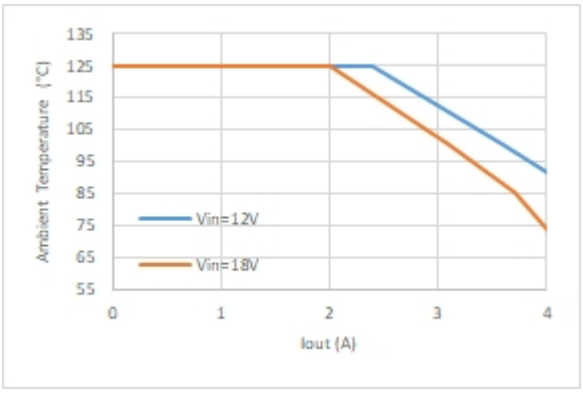
- $V_{INeff}(MIN2) = V_{IN}(MIN2) \pm I_{OUT}(MAX)*(R_{DS(ON)\_HS}(MAX) + DCR(MAX))$
- $V_{IN}(MIN2)$, $V_{IN}(MAX2)$ = see *Input voltage for constant F_{SW}* in **Table 11-2**
- DCR(MAX) = maximum DCR of the inductor
- $t_{OFF\_MIN}(MAX)$ = see **Section 8.5**
- $R_{DS(ON)\_HS}(MAX)$ = see **Section 8.5**

The fourth constraint is the rated frequency range of the IC. See f_{ADJ} in **Section 8.5**. All previously stated constraints (thermal, $V_{IN}(MAX2)$, $V_{IN}(MIN2)$, and device-specified frequency range) must be considered when selecting frequency.

Many applications require that the AM band can be avoided. These applications tend to operate at either 400 kHz below the AM band or 2.1 MHz above the AM band. In this example, 400 kHz is chosen.



(a) F_{SW} = 400 kHz V_{OUT} = 5 V



(b) F_{SW} = 2100 kHz V_{OUT} = 5 V

Figure 11-1. Maximum Ambient Temperature versus Output Current

11.2.2 Setting the Output Voltage

The output voltage of SC81440Q is externally adjustable using a resistor divider network. The range of recommended output voltage is found in **Section 8.3**. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light load efficiency. The recommended value for R_{FBT} is 100 kΩ with a maximum value of 1 MΩ. Once R_{FBT} is selected, **Equation 1** is used to select R_{FBB}. For V_{OUT}=5V, R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ are chosen.

11.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current for systems with a fixed input voltage and 25% for systems with a variable input voltage such as the 12V battery in a car. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must still be used. Equation 9 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, K = 0.40 was chosen and an inductance of approximately 4.9 μH was found. The next standard value of 4.7 μH was selected.

$$L = \frac{V_{IN}-V_{OUT}}{F_{SW}\cdot K\cdot I_{OUT}(MAX)}\cdot\frac{V_{OUT}}{V_{IN}} \quad (9)$$

The saturation current rating of the inductor must be at least as large as the high-side switch current limit, $I_{L\text{-}HS}$ (see **Section 8.5**). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, $I_{L\text{-}LS}$, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage; do not allow the inductor to saturate. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powdered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1 MHz. In any case, the inductor saturation current must not be less than the device high-side current limit, $I_{L\text{-}HS}$ (see **Section 8.5**). To avoid subharmonic oscillation, the inductance value must not be less than that given in **Equation 10**. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L \geq 0.32\cdot\frac{V_{OUT}}{F_{SW}} \quad (10)$$

Equation 10 assumes that this design must operate with input voltage near or in dropout. If minimum operating voltage for this design is high enough to limit duty factor to below 50%, **Equation 11** can be used in place of **Equation 10**.

$$L \geq 0.2\cdot\frac{V_{OUT}}{F_{SW}} \quad (11)$$

Note that choosing an inductor that is larger than the minimum inductance calculated using **Equation 9** through

Equation 11 results in less output capacitance being needed to limit output ripple but more output capacitance being needed to manage large load transients. See **Section 11.2.4**.

11.2.4 Output Capacitor Selection

The value of the output capacitor and its ESR determine the output voltage ripple and load transient performance. The output capacitor is usually determined by the load transient requirements rather than the output voltage ripple. **Table 10-3** can be used to find the output capacitor and C_{FF} selection for a few common applications. Note that a 1 kΩ R_{FF} can be used in series with C_{FF} to further improve noise performance. In this example, improved transient performance is desired giving 2 * 47 µF ceramic as the output capacitor and 220 pF as C_{FF}.

Table 10-3. Recommended Output Ceramic Capacitors and C_{FF} Values

F_{SW}	Transient Performance	3.3 V O_{UTPUT}		5 V O_{UTPUT}	
		Cera C_{OUT}	C_{FF}	Cera C_{OUT}	C_{FF}
2100 kHz	Minimum	3*22µF	68pF	2*22µF	68pF
2100 kHz	Better Transient	2*47µF	100pF	3*22µF	100pF
400 kHz	Minimum	4*22µF	68pF	3*22µF	68pF
400 kHz	Better Transient	3*47µF	100pF	4*22µF	100pF

Most ceramic capacitors deliver far less capacitance than the rating of the capacitor indicates. Be sure to check any capacitor selected for initial accuracy, temperature derating, and voltage derating. **Table 10-3** have been generated assuming typical derating for 16 V, X7R, automotive grade capacitors. If lower voltage, non-automotive grade, or lower temperature rated capacitors are used, more capacitors than listed are likely to be needed.

11.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10 µF of ceramic capacitance is required on the input of the device. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100 nF ceramic capacitor must be used at each input/ground pin pair, VIN1/PGND1 and VIN2/PGND2, immediately adjacent to the converter. This provides a high-frequency bypass for the control circuits internal to the device. These capacitors also suppress SW node ringing, which reduces the maximum voltage present on the SW node and EMI. The 2 * 100 nF must also be rated at 50 V with an X7R or better dielectric. The QFN package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split, and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. In this example, 2 * 4.7 µF and 2 * 100 nF ceramic capacitors are used, one at each VIN/PGND location.

Many times, it is desirable and necessary to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the converter. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitors. The approximate worst-case RMS value of this current can be calculated from **Equation 12** and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \approx \frac{I_{OUT}}{2} \quad (12)$$

11.2.6 BOOT Capacitor

The SC81440Q requires a bootstrap capacitor connected between the CBOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the high-side power MOSFET. A high-quality (X7R) ceramic capacitor of 100 nF and at least 10 V is required.

11.2.7 BOOT Resistor

A BOOT resistor can be connected between the CBOOT and RBOOT pins. Unless EMI for the application being designed is critical, these two pins can be shorted. A 100 Ω resistor between these pins eliminates overshoot. To maximize efficiency, 0 Ω is chosen for this example. Under most circumstances, selecting an RBOOT resistor value above 100 Ω is undesirable since the resulting small improvement in EMI is not enough to justify further decreased efficiency.

11.2.8 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the converter. This output requires a 1 µF, 16 V ceramic capacitor connected from VCC to AGND for proper operation. In general, avoid loading this output

with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see **Section 10.5**). A pullup resistor with a value of 100 kΩ is a good choice in this case.

Note, VCC remains high when VEN_WAKE< EN < VEN. The nominal output voltage on VCC is 3.3 V. Do not short this output to ground or any other external voltage.

11.2.9 BIAS

Because VOUT = 5 V in this design, the BIAS pin is tied to VOUT to reduce LDO power loss. The output voltage is supplying the LDO current instead of the input voltage. The power saving is $I_{LDO} \times (V_{IN} - V_{OUT})$. The power saving is more significant when $V_{IN} >> V_{OUT}$ and with higher frequency operation. To prevent V_{OUT} noise and transients from coupling to BIAS, a series resistor, 1 Ω to 10 Ω, can be added between V_{OUT} and BIAS. A bypass capacitor with a value of 1 μF or higher can be added close to the BIAS pin to filter noise. Note the maximum allowed voltage on the BIAS pin is 12 V.

11.2.10 C_{FF} and R_{FF} Selection

A feedforward capacitor, C_{FF}, is used to improve phase margin and transient response of circuits which have output capacitors with low ESR. Since this capacitor can conduct noise from the output of the circuit directly to the FB node of the IC, a 1 kΩ resistor, R_{FF}, can be placed in series with C_{FF}. If the ESR zero of the output capacitor is below 200 kHz, no C_{FF} must be used.

If output voltage is less than 2.5 V, C_{FF} has little effect, so it can be omitted. If output voltage is greater than 14 V, C_{FF} must not be used since it introduces too much gain at higher frequencies.

11.2.11 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in **Figure 11-2**. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then **Equation 13 and 14** is used to calculate R_{ENT} and V_{OFF}:

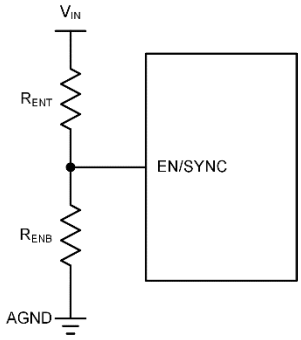


Figure 11-2. UVLO Using EN

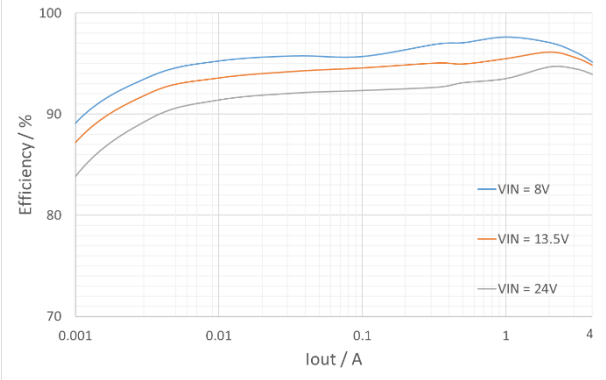
$$R_{ENT} = (\frac{V_{ON}}{V_{EN}} - 1) \cdot R_{ENB} \quad (13)$$

$$V_{OFF} = V_{ON} \cdot (1 - \frac{V_{EN-HYST}}{V_{EN}}) \quad (14)$$

where:

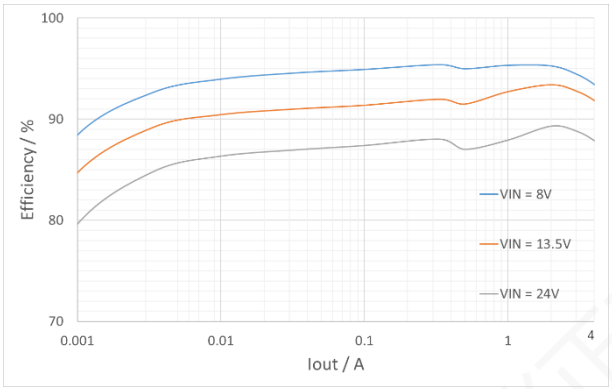
- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

11.3 Application Curves



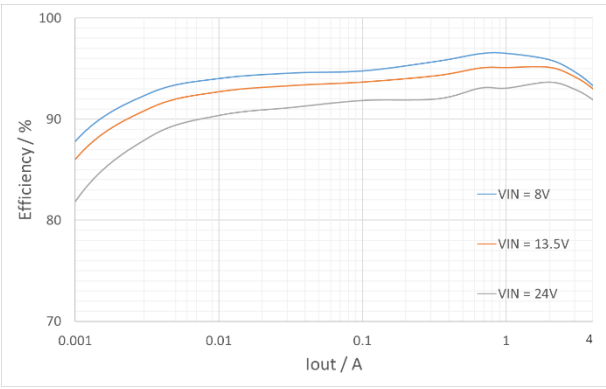
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM

Efficiency Curve



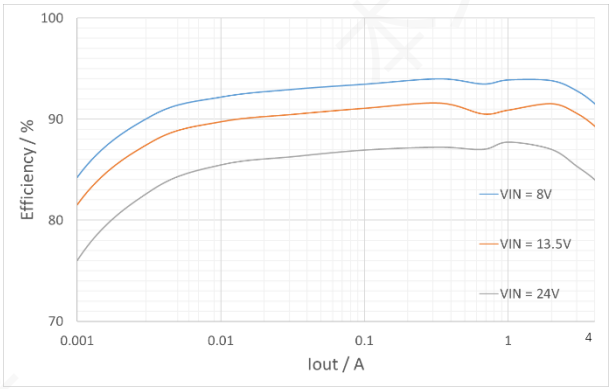
V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM

Efficiency Curve



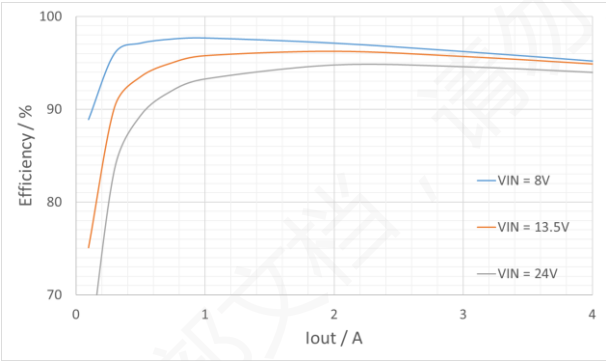
V_{OUT}=3.3V, F_{SW}=400kHz, MODE=APFM

Efficiency Curve



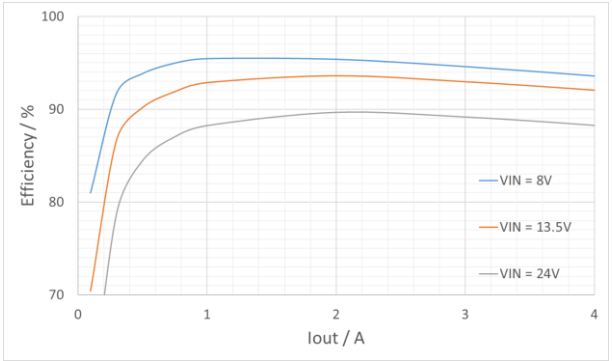
V_{OUT}=3.3V, F_{SW}=2100kHz, MODE=APFM

Efficiency Curve



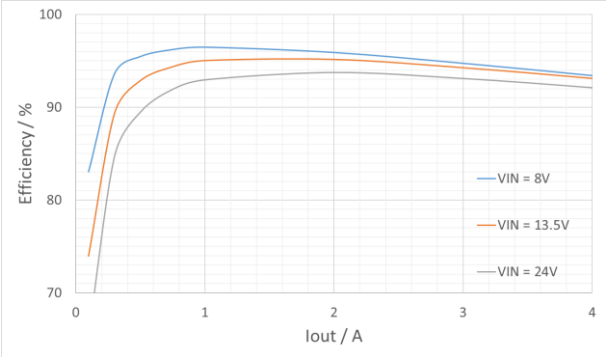
V_{OUT}=5V, F_{SW}=400kHz, MODE=FPWM

Efficiency Curve



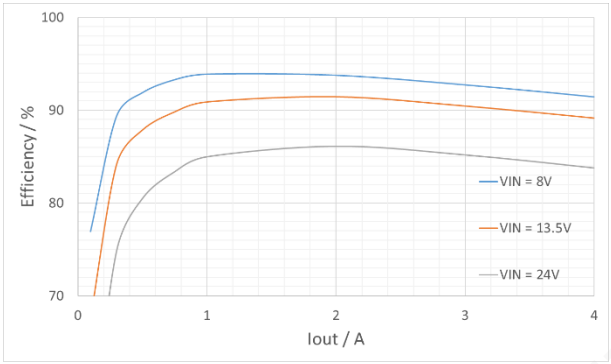
V_{OUT}=5V, F_{SW}=2100kHz, MODE= FPWM

Efficiency Curve



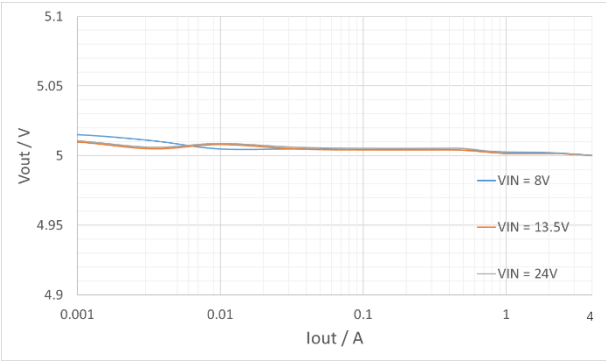
V_{OUT}=3.3V, F_{SW}=400kHz, MODE= FPWM

Efficiency Curve



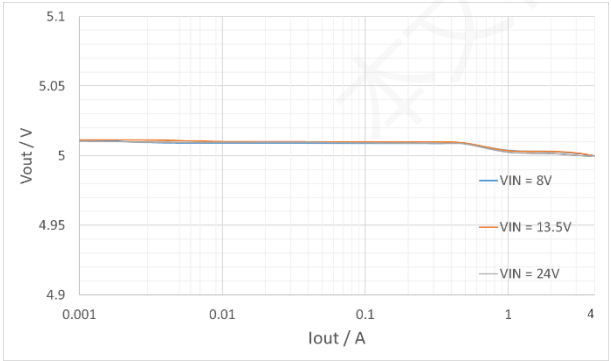
V_{OUT}=3.3V, F_{SW}=2100kHz, MODE= FPWM

Efficiency Curve



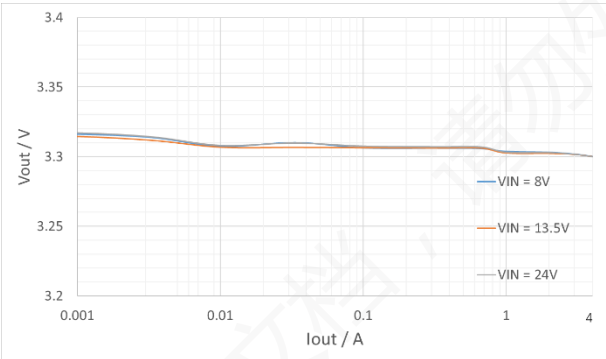
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM

Line and Load Regulation



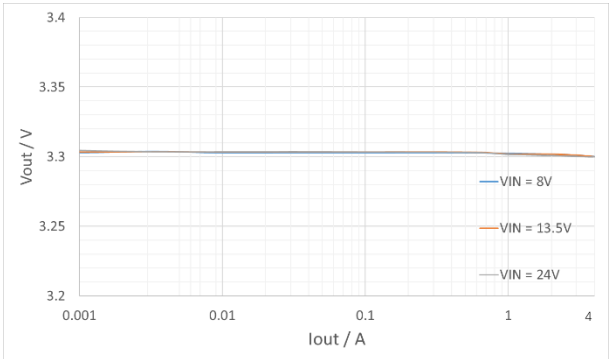
V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM

Line and Load Regulation



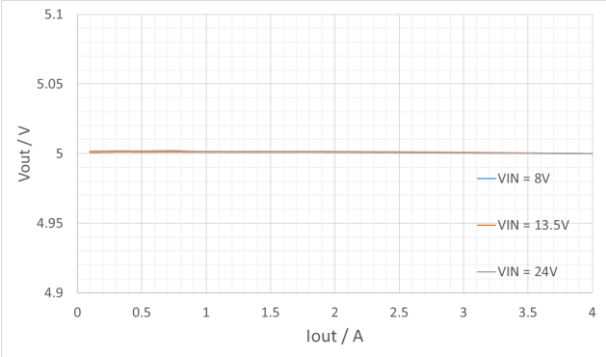
V_{OUT}=3.3V, F_{SW}=400kHz, MODE=APFM

Line and Load Regulation



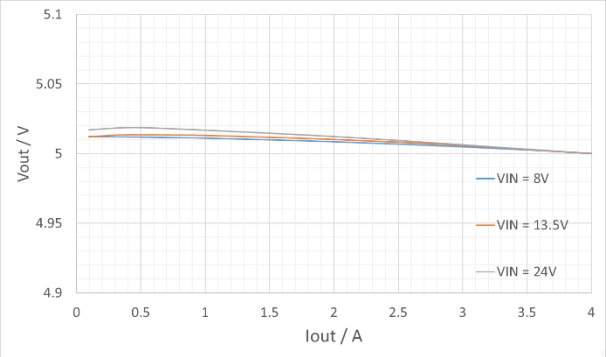
V_{OUT}=3.3V, F_{SW}=2100kHz, MODE=APFM

Line and Load Regulation



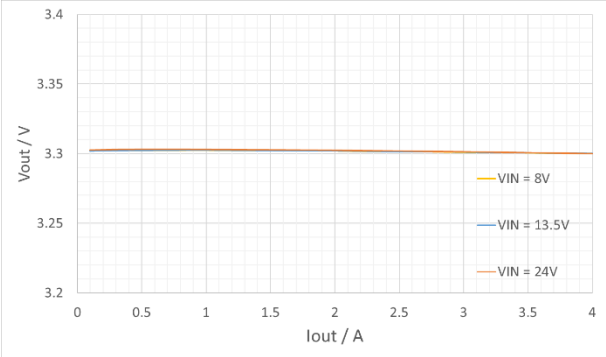
V_{OUT}=5V, F_{SW}=400kHz, MODE=FPWM

Line and Load Regulation



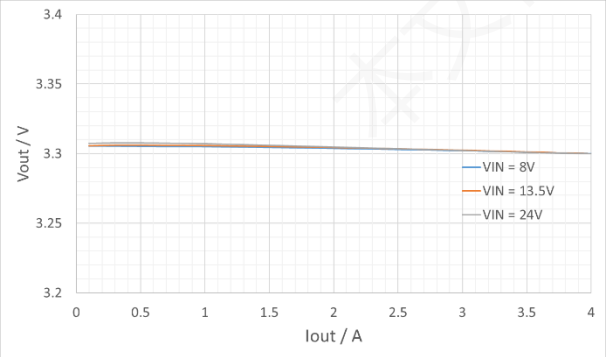
V_{OUT}=5V, F_{SW}=2100kHz, MODE= FPWM

Line and Load Regulation



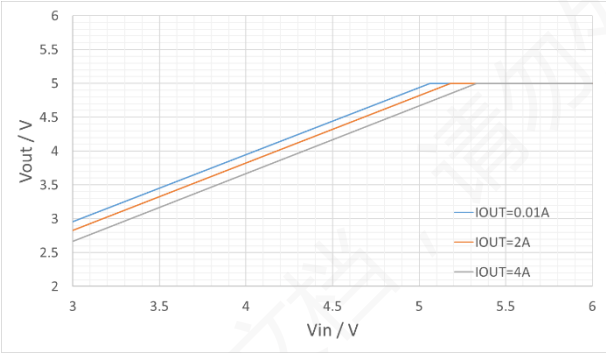
V_{OUT}=3.3V, F_{SW}=400kHz, MODE= FPWM

Line and Load Regulation



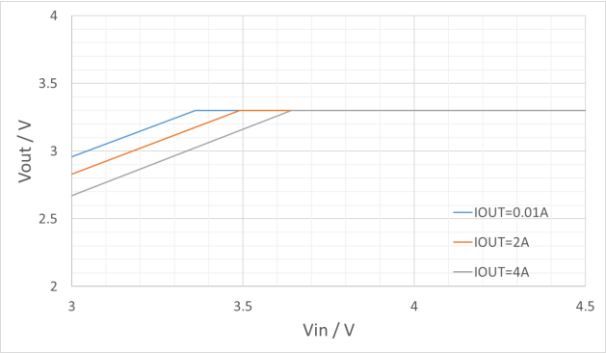
V_{OUT}=3.3V, F_{SW}=2100kHz, MODE= FPWM

Line and Load Regulation



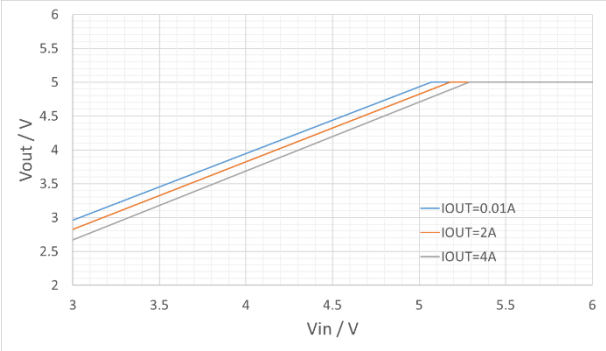
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM

Dropout Curve



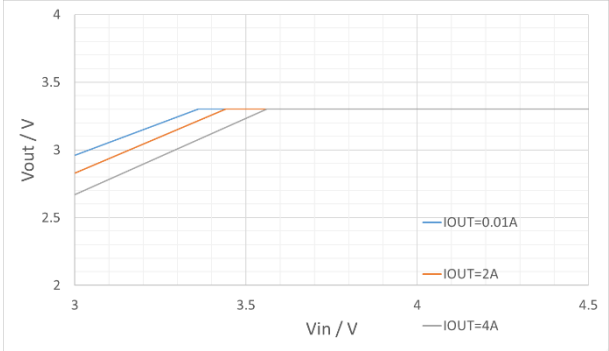
V_{OUT}=3.3V, F_{SW}=400kHz, MODE=APFM

Dropout Curve



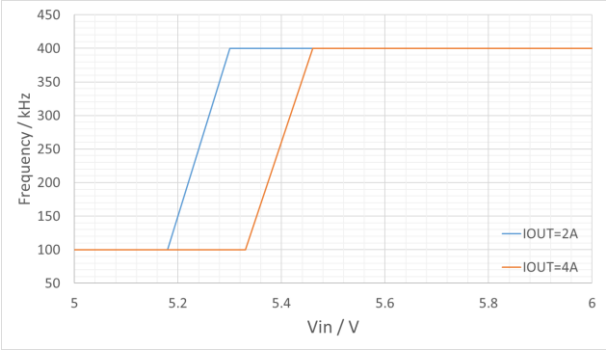
V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM

Dropout Curve



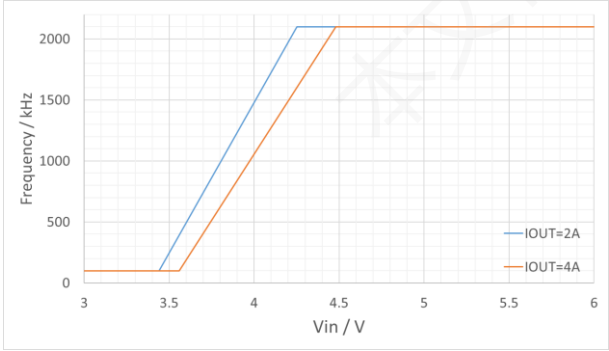
V_{OUT}=3.3V, F_{SW}=2100kHz, MODE=APFM

Dropout Curve



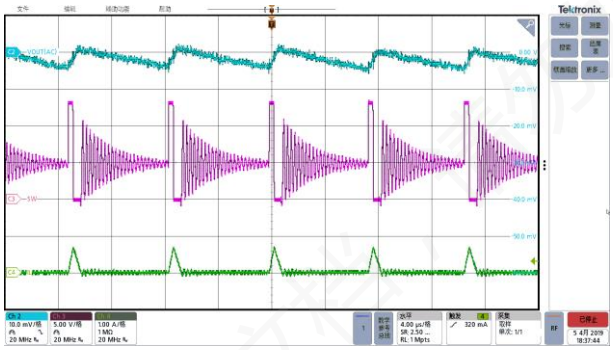
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM

Frequency Dropout



V_{OUT}=3.3V, F_{SW}=2100kHz, MODE=APFM

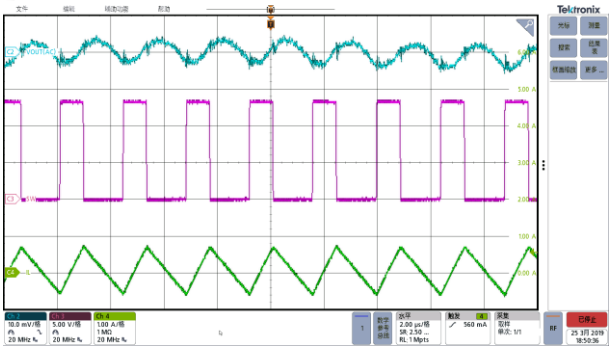
Frequency Dropout



V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM, I_{OUT}=50mA

Cout=4*22μF

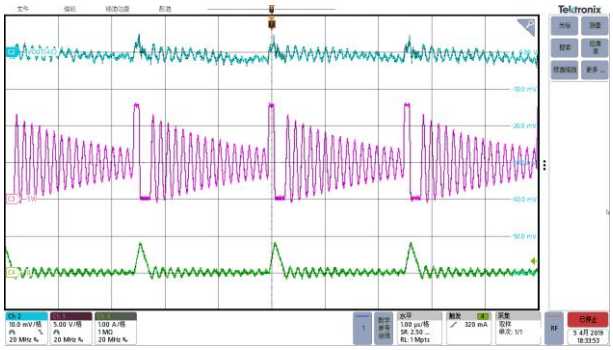
Switching Waveform and V_{OUT} Ripple



V_{OUT}=5V, F_{SW}=400kHz, MODE=FPWM, I_{OUT}=50mA

Cout=4*22μF

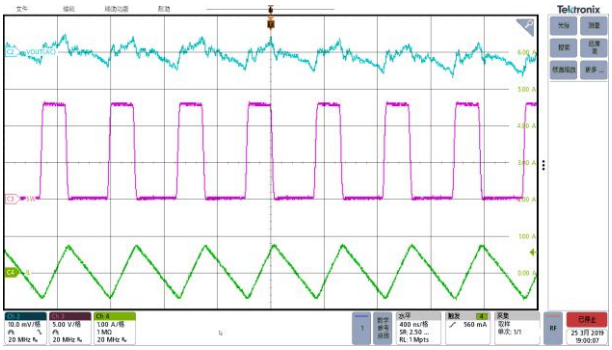
Switching Waveform and V_{OUT} Ripple



V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM, I_{OUT}=50mA

Cout=4*22μF

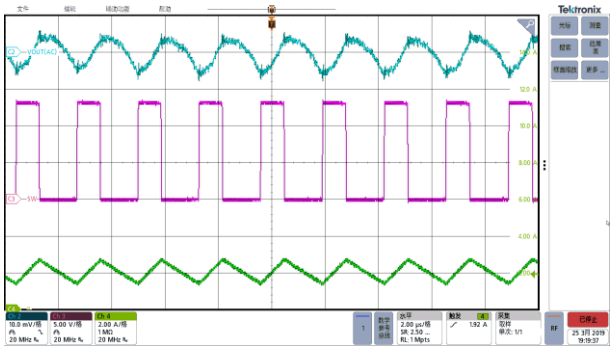
Switching Waveform and V_{OUT} Ripple



V_{OUT}=5V, F_{SW}=2100kHz, MODE=FPWM, I_{OUT}=50mA

Cout=4*22μF

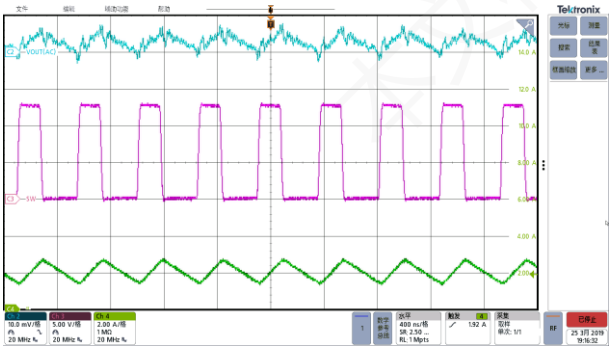
Switching Waveform and V_{OUT} Ripple



V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM, I_{OUT}=2A

Cout=4*22μF

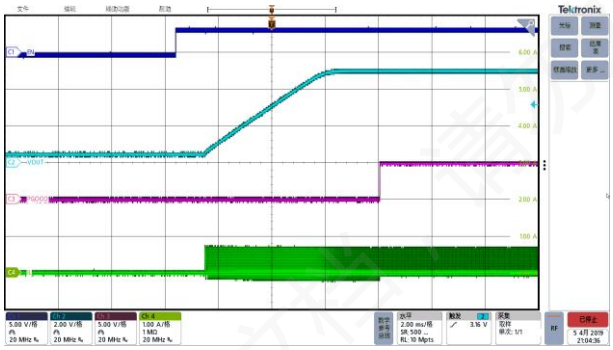
Switching Waveform and V_{OUT} Ripple



V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM, I_{OUT}=2A

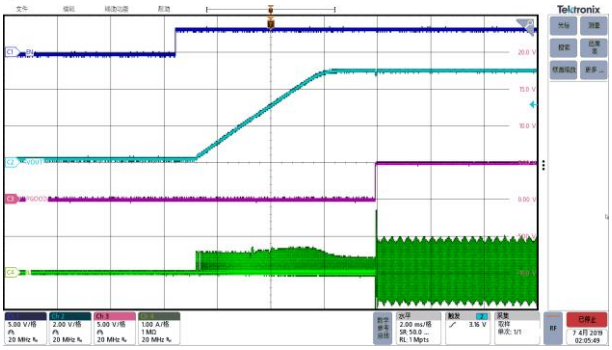
Cout=4*22μF

Switching Waveform and V_{OUT} Ripple



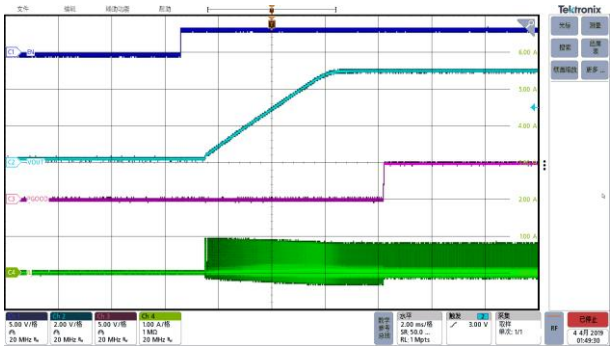
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM

tart-up with 50mA Load



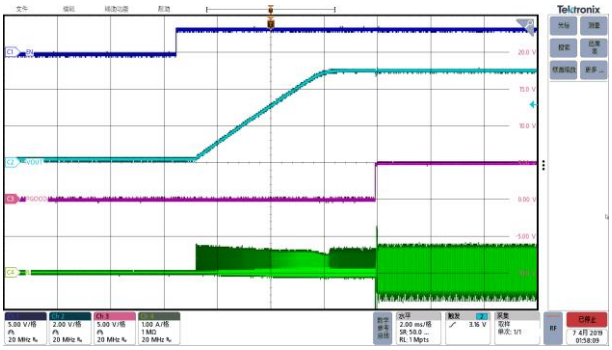
V_{OUT}=5V, F_{SW}=400kHz, MODE=FPWM

Start-up with 50mA Load



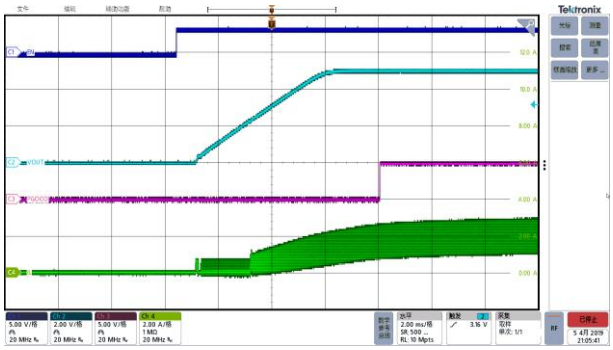
V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM

tart-up with 50mA Load



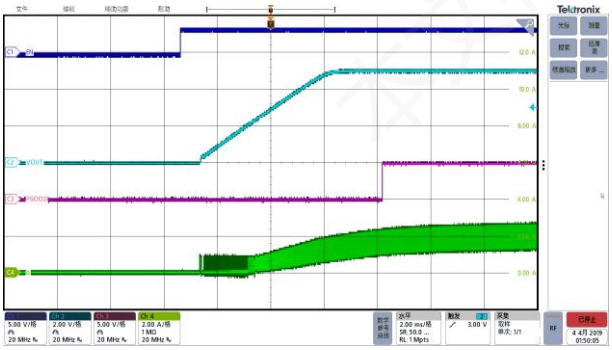
V_{OUT}=5V, F_{SW}=2100kHz, MODE=FPWM

Start-up with 50mA Load



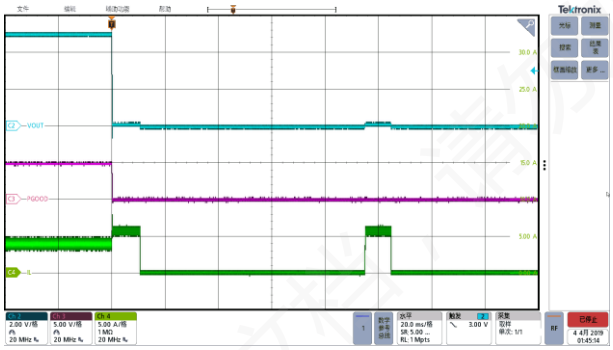
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM

Start-up with 2A Load



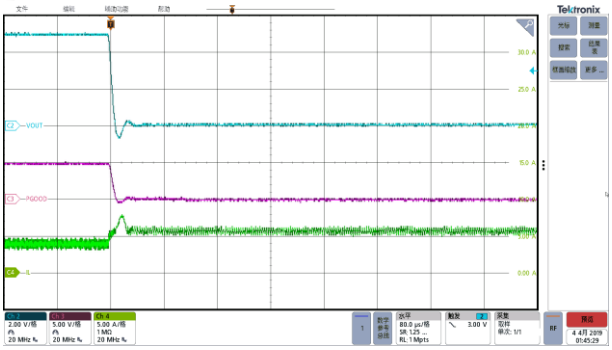
V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM

Start-up with 2A Load



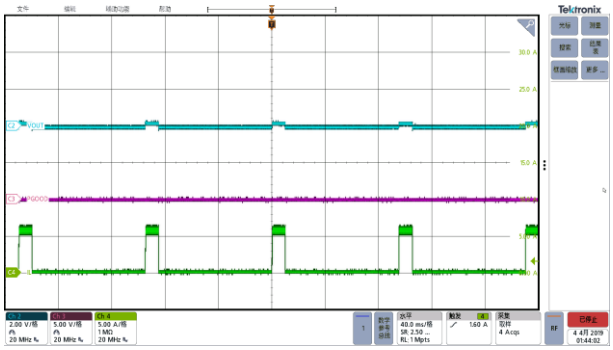
V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM, I_{OUT}=4A

Enter Hiccup



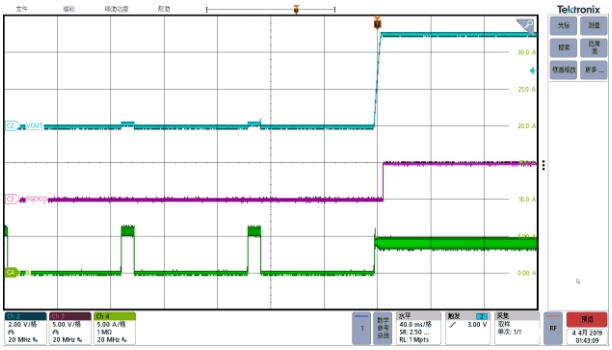
V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM, I_{OUT}=4A

Recovery from Hiccup



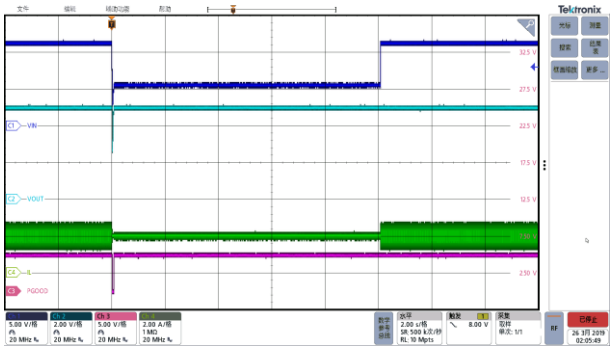
V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM, I_{OUT}=4A

Keep Hiccup



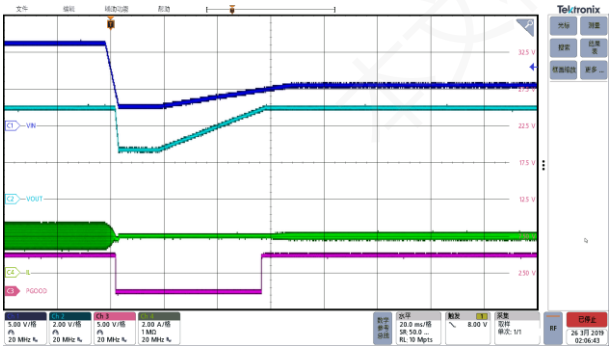
V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM, I_{OUT}=4A

Recovery from Hiccup



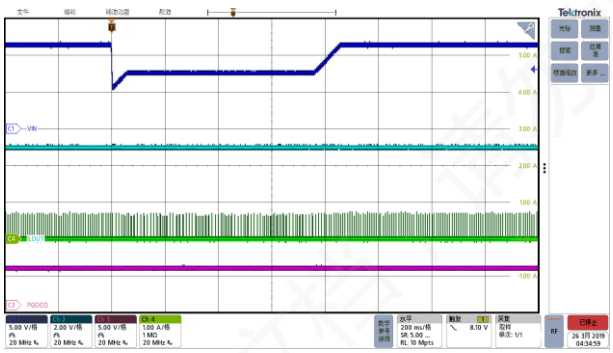
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM, I_{OUT}=2A

Cold Crank Test



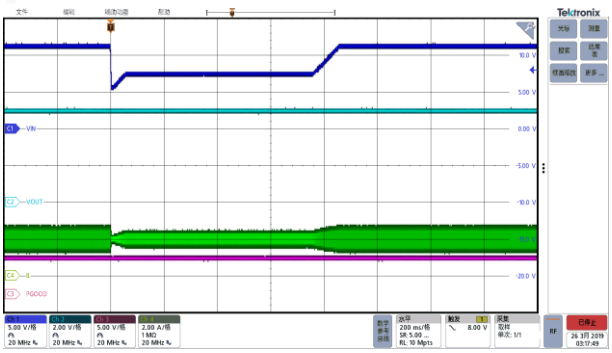
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM, I_{OUT}=2A

Cold Crank Test (Zoomin)



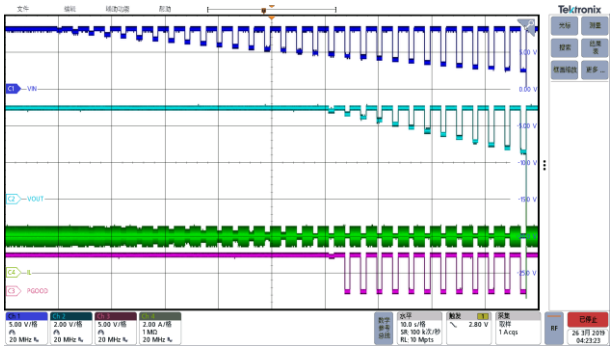
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM, I_{OUT}=0A

Warm Crank Test



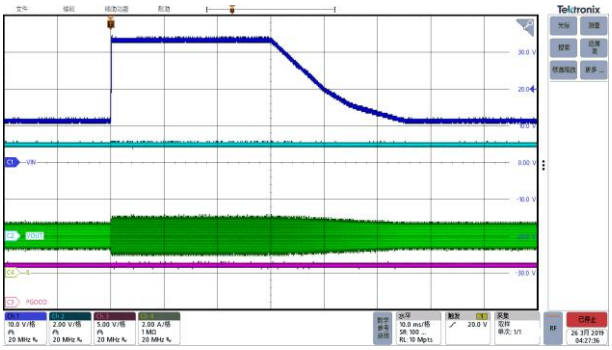
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM, I_{OUT}=2A

Warm Crank Test



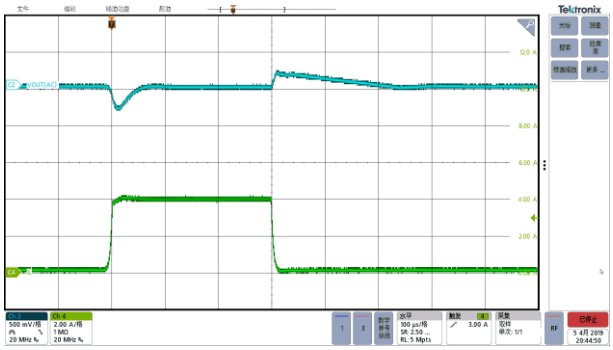
V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM, I_{OUT}=2A

Waterfall Test



V_{OUT}=5V, F_{SW}=400kHz, MODE=APFM, I_{OUT}=2A

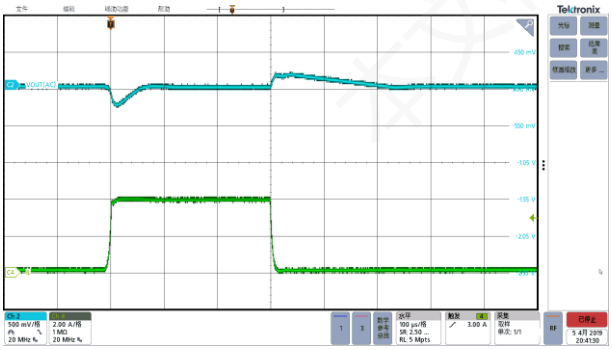
Suppressed Load Dump Test



V_{OUT}=3.3V, F_{SW}=400kHz, MODE=APFM

I_{OUT}=0.1A->4A->0.1A, T_r=T_f=5μs

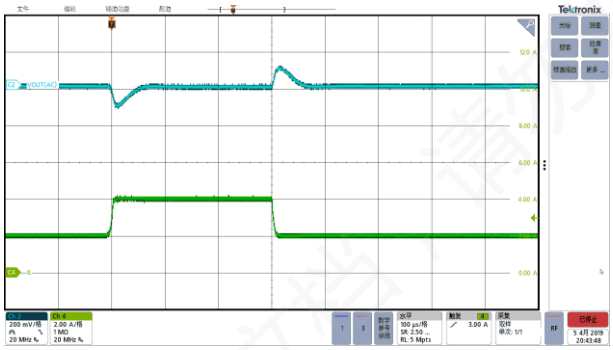
Load Transient Performance



V_{OUT}=3.3V, F_{SW}=2100kHz, MODE=APFM

I_{OUT}=0.1A->4A->0.1A, T_r=T_f=5μs

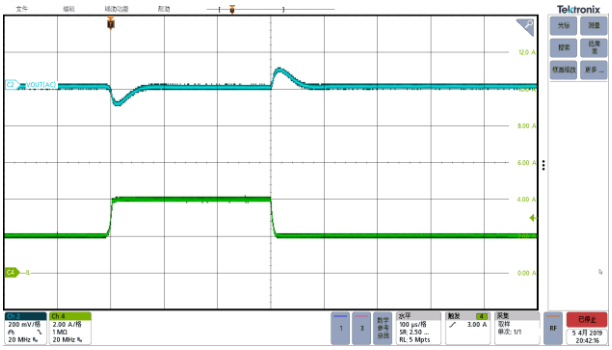
Load Transient Performance



V_{OUT}=3.3V, F_{SW}=400kHz, MODE=APFM

I_{OUT}=2A->4A->2A, T_r=T_f=4μs

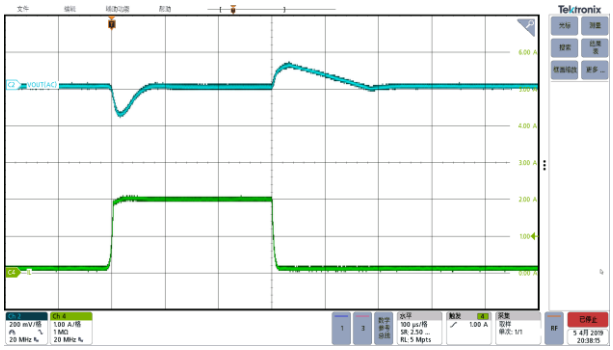
Load Transient Performance



V_{OUT}=3.3V, F_{SW}=2100kHz, MODE=APFM

I_{OUT}=2A->4A->2A, T_r=T_f=4μs

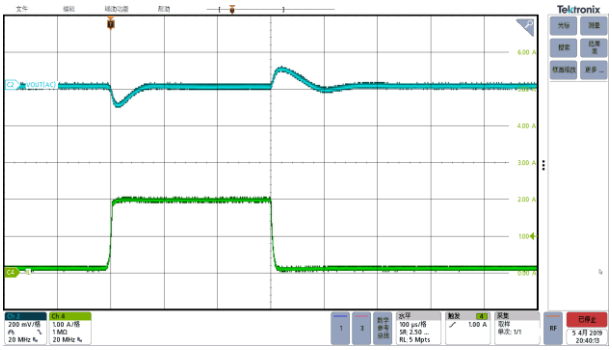
Load Transient Performance



V_{OUT}=3.3V, F_{SW}=2100kHz, MODE=APFM

I_{OUT}=0.1A->2A->0.1A, T_r=T_f=3μs

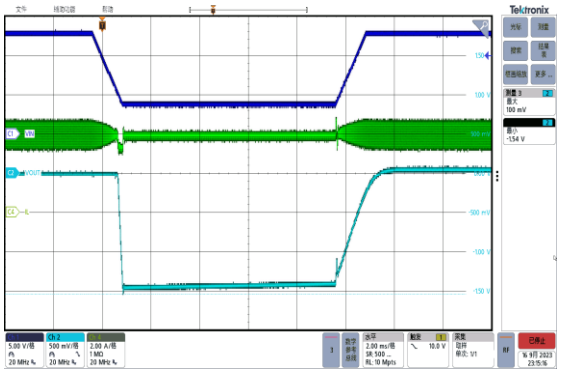
Load Transient Performance



V_{OUT}=3.3V, F_{SW}=2100kHz, MODE=FPWM

I_{OUT}=0.1A->2A->0.1A, T_r=T_f=3μs

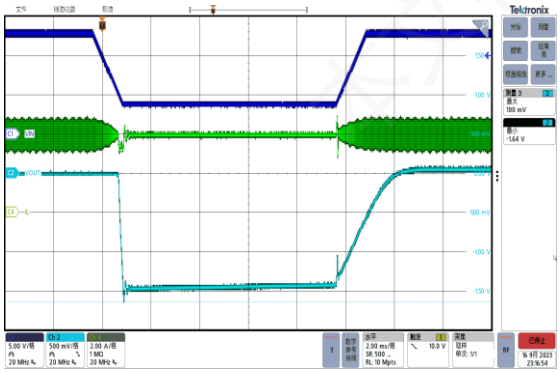
Load Transient Performance



V_{OUT}=5V, F_{SW}=2100kHz, MODE=APFM, I_{OUT}=4A

Vin=13.5V->4V->13.5V, T_r=T_f=1ms

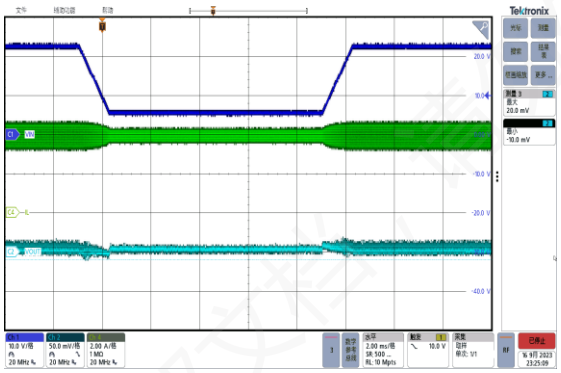
Line Transient Performance



V_{OUT}=5V, F_{SW}=400kHz, MODE=FPWM, I_{OUT}=4A

Vin=13.5V->4V->13.5V, T_r=T_f=1ms

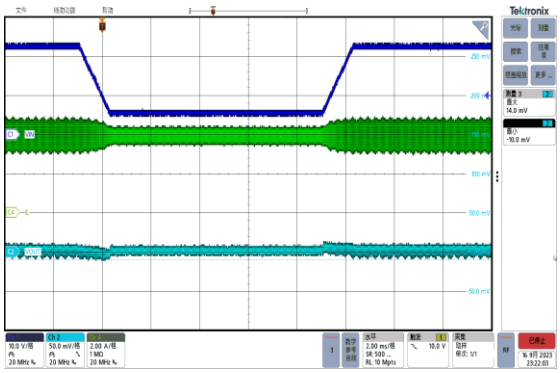
Line Transient Performance



V_{OUT}=3.3V, F_{SW}=2100kHz, MODE=APFM, I_{OUT}=4A

Vin=24V->6V->24V, T_r=T_f=1ms

Line Transient Performance



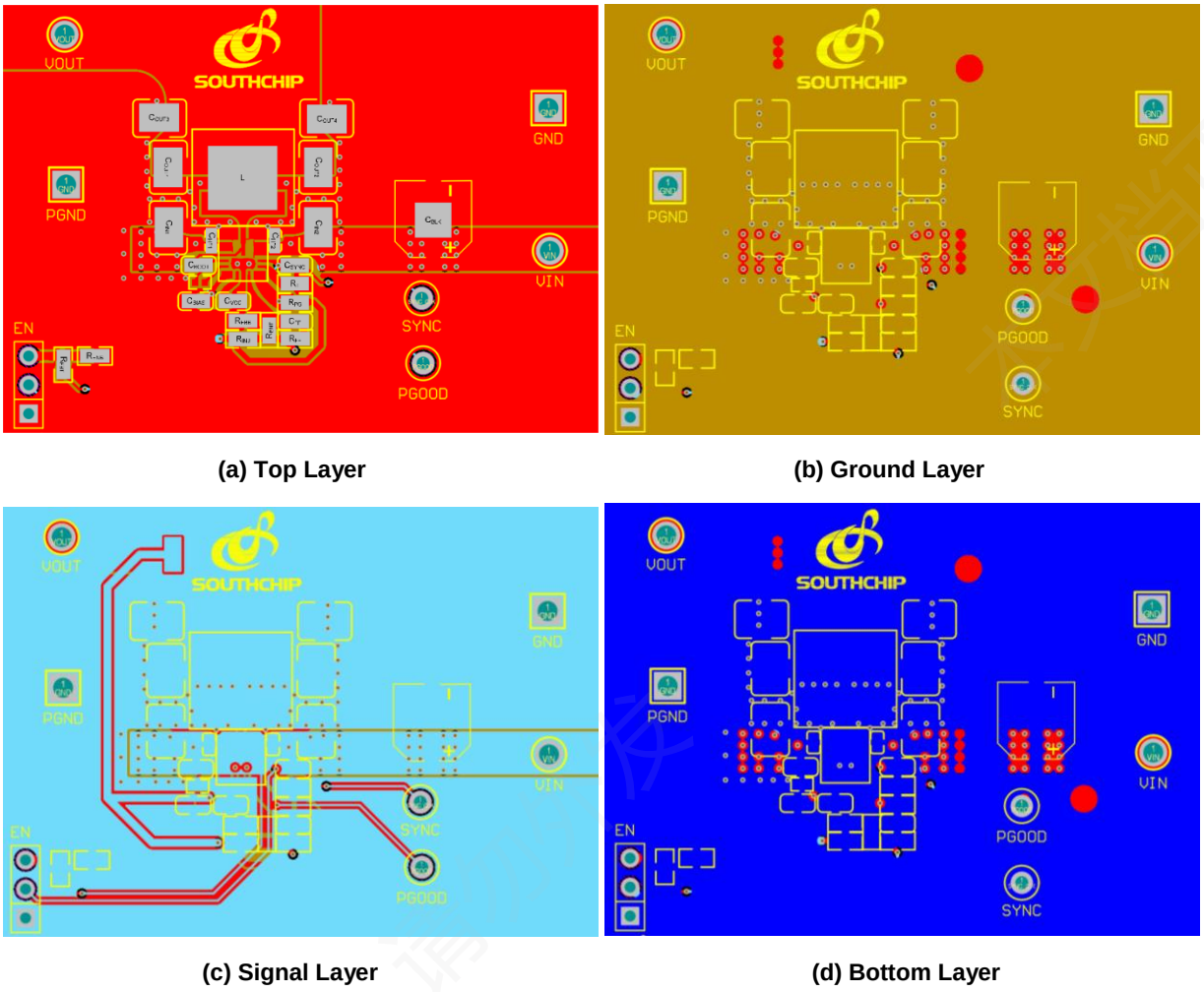
V_{OUT}=3.3V, F_{SW}=400kHz, MODE=FPWM, I_{OUT}=4A

Vin=24V->6V->24V, T_r=T_f=1ms

Line Transient Performance

12 Layout Guide

The PCB layout is critical to get the optimal performance of DC-DC converter. A good PCB layout can improve the robustness and EMI performance of design. For SC81440Q, a buck converter, the loop consisting of power supply, input capacitors and power ground is the most important loop. Because this loop carries the input transient currents that cause the input voltage transient at input capacitors. Bad layout means larger trace inductance that can cause larger voltage transient. Generally, to reduce the PCB inductance, the area of this loop must be small, and the trace must be wide. **Figure 12-1** shows a recommended layout.



(a) Top Layer **(b) Ground Layer**

(c) Signal Layer **(d) Bottom Layer**

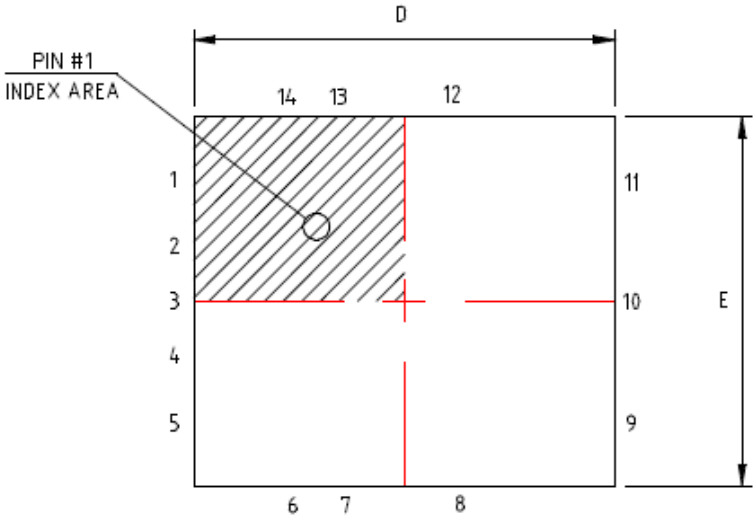
Figure 12-1. Layout Example

- Maintain continuous copper pour under chip to ensure proper thermal and EMI performance.
- Place the input capacitor or capacitors as close as possible input pin pairs, and use a wide VIN plane on a lower layer to connect both of the VIN pairs together to the input supply. With the QFN package, there are two VIN/PGND pairs on either side of the package, VIN1 to PGND1 and VIN2 to PGND2, which provides for a symmetrical layout and helps minimize switching noise and EMI generation.
- The VIN, VOUT, and GND paths must be wide and direct as possible to reduce any voltage drops on the input or output paths of the converter and maximizes efficiency.

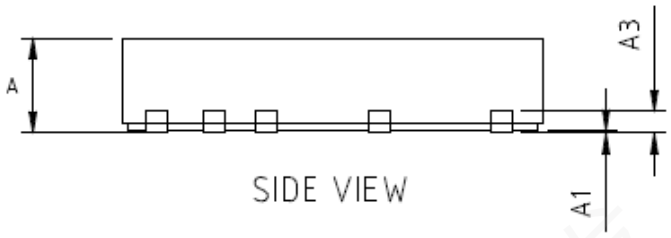
- Layer of the PCB beneath the top layer with the IC must be a ground plane. This plane acts as a noise shield and a heat dissipation path. Using the layer directly next to the IC reduces the inclosed area in the input circulating current in the input loop, reducing inductance.
- Place C_{VCC} close to the VCC and AGND pins. This capacitor must be routed with short, wide traces to the VCC and AGND pins.
- Place C_{BOOT} close to the CBOOT pin, and use wide traces to rout them. It is important to route the SW connection under the device through the gap between VIN2 and RBOOT pins, reducing exposed SW node area.
- If an R_{BOOT} resistor is used, place as close as possible to CBOOT and RBOOT pins. If high efficiency is desired, RBOOT and CBOOT pins can be shorted, and this short must be placed as close as possible to RBOOT and CBOOT pins.
- Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.
- Place R_{FBB}, R_{FBT}, R_{FF}, and C_{FF}, if used, as close as possible to the device. The connections to FB and AGND through RFBB must be short and close to those pins on the device. The connection to VOUT can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the converter.
- Provide enough PCB area for proper heat sinking. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces must be used for all pins except where noise considerations dictate minimization of area.

MECHANICAL DATA

QFN-14

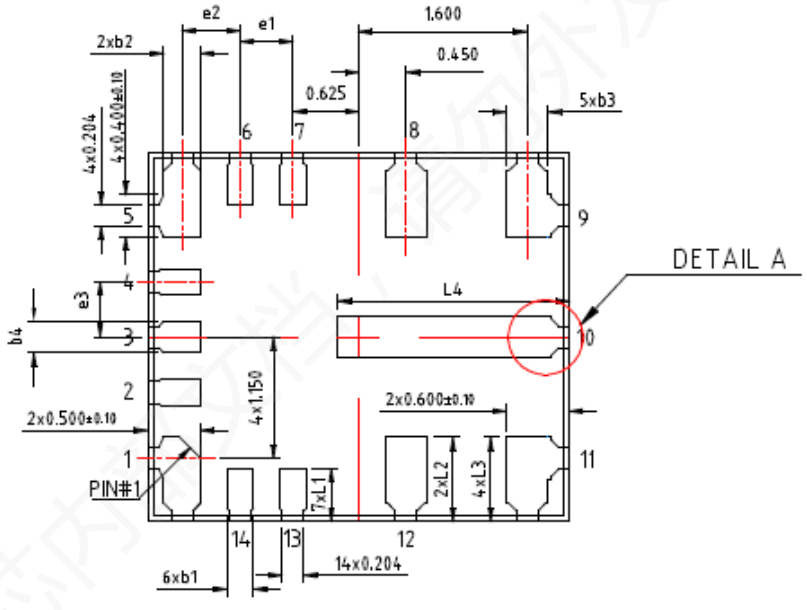


TOP VIEW

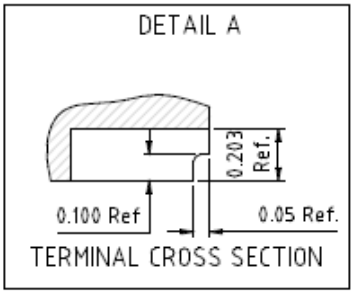


SIDE VIEW

Thickness / Symbol	Dimension Table		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.203 Ref.	---
b1	0.20	0.25	0.30
b2	0.30	0.35	0.40
b3	0.35	0.40	0.45
b4	0.25	0.30	0.35
D	3.90	4.00	4.10
E	3.40	3.50	3.60
e1	0.50 BSC		
e2	0.55 BSC		
e3	0.525 BSC		
L1	0.40	0.50	0.60
L2	0.70	0.80	0.90
L3	0.70	0.80	0.90
L4	2.10	2.20	2.30



BOTTOM VIEW



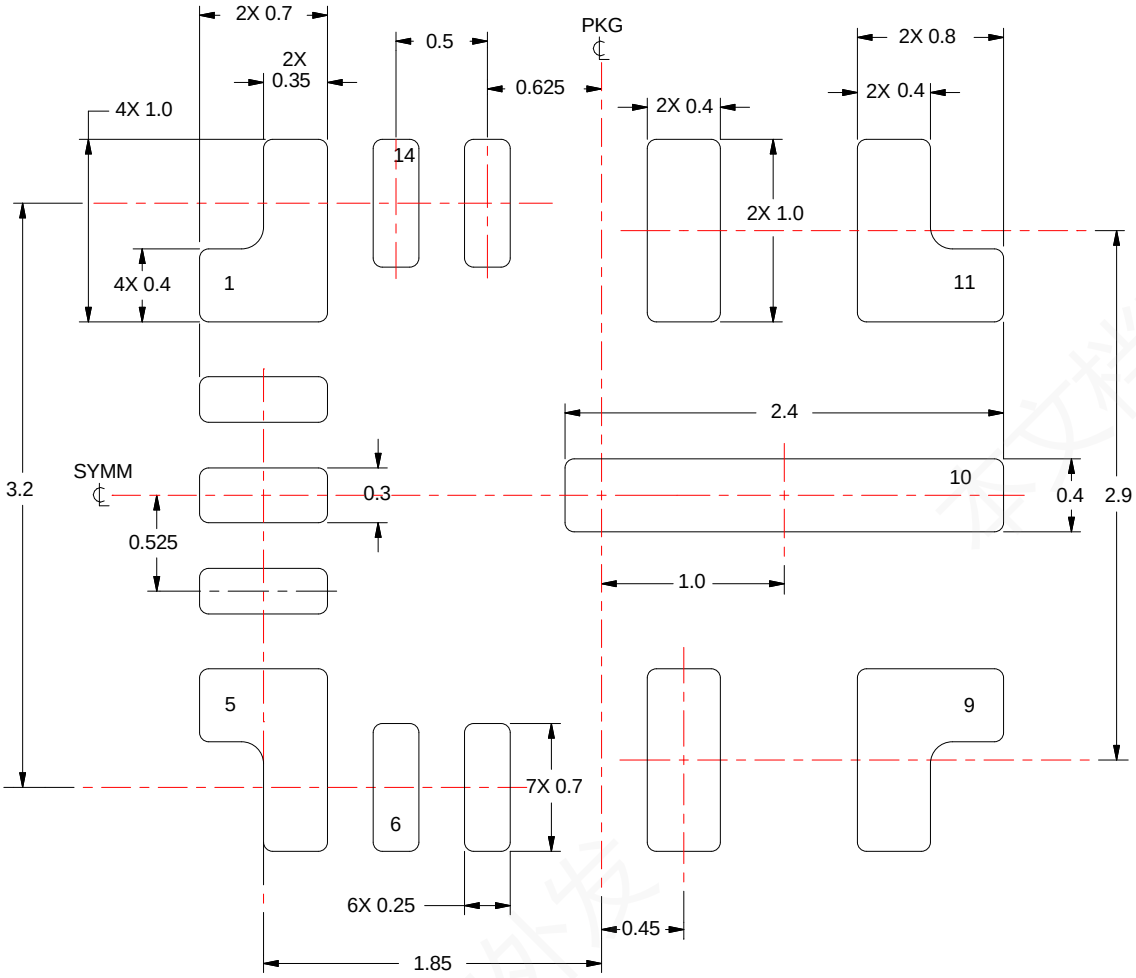
Wettable Flanks :

☑ Yes

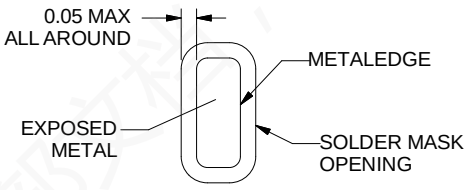
☐ No

RECOMMENDED FOOTPRINT

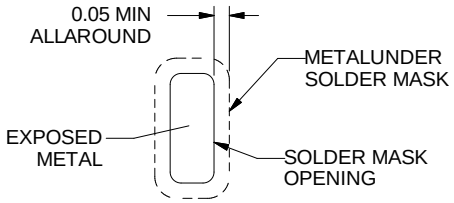
QFN-14



LAND PATTERN



NON SOLDER MASK DEFINED

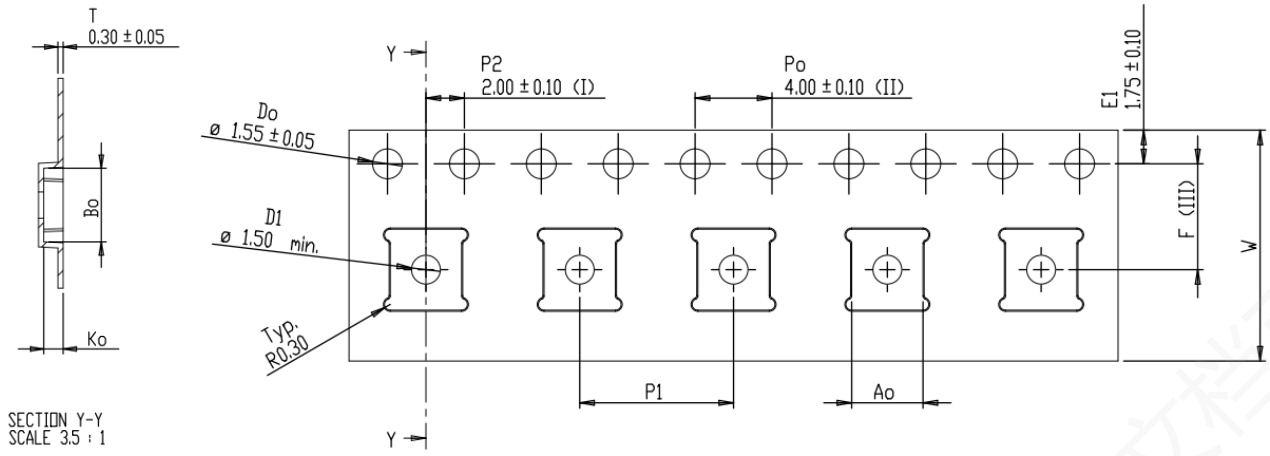


SOLDER MASK DEFINED

Unit： mm

TAPE AND REEL INFORMATION

QFN-14 Carrier Tape

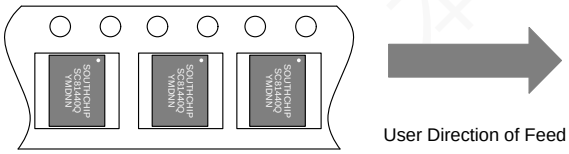


UNIT: MM

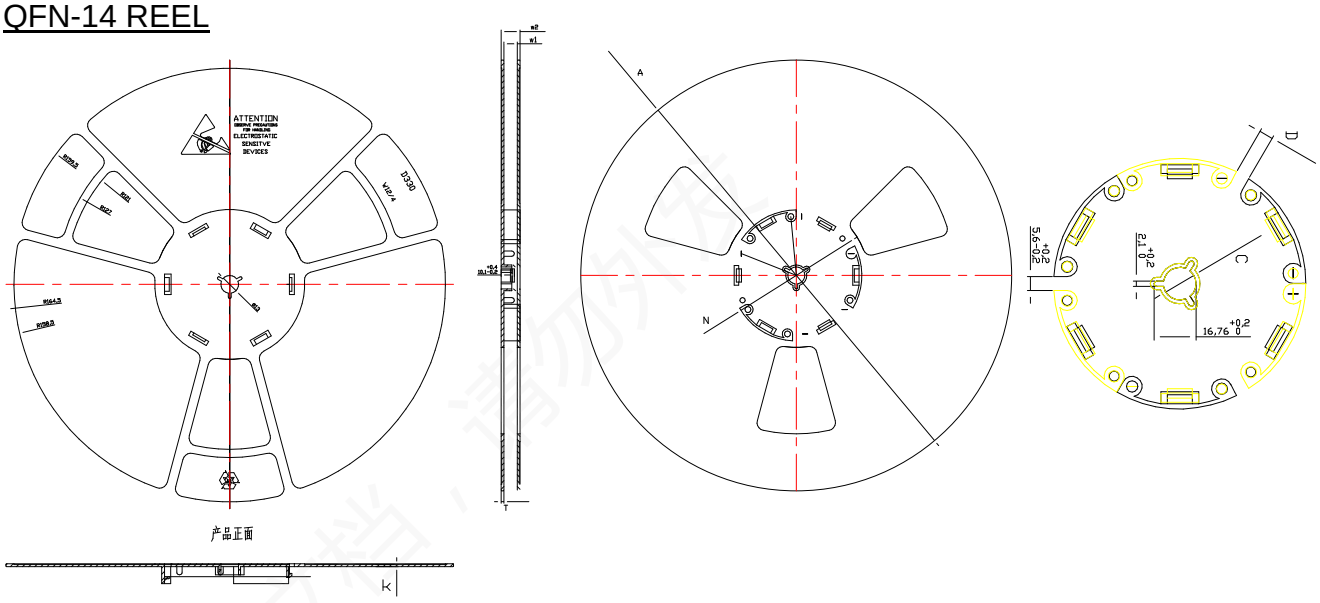
Ao	3.71	+/- 0.10
Bo	4.21	+/- 0.10
Ko	1.11	+/- 0.10
F	5.50	+/- 0.10
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

Unit Orientation In Pocket



QFN-14 REEL



UNIT: MM

TYPE	A	N	C	D	w1	w2	T	k
12MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	12.4 +2 -0	16.6 +2 -0	2.1±0.15	1.4 +0.15 -0.1

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