High Efficiency 24V 6.5A Synchronous Buck Converter with FCCM Mode

1 Descriptions

SC81360F is a high-efficiency synchronous buck converter with few external components and is easy to use in compact applications. The device operates with input voltages from 4V to 24V with a typical switching frequency of 700kHz. It integrates power MOSFETs and can support up to 6.5A continuous output current.

The device adopts a constant on-time control mode with internal compensation, which features excellent load transient performance and supports low equivalent series resistance output capacitors such as ceramic (MLCC) capacitors. It can operate in the 100% duty cycle to offer a low input-to-output voltage differential when the VIN equals VOUT.

The device operates in forced CCM Mode, delivering low output ripple and fast transient response under light load.

SC81360F provides protections, including input under-voltage protection, cycle-by-cycle peak current limitation, and thermal shutdown protection with auto-recovery.

SC81360F is available in QFN-11(2mmx2mm) Package.

2 Features

- 4~24V Input Voltage Range
- 0.6V Reference with ±1% Accuracy
- Max 6.5A Continuous Output Current
- Forced CCM Mode Operation
- Integrated 27mΩ/11mΩ MOSFET
- Low Dropout Mode with Almost 100% Duty Cycle
- 700K Switching Frequency
- COT with Fast Load Transient Performance
- Internal Soft Start
- Power Good Pin
- Cycle-by-Cycle Valley and Peak Current Limit
- Output Discharge via SW pin
- Short Circuit Protection with Hiccup Mode
- Input OVP
- ULVO, OUTOVP, TSD Protection (Non-Latch)
- QFN2X2 Package Available

3 Applications

- Flat Panel Television and Monitors
- Set-Top Boxes
- HUB
- Portable Devices

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC81360FQFBR	QFN-11	2.00mm x 2.00mm

5 Typical Application Circuit

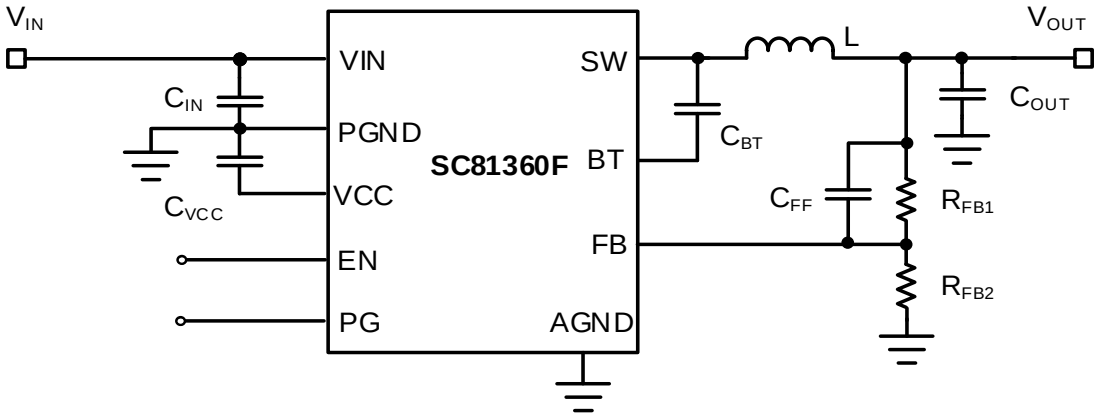
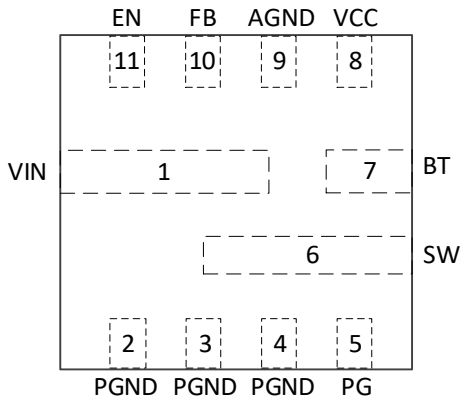


Figure. 1 Typical application circuit

6 Terminal Configuration and Functions

TOP VIEW



QFN-11 (2mm x 2mm)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VIN	PWR	Power input node of the converter. Connect a decoupled capacitor between VIN and GND close to the IC.
2,3,4	PGND	PWR	Power ground.
5	PG	O	Open drain power good output. Connect to a voltage source with an external pull-up resistor. PG goes high when the output range is within the target value.
6	SW	PWR	Switching Node. Connect to the switch node of the power inductor.
7	BT	PWR	Connect a 220nF X7R ceramic capacitor between the BT and SW pin to provide the boosted bias voltage for the high-side gate driver.
8	VCC	O	Internal VCC LDO output. This pin supplies an internal driver and control circuit. Connect a minimum of 1μF
9	AGND	PWR	Analog ground.
10	FB	I	Feedback node of VOUT output voltage. Set the VOUT output voltage using the external resistor divider connected to this pin.
11	EN	I	Enable logic input pin. A high logic level enables the device, and a low logic level turns off the device. EN is internally pulled low.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN	-0.3	28	V
	SW	-0.3	28	V
	SW (10ns transient)	-4	30	V
	BT - SW	-0.3	6	V
	PG, VCC, FB, EN	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	VIN voltage range	4		24	V
V_{OUT}	VOUT voltage range	0.6		20	V
I_{OUT}	Continuous Output Current			6.5	A
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL RESISTANCE(1)		QFN-11 (2mm x 2mm)	UNIT
Θ_{JA}	Junction to ambient thermal resistance	75	°C/W
Θ_{JC}	Junction to case resistance	14	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.5 Electrical Characteristics

V_{IN} = 12V, T_J= -40°C to 125°C, typical values are tested at T_J= 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4		24	V
I_{VIN}	Quiescent current	V_{EN} = 3.3V, V_{FB} = 0.62V		420		μA
I_{VIN_SD}	VIN Shutdown current	V_{EN} = 0V			3	μA
POWER SWITCH						
R_{DSON_HS}	High-side MOS on resistance			27		mΩ
R_{DSON_LS}	Low-side MOS on resistance			11		mΩ
SW_{LKG}	Switch leakage	V_{EN} = 0V, V_{SW} = 0V			1	μA
VCC REGULATOR						
V_{VCC}	VCC Voltage		4.8	5	5.2	V
V_{VCC_REG}	VCC load regulation	I_{VCC} = 5mA		2		%
CURRENT LIMIT						
I_{LMT_LS}	Low-side valley current limit		5.7	7.1	8.5	A
I_{ZCD}	Zero-crossing current	V_{OUT} = 3.3V, L = 2.2μH		220		mA
I_{LMT_HS}	High-side peak current limit		8.5	11.5	14.5	A
SWITCHING FREQUENCY AND MINIMUM OFF TIMER						
F_{SW}	Switching frequency	V_{IN} = 12V, V_{OUT} = 3.3V	600	700	800	kHz
T_{MIN_ON}	Minimum on time			50		ns
T_{MIN_OFF}	Minimum off time			200		ns
T_{MAX_ON}	Maximum on time			31		μs
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
V_{OVP}	VOUT OVP threshold		125	130	135	V_{FB}%
V_{UVP}	VOUT UVP threshold		55	60	65	V_{FB}%
t_{UVPDLY}	VOUT UVP deglitch time			32		μs
V_{IN_OVP}	VIN OVP rising threshold		25.5	26.5	27.5	V
$V_{IN\_OVP\_HYS}$	VIN OVP hysteresis			1.1		V
FEEDBACK VOLTAGE AND SOFT START						
V_{FB}	Feedback regulation voltage	T_J = 25℃	594	600	606	mV

		T_J = -40℃ to 125℃	590	600	610	mV
T_{SS}			1.7	2.3	2.9	ms
ENABLE (EN) AND UNDER VOLTAGE LOCKOUT (UVLO)						
V_{EN_R}	Enable rising threshold		1.16	1.2	1.24	V
V_{EN_HYS}	Enable hysteresis			150		mV
I_{EN}	Enable input current	V_{EN} = 3.3V		3.5		μA
$V_{VCC\_UVLO\_R}$	VCC UVLO rising threshold		3.4	3.6	3.8	V
$V_{VCC\_UVLO\_HYS}$	VCC UVLO threshold hysteresis			450		mV
$V_{IN\_UVLO\_R}$	VIN UVLO rising threshold		3.7	3.9	4.1	V
$V_{IN\_UVLO\_HYS}$	VIN UVLO threshold hysteresis			500		mV
POWER GOOD						
$V_{PG\_F(FAULT)}$	PG for falling threshold (Fault)		85	90	95	$\%V_{REF}$
$V_{PG\_R(GOOD)}$	PG for rising threshold (Good)		90	95	100	$\%V_{REF}$
$V_{PG\_R(FAULT)}$	PG for rising threshold (Fault)		110	115	120	$\%V_{REF}$
$V_{PG\_F(GOOD)}$	PG for falling threshold (Good)		100	105	110	$\%V_{REF}$
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			155		°C
	Thermal shutdown hysteresis			20		°C

8 Functional Block Diagram

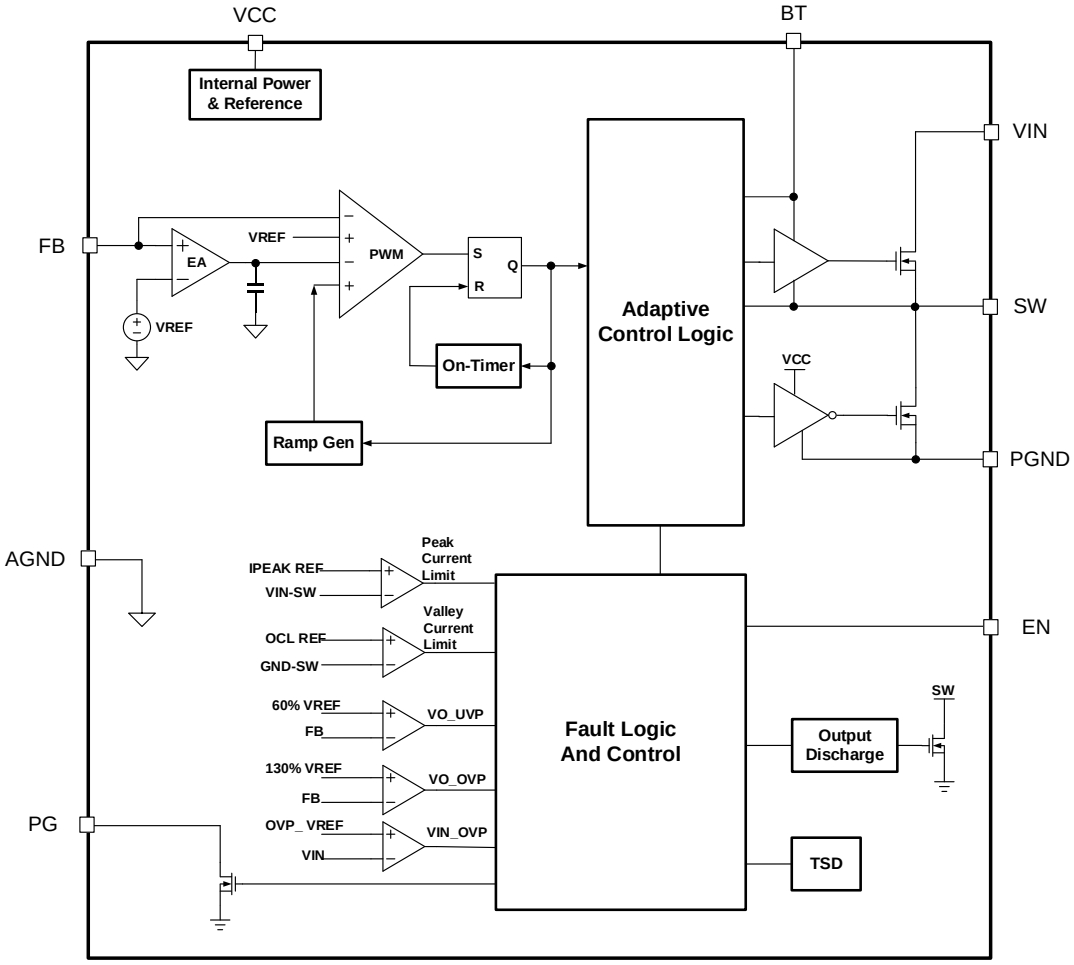


Figure 2 Functional Block Diagram

9 Feature Description

9.1 Overview

The SC81360F is a synchronous 24V buck converter with integrated power MOSFETs capable of supporting 6.5A continuous output current.

The SC81360F adopts a constant-on-time (COT) mode with a pseudo-fixed switching frequency. It can provide a fast transient response. The device integrated an internal ramp compensation circuit that supports low ESR output capacitors, such as ceramic capacitors. It simplifies the design procedure and reduces the cost of external components. The device operates in forced CCM Mode, delivering low output ripple and fast transient response under light load.

The SC81360F supports complete protection, including input under-voltage protection, input over-voltage protection, output over-voltage protection, cycle-by-cycle valley current limitation, short circuit protection with hiccup mode, and thermal shutdown protection.

9.2 FCCM Operation

The buck converter operates in the forced continuous conduction mode (FCCM). At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback (FB) voltage is below the reference voltage V_{REF}. The on period is set proportional to the converter input voltage and inversely proportional to the output voltage. When the HS - FET is turned off after the on period, the low - side MOSFET (LS - FET) is turned on. The on period is reset, and the HS-FET turns on again when the FB voltage falls below the V_{REF}. This process maintains a pseudo - fixed frequency over the input voltage range. A dead-time control scheme is internally integrated to avoid shoot-through between the LS-FET and HS-FET.

9.3 Enable and Disable

The SC81360F has an enable control pin EN. The device is enabled when VIN rises above UVLO threshold and the EN pin voltage exceeds enable threshold of 1.2V. If the device is enabled, the converter starts switching and regulates the output voltage to the target.

EN is clamped internally by a 3.7V series Zener diode and pull-down by an 1MΩ resistor.

9.4 Soft Start

The SC81360F has the soft-start (SS) function, which makes the output smooth when powering up. Ensure the input voltage is ready before togging the EN pin from low to high. When the EN becomes high, the output voltage increases slowly with the SS function. Once the output reaches the target value, the SS process is finished.

If the output of the power rails is pre-biased by a specific voltage during start-up, the device will not activate switching until the internal SS voltage becomes higher than the pre-bias voltage. This scheme ensures a smooth soft-start process.

9.5 Power Good Indication

The SC81360F provides an open drain output (PG Pin) to indicate the output voltage status. Pull the PG pin to an appropriate DC voltage (not exceeding 6V) through a resistor. It's recommended to use a pull-up resistor range from 10kΩ to 100kΩ.

During the power-up, the PG output is pulled low. When the FB voltage is within the power good range, and the soft start is finished, the internal PG switch is turned off, and the external voltage pulls up the PG pin voltage; when the FB voltage is out of this good range, the PG switch is turned on, and the PG pin voltage will be pulled down to low. The power good indication can be referred to in Figure 3.

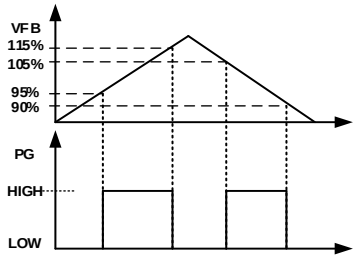


Figure.3 Power Good Indication

When EN is off, UVLO, thermal shutdown, and VIN OVP, the PG pin can also pull down.

9.6 Protection Functions

9.6.1 Under Voltage Lock Out

The SC81360F features an input under-voltage lockout (UVLO) function to stop the operation of the converter when the input voltage drops below the UVLO falling threshold. The IC resumes regular operation when the rising voltage at the VIN pin is above the UVLO rising threshold.

The SC81360F also has VCC UVLO. The SC81360F starts up only when both VCC and VIN exceed their UVLO rising threshold. It shuts down when VCC or VIN is below the UVLO falling threshold. These UVLO protections are non-latching.

9.6.2 Input Over Voltage Protection

The part will be shut down with non-latched if the VIN exceeds the OVP threshold. This device restarts working when the VIN drops below the falling threshold.

9.6.3 Over Current Protection

The SC81360F has inductor overcurrent limit (OCL) protection through cycle-by-cycle valley current detection. The drain to the source voltage of LS-FET senses the switching current.

When the HS-FET turns on, the switching current increases at a linear slew rate. When the HS-FET turns off, the current decreases linearly. If the sensed current exceeds the OCL threshold, the LS-FET will remain on even if the FB voltage is lower than the reference. The new switching cycle can be delayed until the switch current drops to the OCL threshold. Thus, the maximum load current is shown below:

$$I_{max} = I_{OCL} + \frac{\Delta I_L}{2}$$

When the OCL is triggered, the inductor current is limited, and the output voltage will drop due to higher load conditions. The part will enter hiccup protection mode when the output voltage drops below the UVP threshold.

9.6.4 Output Under Voltage Protection

The SC81360F has output under-voltage protection. When the FB voltage drops below 60% of VREF, the UVP comparator goes high, and the converter will enter hiccup mode after 32μs delay time.

In hiccup mode, the SC81360F periodically stops switching, and then IC tries to restart with a soft start. If the short condition still exists during the hiccup on time, the device will stop switching again. This protection mode is beneficial when the output is dead-shorted to the ground. The average short-circuit current is significantly reduced to alleviate the thermal issue and to protect the converter. Once the short-circuit condition is removed, The SC81360F exits hiccup mode and returns to regular operation.

9.6.5 Output Over Voltage Protection

The SC81360F has an over-voltage protection. When the VFB exceeds 130% of V_{REF}, the OVP comparator goes high, the HS-FET driver is turned off, and the output will be discharged.

9.6.6 Output Voltage Discharge

The SC81360F discharges the output when the controller is turned VIN off, EN off, or other protections, such as OVP, UVP, UVLO, and thermal shutdown. The discharge current on the output is about 50mA.

9.6.7 Over Temperature Protection

Once the IC detects the chip junction temperature exceeds the threshold of 150°C, the IC goes into thermal shutdown and stops switching. When the junction temperature falls below the typical 125°C, the IC resumes operation with a power-up sequence.

10 Application Information

10.1 Output Voltage

The output voltage can be configured for customized values using external feedback resistors.

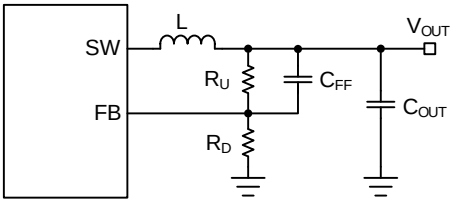


Figure 4 Output Voltage Setup with Divide Resistor

$$V_{OUT} = V_{REF} \times (\frac{R_U+R_D}{R_D})$$

Use 1% tolerance or higher accuracy resistors and keep the feedback resistors close to the FB pin on the PCB layout. Considering interference and losses, the upper-dividing resistor (RU) on FB is recommended to be no more than 60K. A feed-forward capacitor is necessary and is recommended to be 10~33pF.

10.2 Inductor Selection

The inductor selection is a tradeoff between size, cost, efficiency, and transient response performance. The critical parameters of an inductor are inductance, DC resistance, and saturation current.

Generally, choose the inductor current ripple ΔI_L to be approximately 30% to 50% of the maximum load current. The switching frequency, input voltage, output voltage, and output ripple determine the inductor value:

$$\mathrm{L} = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The inductor saturation current should be higher than the inductor peak current.

10.3 Input Capacitor Selection

The input current of the Buck converter is discontinuous, and the input capacitor should be carefully selected. The SC81360F requires input decoupling capacitors and sufficient bulk capacitors. Reserve at least a 10uF MLCC to reduce the voltage spikes.The input voltage ripple caused by the capacitance can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Placing a solid-state capacitor at the input can effectively suppress surges (hot-plugging) and reduce the input ripple.

10.4 Output Capacitor Selection

Since ceramic capacitors have low ESR and good high-frequency filtering, they are recommended for the best ripple performance across temperature and input voltage variations. The output voltage ripple is estimated as the following equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Based on the voltage coefficient of ceramic, it loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate, effective capacitance. Larger capacitors cause lower output voltage ripple and higher load transient performance.

When using a solid-state capacitor as the output capacitor, it is advisable to reserve a placement for the RFF resistor in series with the CFF capacitor. Combining it with the CFF capacitor is beneficial for loop stability debugging and optimization.

10.5 EN Pin Configuration

For an application that is enabled by VIN, connecting the EN pin through a pull-up resistor to VIN limits the current at the EN pin to less than 200μA, which prevents damage to the internal zener diode. A resistor of 200KΩ ~ 1MΩ is recommended for 20V input applications.

The device can also use a divider resistor between VIN and GND to program the input automatic start-up voltage:

$$V_{IN\_START} = 1.2 \times (\frac{R_{UP}+R_{DOWN}//1M}{R_{DOWN}//1M})$$

10.6 Parameters Selection

Table 1 lists the recommended parameter values for common output voltages.

Table 1: Parameters Selection for Common Output Voltages

VO(V)	RU(KΩ)	RD(KΩ)	CFF(pF)	L(μH)
5	40.2	5.49	33	3.3
3.3	40.2	8.87	33	3.3
2.5	40.2	12.7	33	2.2
1.8	40.2	20	33	2.2
1.5	40.2	26.7	33	1.5
1.2	40.2	40.2	33	1.5
1	40.2	60.4	33	1.5
0.6	0	10	NC	0.68

11 Layout Guide

For a COT buck coverter, the layout is an important step. If the layout is not carefully designed, the converter may suffer instability and noise issues. A reasonable PCB design is the key to the safe, efficient and stable operation of the IC. The following are some PCB design rules for your reference:

1) The input MLCCs should be placed as close as possible to the VIN and PGND pins of the IC to minimize the BUCK hot loop. A large-area copper pour should be created to connect the PGND pins of the IC and those of the input MLCCs. Additionally, some metallized vias should be placed to connect the top copper area to the internal and bottom GND layers. This approach can minimize the GND impedance and maximize the thermal performance.

2) Ensure the lowest impedance between the AGND pin and the PGND pin. Place multiple vias (≥3) near the AGND pins and connect them to the PGND through internal GND layers.

3) The VCC capacitor should be placed as close as possible to the VCC/AGND pins of the IC.

4) The dividing resistors of the output feedback should be close to the AGND and FB pin.

5) The BT capacitor should be placed as close as possible to the BT/SW pins of the IC, ensuring that the traces are as short as possible.

6) Ensure that the SW trace is as thick and short as possible when placing the inductor. Keep the SW node as far away as possible from the output feedback resistors (FB dividing resistors).

7) To achieve better thermal performance and lower ground impedance, a PCB with four or more layers is recommended. It is advisable to set the first middle layer(Middle layer1) as a GND copper pour.

The following figures provide a typical reference for PCB design.

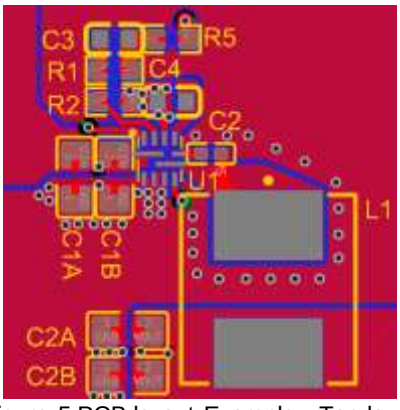


Figure 5 PCB layout Example - Top layer

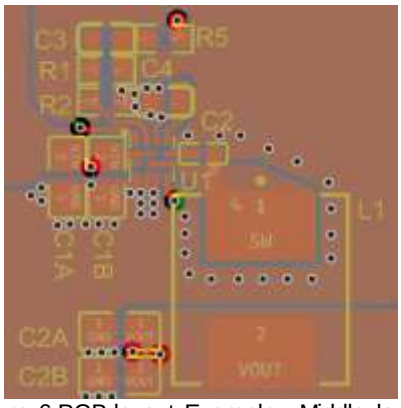


Figure 6 PCB layout Example - Middle layer1

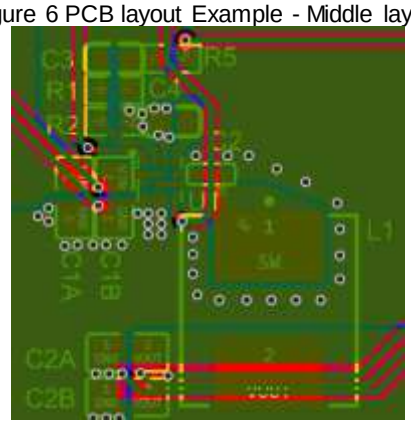


Figure 7 PCB layout Example - Middle layer2

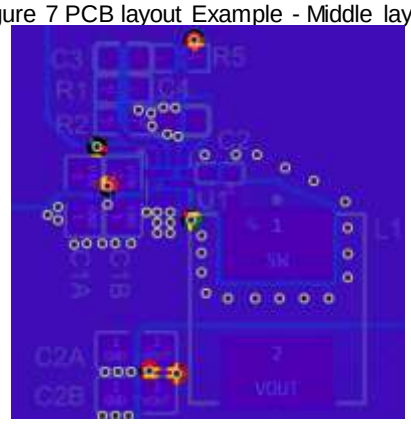
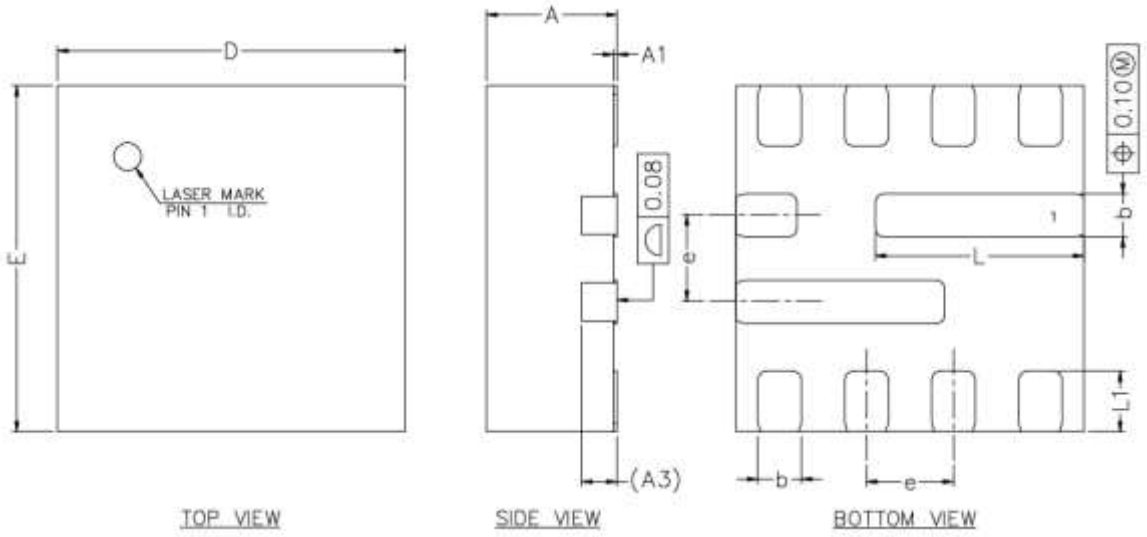
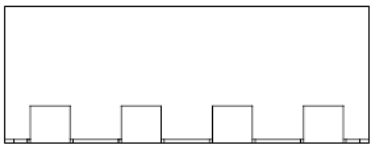


Figure 8 PCB layout Example - Bottom layer

MECHANICAL DATA

QFN-11 2mm x 2mm





SIDE VIEW

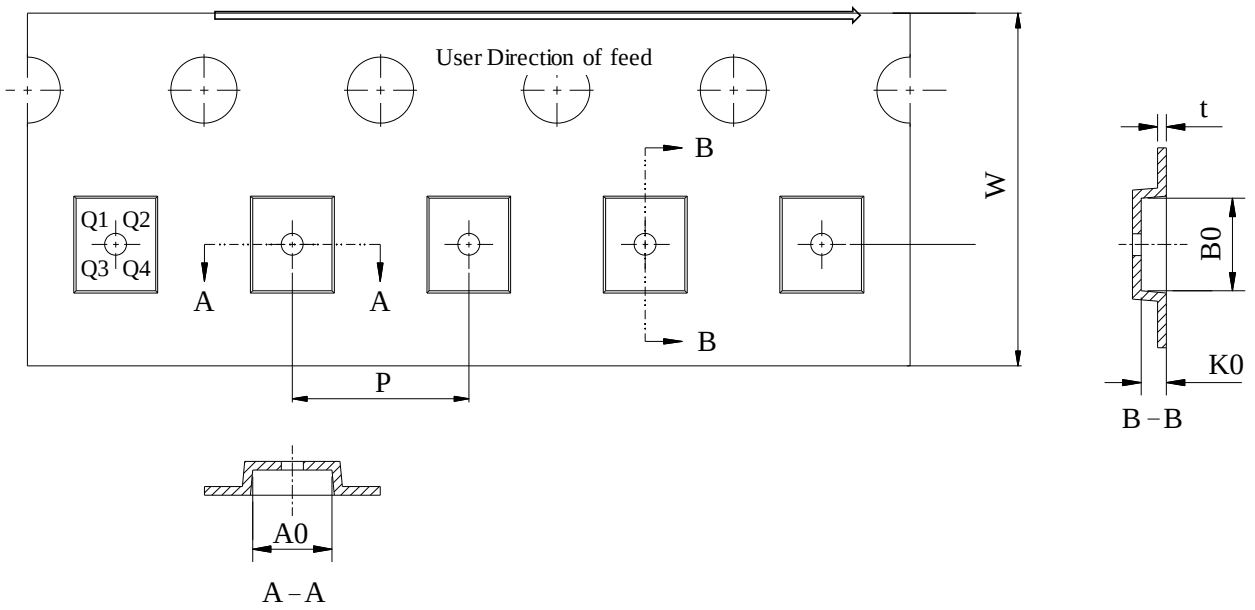
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	1.90	2.00	2.10
e	0.40	0.50	0.60
L	1.15	1.20	1.25
L1	0.30	0.35	0.40

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

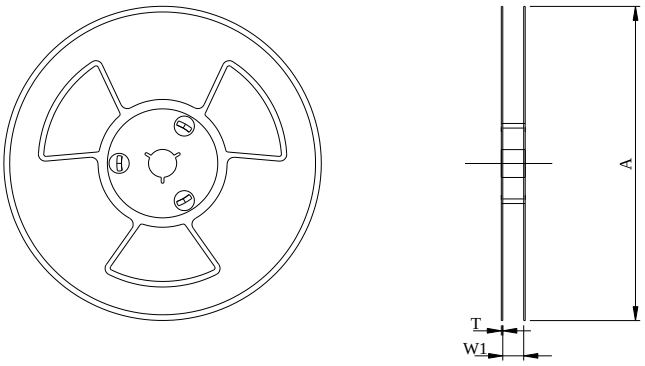
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12	8	2.2	2.2	0.95	0.25	Q1

REEL



Item	A	W1	T	Quantity
Size	330mm	12.4mm	2.4mm	5000ea/Reel

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