High Efficiency 17V 3A Synchronous Buck Converter in SOT563 Package

1 Descriptions

The SC81230H and SC81230G are high-efficiency synchronous buck converters requiring minimal external components, making them easy to implement in compact applications. They integrate power MOSFETs and can support up to 3A of continuous output current with wide input voltages from 3V to 17V and a typical switching frequency of 1.2MHz. The devices can operate in a large duty cycle to offer a low input-to-output voltage differential when the VIN is equal to VOUT.

Additionally, the converters adopt a constant on-time control mode with internal compensation, which features excellent load transient performance and supports low equivalent series resistance output capacitors such as ceramic (MLCC) capacitors.

The SC81230H adopts PSM (Power Save Mode) operation and features low quiescent current, maximizing efficiency during light-load operation. The SC81230G adopts FCCM (Forced Continuous Conduction Mode) operation with fixed switching frequency and delivers lower voltage ripple at light load.

SC81230X offers multiple protection features. These include input under - voltage protection, cycle - by - cycle peak current limitation, and thermal shutdown protection with auto - recovery.

SC81230X is available in FCSOT563 Package.

2 Features

- COT with Excellent Load Transient Performance
- High Efficiency with Integrated 58/28mΩ MOSFETs
- 3~17V Wide Input Voltage Range
- 0.6~11V Output Voltage Range
- 0.6V ±1.5% (25°C) Reference Voltage
- Up to 3A Continuous Output Current
- SC81230H: PSM, 120μA Low Quiescent Current
- SC81230G: FCCM
- 1.2MHz Switching Frequency
- Low Dropout Mode
- 1.6ms Fixed Soft Start
- Cycle-by-Cycle Valley Current Limit
- Short Circuit Protection with Hiccup Mode
- ULVO, TSD Protection
- SOT563 Package

3 Applications

- Router, WLAN/Wi-Fi
- Set-Top Boxes
- Flat-Panel Televisions and Monitors
- Portable Devices

4 Device Information

ORDER NUMBER	MODE	PACKAGE	BODY SIZE
SC81230HSBER	PSM	FCSOT563	1.6mm x 1.2mm
SC81230GSBER	FCCM	FCSOT563	1.6mm x 1.2mm

5 Typical Application Circuit

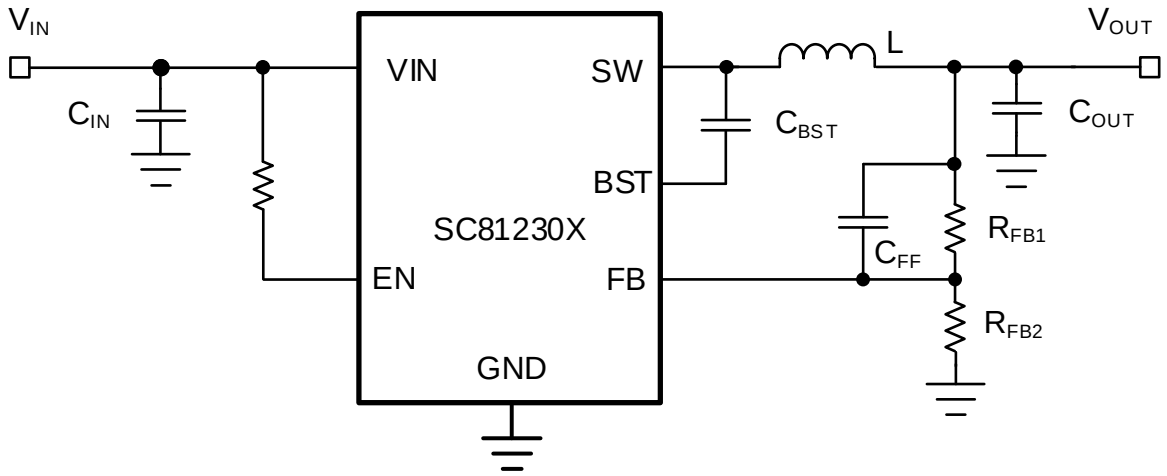
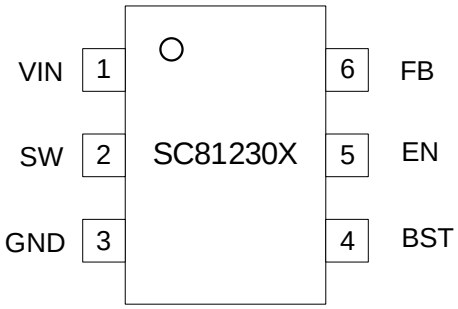


Figure. 1 Typical application circuit

6 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VIN	PWR	The power input node of the converter. Connect a decoupling capacitor between VIN and GND close to the IC.
2	SW	PWR	Switching Node. Connect to the switch node of the power inductor.
3	GND	PWR	Power ground.
4	BST	PWR	Connect a 100nF X7R ceramic capacitor between the BST pin and SW pin to provide the boosted bias voltage for the high-side gate driver.
5	EN	I	Enable the logic input pin. A logic high level enables the device, while a logic low level disables it. The EN pin is internally pulled low.
6	FB	I	The feedback node for the VOUT output voltage. The VOUT output voltage is set by the external resistor divider connected to this pin. A feed-forward capacitor (C_{FF}) is necessary to ensure sufficient loop stability and achieve a fast load transient response.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN	-0.3	18	V
	SW	-1	18	V
	SW for less than 10ns	-5.5	20	V
	BT - SW	-0.3	6	V
	FB, EN	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	-2	+2	kV
	Charged device model (CDM) ESD stress voltage(3)	-750	+750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

(4)

7.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	VIN voltage range	3		17	V
V_{OUT}	VOUT voltage range	0.6		11	V
I_{OUT}	Output Current			3	A
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL RESISTANCE(1)		FCSOT563	UNIT
Θ_{JA}	Junction to ambient thermal resistance	136	°C/W
Θ_{JC}	Junction to case resistance	58	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.5 Electrical Characteristics

V_{IN} = 12V, T_J= 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		3		17	V
I_{VIN}	Quiescent current	V_{EN} = 3.3V, V_{FB} = 0.62V		120	150	μA
I_{VIN_SD}	VIN Shutdown current	V_{EN} = 0V		1	4.5	μA
POWER SWITCH						
R_{DSON_HS}	High side MOS on resistance			58		mΩ
R_{DSON_LS}	Low side MOS on resistance			28		mΩ
CURRENT LIMIT						
I_{LMT_LS}	Low-side valley current limit		3	4	5	A
I_{ZCD}	Zero-crossing current, SC81230H only	VOUT = 3.3V, L = 2.2μH		10		mA
I_{NCL}	Negative current limit. SC81230G only	VOUT = 3.3V, L = 2.2μH		-2.4		A
SWITCHING FREQUENCY AND MINIMUM OFF TIMER						
F_{SW}	Switching frequency	VIN = 12V, VOUT = 3.3V	1000	1200	1350	kHz
T_{MIN_ON}	Minimum on time			45		ns
T_{MIN_OFF}	Minimum off time			140		ns
T_{MAX_ON}	Maximum on time			2.1		μs
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
V_{UVP}	VOUT UVP threshold		57	60	63	V_{FB}%
t_{UVPDLY}	VOUT UVP deglitch time			32		μs
V_{IN_OVP}	Input OVP to disable FCCM mode SC81230G only	Rising threshold		15.5		V
		Hysteresis		1		V
T_{HICC_OFF}	Hiccup off time			5		ms
FEEDBACK VOLTAGE AND SOFT START						
V_{FB}	Feedback regulation voltage of SC81230H	T_J=25°C	591	600	609	mV
		T_J=-40~+125°C	588	600	612	mV
V_{FB}	Feedback regulation voltage of SC81230G	T_J=25°C	588	600	612	mV
		T_J=-40~+125°C	585	600	615	mV
T_{SS}	Soft start time		1	1.6	2.2	ms
ENABLE (EN) AND UNDER VOLTAGE LOCKOUT (UVLO)						
V_{EN_R}	Enable rising threshold		1.15	1.2	1.25	V
V_{EN_HYS}	Enable hysteresis			100		mV
I_{EN}	EN pin input current	V_{EN} = 2V		1.7		μA
V_{ENC}	EN pin clamping voltage	I_{EN} = 100μA	4.2	4.8	5.4	V
$V_{IN\_UVLO\_R}$	VIN UVLO rising threshold		2.75	2.9	3	V
$V_{IN\_UVLO\_HYS}$	VIN UVLO threshold hysteresis			210		mV
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		°C

8 Functional Block Diagram

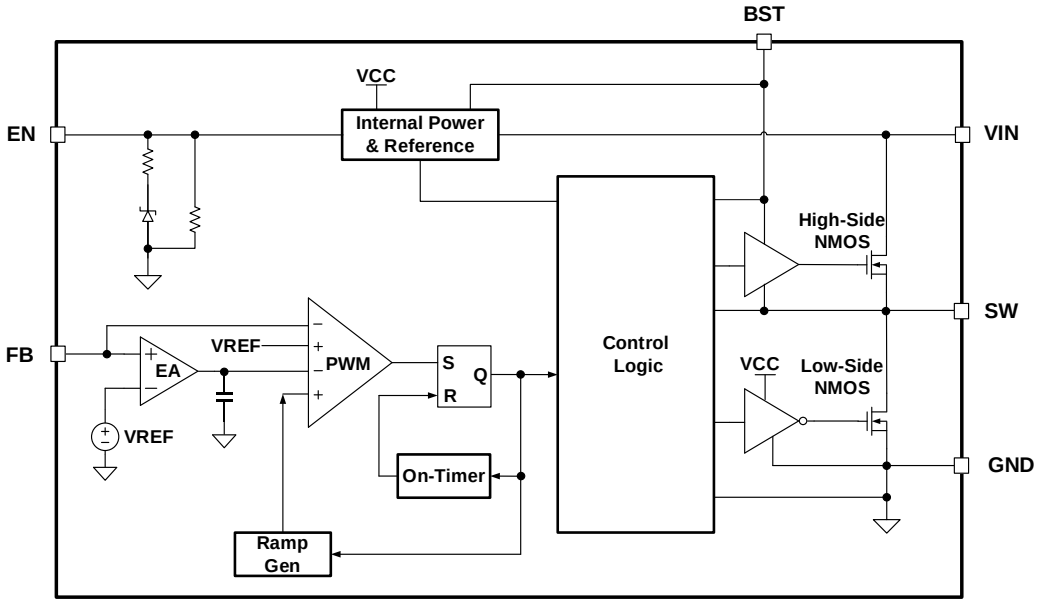


Figure 2 Functional Block Diagram

9 Feature Description

9.1 Overview

The SC81230X is a synchronous 17V buck converter with integrated power MOSFETs and is capable of supporting a 3A continuous output current.

The SC81230X adopts the constant - on - time (COT) mode with a pseudo - fixed switching frequency. It can provide a fast load transient response. An internal compensation circuit is applied to reduce the number of external components and simplify the design procedure. It can use very low ESR output capacitors, such as ceramic capacitors.

The SC81230X provides full protection features, including input under-voltage protection, input over-voltage protection, output over-voltage protection, cycle-by-cycle valley current limitation, short-circuit protection with hiccup mode, and thermal shutdown protection.

9.2 PSM Operation

The SC81230H adopts power save mode (PSM) control. As the load current decreases, the converter enters discontinuous conduction mode (DCM) after the inductor current crosses zero. In this operation, when the FB voltage is below the VREF, the HS-FET is turned on for a fixed period. Then, with the LS-FET turned on, the inductor current decreases. The LS-FET driver enters the Hi-Z state when the inductor current reaches zero. It takes a longer time to discharge the output capacitor with a light load current. The HS-FET will turn on again when the FB voltage drop to V_{REF}. With this mechanism, the SC81230H reduces the switching frequency and improves the efficiency at light load. The device can also revert to CCM operation once the output current exceeds the critical level. The critical current can be calculated by the below equation:

$$I_{OUT(CRIT)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

The SC81230H operates in the continuous conduction mode (CCM) when the valley inductor current is greater than zero amps. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback (FB) voltage is below the reference voltage V_{REF}. The on period is set proportional to the converter input voltage and inversely proportional to the output voltage. When the HS - FET is turned off after the on period, the low - side MOSFET (LS - FET) is turned on. The on period is reset, and the HS-FET turns on again when the FB voltage falls below the V_{REF}. This process maintains a pseudo - fixed frequency over the input voltage range. A dead-time control scheme is internally integrated to avoid shoot-through between the LS-FET and HS-FET.

9.3 FCCM Operation

The SC81230G adopts forced continuous conduction mode (FCCM) control. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback (FB) voltage is below the reference voltage V_{REF}. The on period is set proportional to the converter input voltage and inversely proportional to the output voltage. When the HS - FET is turned off after the on period, the low - side MOSFET (LS - FET) is turned on. The on period is reset, and the HS-FET turns on again when the FB voltage falls below the V_{REF}. This process maintains a pseudo - fixed frequency over the input voltage range. A dead-time control scheme is internally integrated to avoid shoot-through between the LS-FET and HS-FET.

9.4 Low Dropout Operation

At the beginning of each cycle, the HS-FET is turned on by the on-timer which is set according to the input and output voltage. When the on timer expires, if the FB voltage is still below the reference voltage V_{REF}, the on-timer will be extended, and the HS-FET will remain on until the maximum on time is reached. Then the HS-FET turns off, and the LS-FET turns on. The maximum on-time of HSFET is limited to 2.1μs and the minimum off-time is limited to 140ns, therefore the maximum duty cycle during low dropout can approach 94%.

9.5 Enable and Disable

The SC81230X has an enable control pin EN. The device is enabled when VIN rises above UVLO threshold and the EN pin voltage exceeds enable threshold of 1.2V. If the device is enabled, the converter starts switching and regulates the output voltage to the target.

The EN pin is clamped internally by a 4.8V series Zener diode and pull-down by an 1MΩ resistor.

9.6 Soft Start

The SC81230X features the soft-start (SS) function, which makes the output smooth during start-up. Ensure the input voltage is ready before toggling the EN pin from low to high. When the EN becomes high, the output voltage increases slowly with the SS function. Once the output reaches the target value, the SS process is finished.

If the output is pre-biased to a specific voltage during start-up, the device will not initiate switching until the internal SS

voltage exceeds the pre-bias voltage. This scheme ensures a smooth soft-start process.

9.7 Protection Functions

9.7.1 Under Voltage Lock Out

The SC81230X features an input under-voltage lockout (UVLO) function to stop the operation of the converter when the input voltage drops below the UVLO falling threshold. The IC resumes normal operation when the voltage at the VIN pin is above the UVLO rising threshold.

9.7.2 Over Current Protection

The SC81230X has inductor overcurrent limit (OCL) protection through cycle-by-cycle valley current detection. The switching current is sensed by the drain to the source voltage of LS-FET.

The inductor current increases at a linear slew rate during the HS-FET turns on. During the HS-FET turns off, the current decreases linearly. If the sensed current exceeds the OCL threshold, the LS-FET will remain on even if the FB voltage is lower than the reference. The new switching cycle can be delayed until the switch current drops to the OCL threshold. Thus, the maximum load current is shown below:

$$I_{max} = I_{OCL} + \frac{\Delta I_L}{2}$$

When the OCL is triggered, the inductor current is limited, and the output voltage will drop due to higher load conditions. When the output voltage drops below the UVP threshold, the part will enter hiccup protection mode.

9.7.3 Negative Current Limit Protection

The SC81230G operates in FCCM mode and has a negative current limit (NCL) protection to limit the negative inductor current under light load. The protection detects the valley of the inductor current when the low-side FET on. If the inductor current exceeds the NCL threshold, the low-side FET will be turned off and the high-side FET will be turned on, leading to the output voltage being higher than the target. Do not use an excessively small inductance to avoid triggering NOC; the minimum inductance is specified as:

$$L > \frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN\_MAX}})}{2 \times FSW \times NCL}$$

9.7.4 Input Over Voltage Protection

The SC81230G features input over-voltage protection (VIN_OVP) when the voltage at the VIN pin exceeds a typical value of 15.5V. When VIN_OVP is triggered, the device exits forced-PWM mode and enters PSM mode instead.

In PSM, when the FB voltage is below VREF, the HS-FET is turned on for a fixed period. Then, with the LS-FET turned on, the inductor current decreases. The LS-FET driver enters the Hi-Z state when the inductor current reaches zero. It takes a longer time to discharge the output capacitor with a light load current. The HS-FET will turn on again when the FB voltage drop to V_{REF}.

This protection is specifically designed for a pre-biased output condition. When the output is continuously higher than the target, the converter operates in reverse boost mode to discharge the output voltage to the input, which may cause overvoltage stress and potentially damage the device.

9.7.5 Output Under Voltage Protection

The SC81230X has output under-voltage protection. When the FB voltage drops below 60% of V_{REF}, the UVP comparator goes high, and the converter will enter hiccup mode after 32μs delay period.

In hiccup mode, the SC81230X periodically stops switching for a typical 5ms, then it tries to restart with a soft start. If the short-condition still exists during the hiccup in a timely manner, the device will stop switching again. This protection mode is especially useful when the output is shorted to the ground. The average inductor current is greatly reduced to alleviate the thermal issue and protect the converter. Once the short-circuit condition is removed, the SC81230X exits hiccup mode and returns to normal operation.

9.7.6 Over Temperature Protection

Once the IC detects that the chip junction temperature exceeds the threshold of 160°C, the IC goes into thermal shutdown and stops switching. When the junction temperature drops below 140°C, it resumes operation with a power up sequence.

10 Application Information

10.1 Output Voltage

The output voltage can be configured for customized values using external feedback resistors.

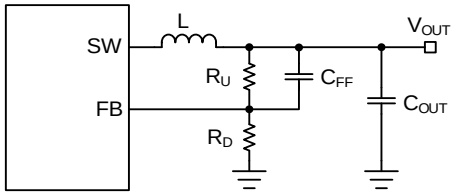


Figure 3 Output Voltage Setup with Divide Resistor

$$V_{OUT} = 0.6V \times (\frac{R_U+R_D}{R_D})$$

Use 1% tolerance or higher accuracy resistors and keep the feedback resistors close to the FB pin on the PCB layout. A larger R_U reduces standby loss but may be susceptible to noise. When considering both standby loss and noise immunity, it is recommended to select a 10kΩ or less resistor for R_D. A feed-forward capacitor (C_{FF}) is necessary to ensure sufficient loop stability and achieve a fast load transient response, and it is recommended to be in the range of 10–47pF.

Refer to Table 1 for the recommended selection of R_U, R_D and C_{FF}.

10.2 Inductor Selection

The inductor selection is a tradeoff between size, cost, efficiency, and transient response performance. The critical parameters of an inductor are inductance, DC resistance, and saturation current.

Generally, choose the inductor current ripple ΔI_L to be approximately 20% to 60% of the maximum load current. The switching frequency, input voltage, output voltage, and output ripple determine the inductor value:

$$L = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The inductor saturation current should be higher than the inductor peak current.

10.3 Input Capacitor Selection

The input current of the Buck converter is discontinuous, and the input capacitor should be carefully selected. The SC81230X requires input decoupling capacitors and sufficient bulk capacitors. Reserve at least a 10μF Multi - layer Ceramic Capacitor (MLCC) to reduce the voltage spikes. The input voltage ripple caused by the capacitors can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Placing a solid-state capacitor at the input can effectively suppress surges (hot-plugging) and reduce the input ripple.

10.4 Output Capacitor Selection

Since ceramic capacitors have low ESR and good high-frequency filtering, they are recommended for the best ripple performance across temperature and input voltage variations. The output voltage ripple is estimated as the following equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Based on the voltage coefficient of ceramic, it loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate, effective capacitance. Larger capacitors cause lower output voltage ripple and higher load transient performance.

10.5 EN Pin Configuration

For an application that is enabled by VIN, connecting the EN pin through a pull-up resistor to VIN limits the current at the EN pin to less than 200μA, which prevents damage to the Zener diode. A resistor of 100KΩ~1MΩ is recommended for such applications.

It can also use a divider resistor between VIN and GND to program the input automatic start - up voltage:

$$V_{IN\_START} = 1.2 \times (\frac{R_{UP}+R_{DOWN}//1M}{R_{DOWN}//1M})$$

10.6 Parameters Selection

Table 1 lists the recommended parameter values for common output voltages.

Table 1: Parameters Selection for Common Output Voltages

VO(V)	R_U(KΩ)	R_D(KΩ)	C_{FF}(pF)	L(μH)
0.6	0	10	-	0.68
1.05	7.5	10	33	0.82
1.2	10	10	33	1
1.5	15	10	33	1
1.8	20	10	33	1
3.3	135	30	33	2.2
5	220	30	22	2.2
10	470	30	10	4.7

11 Layout Guide

For a COT buck converter, the layout is an important step. If the layout is not carefully designed, the converter may suffer instability and noise issues. A reasonable PCB design is the key to the safe, efficient and stable operation of the IC. The following are some PCB design rules for your reference:

1) The input MLCCs should be placed as close as possible to the VIN and GND pins of the IC to minimize the BUCK hot loop. A small hot loop reduces voltage spikes at the VIN and SW pins, which benefits lower voltage stress and better EMI performance.

2) A large-area copper pour should be created to connect the GND pins of the IC and those of the input MLCCs. Additionally, some vias should be placed to connect the top copper area to the internal and bottom GND layers. This approach can minimize the GND impedance and maximize the thermal performance.

3) The GND of the input MLCCs and the output capacitors should be connected using a wide, short copper pour. Sufficient vias should be used to optimize the GND impedance.

4) The voltage-divider resistors for the output feedback should be placed close to the FB pin. They should be kept away from the SW trace and inductor. Additionally, the trace of the FB node should be made as short and small as possible to prevent noise coupling.

5) To minimize radiated emissions, ensure that the SW trace is as thick and short as possible when placing the inductor.

6) The BT capacitor should be placed as close as possible to the BT/SW pins of the IC, ensuring that the traces are as short as possible. The following figures provide a typical reference for PCB design.

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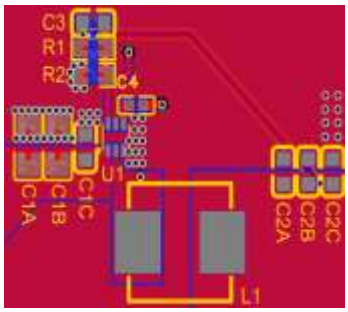


Figure 4 PCB layout Example - Top layer

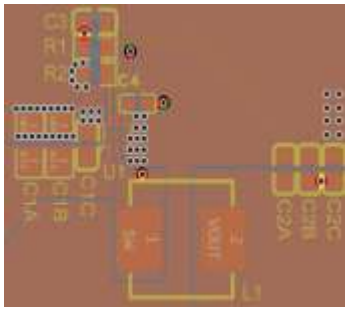


Figure 5 PCB layout Example - Middle layer1

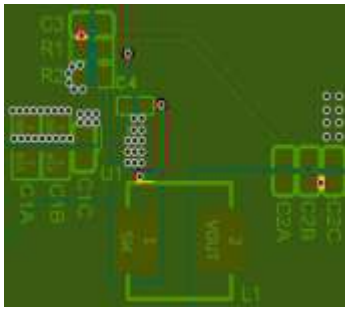


Figure 6 PCB layout Example - Middle layer2

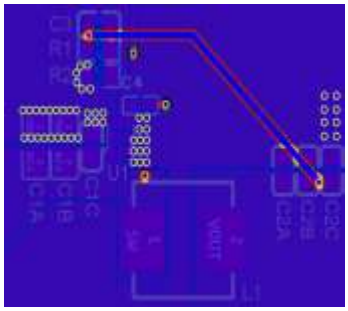
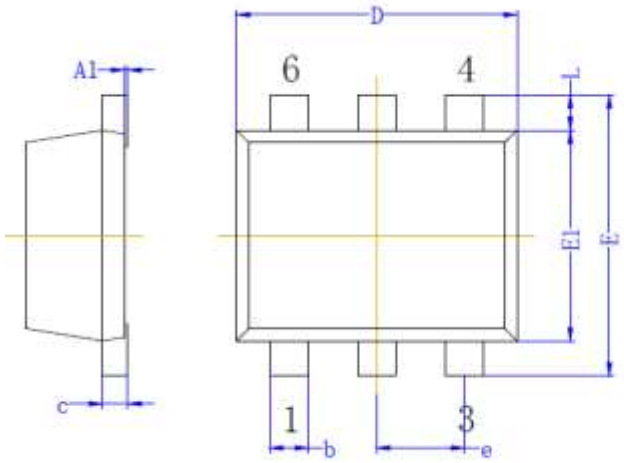


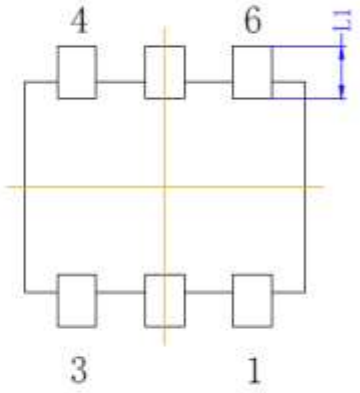
Figure 7 PCB layout Example - Bottom layer

MECHANICAL DATA

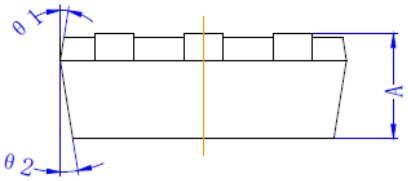
SOT563



TOP VIEW



BOTTOM VIEW

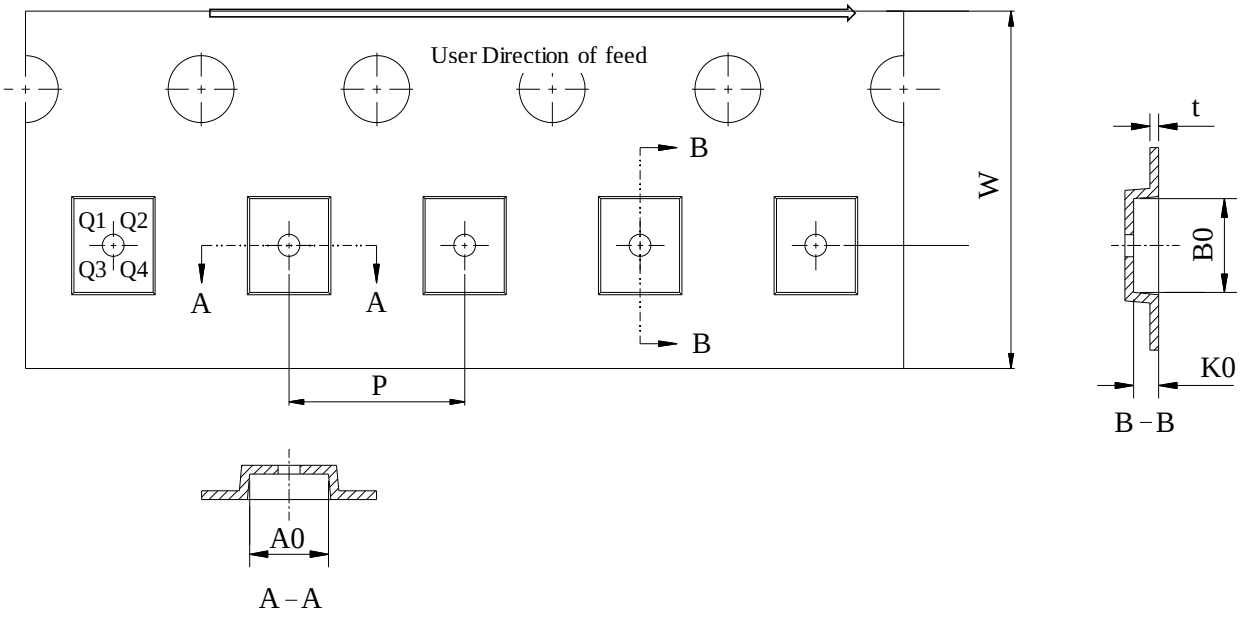


SIDE VIEW

Symbol	Minimum	Normal	Maximum
D	1.50	1.60	1.70
E1	1.10	1.20	1.30
E	1.50	---	1.70
A	0.525	---	0.60
A1	0.00	---	0.05
b	0.17	0.22	0.27
e		0.50 BSC	
L	0.10	---	0.30
L1	0.20	---	0.40
c	0.09	---	0.18
θ1		9° REF	
θ2		9° REF	

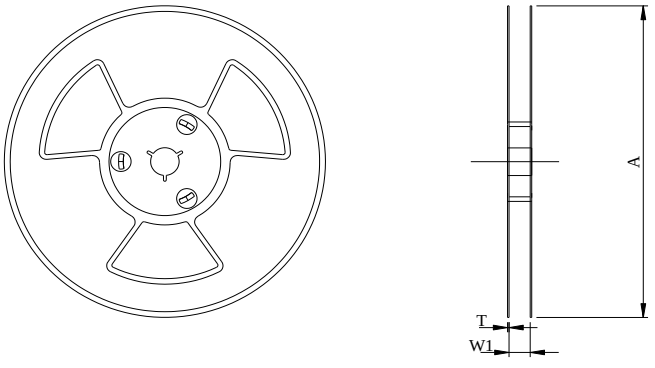
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	8.00±0.3	4.00±0.1	1.80±0.05	1.83±0.05	0.75±0.1	0.20±0.02	Q3

REEL



Item	A	W1	T
Size (mm)	180±1.0	8.6±0.3	1.4±0.3

User Direction of feed

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