High-Efficiency 5.5V 2A Synchronous Buck Converter with Low Quiescent Current in SOT563 Package

1 Descriptions

SC8105B is a high-efficiency synchronous buck converter with few external components and is easy to use in compact applications. The device operates with input voltages from 2.3V to 5.5V with a typical switching frequency of 2.2MHz and supports output voltage from 0.6V to V_{IN}. It integrates power MOSFETs and can support up to 2A load current. SC8105B can operate in the 100% duty cycle to offer a low input-to-output voltage differential when the VIN equals VOUT.

The device also features low quiescent current and PSM mode operation to maximum efficiency at light load. With PSM mode and low quiescent current during standby or light load, the device can further prolong battery life and is suitable for battery-powered applications.

The device adopts a constant on-time control mode with internal compensation, which features excellent load transient performance and supports low equivalent series resistance output capacitors such as ceramic (MLCC) capacitors.

SC8105B provides protections, including input under-voltage protection, cycle-by-cycle peak current limitation, and thermal shutdown protection with auto-recovery.

SC8105B is available in FCSOT563 Package.

2 Features

- Input Voltage Range:2.3 V to 5.5V
- 0.6V Reference with ±1% Accuracy
- 7μA Low Quiescent Current
- Power Save Mode
- 2A Continuous Output Current Capability
- Integrated 100mΩ High-side and 60mΩ low-side MOS
- Ultra-fast Transient Response
- Optimized for Low-ESR Ceramic Output Capacitors
- Real 100% Duty Cycle
- 2.2MHz Typical Switching Frequency
- Internal Soft-Start
- EN Control Pin
- Output Discharge Function
- Cycle-by-Cycle Over Current Protection
- Thermal Shutdown Protection
- Under Voltage Protection
- Thermal Shutdown Protection
- FCSOT563 Package

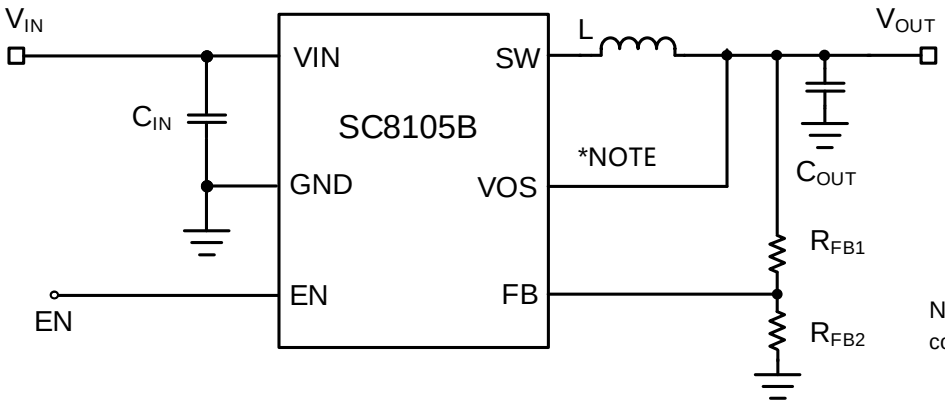
3 Applications

- Smart Phone
- STB, PC, Notebook, Server
- SSD, Memory Supply
- Battery-Powered Devices

4 Device Information

Part Number	Package	Dimension
SC8105BSBER	FCSOT563	1.60mm x 1.60mm

5 Typical Application Circuit

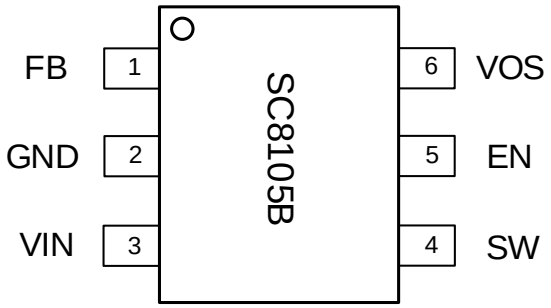


Note: VOS must be directly connected to the output node

Figure. 1 Typical application circuit

6 Terminal Configuration and Functions

Top View



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	FB	I	Feedback node of VOUT output voltage. Set the VOUT output voltage by the external resistor divider connected to this pin.
2	GND	PWR	Power and analog Ground.
3	VIN	PWR	The power input node of the converter.
4	SW	PWR	Switching Node. Connect to the switch node of the converter.
5	EN	I	Enable logic input pin. Logic high level enables the device and logic low level disables the device. Do not leave it floating.
6	VOS	I	Output voltage sense for the control loop. It must be directly connected to the output node and cannot be connected in series with any resistors.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	VIN, SW, VOS	-0.3	6	V
	SW for less than 10ns	-3	8	V
	FB, EN	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.3		5.5	V
V_{OUT}	Output voltage range	0.6			V
I_{OUT_max}	Max output Current range			2	A
F_{SW}	Switching frequency		2.2		MHz
L	Inductance of the inductor		1		μH
C_{OUT}	Effective output capacitance	4.7			μF

7.4 Thermal Information

THERMAL RESISTANCE(1)		FCSOT563(1.6X1.6mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	128	°C/W
θ_{JC}	Junction to case resistance	40	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.5 Electrical Characteristics

TA= 25°C, V_{IN} = 3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Operating voltage		2.3		5.5	V
V_{UVLO}	VIN under-voltage lockout threshold	Rising edge	2.1	2.2	2.3	V
		Hysteresis		200		mV
I_Q	No switching IQ from VIN	EN = H, not switching,		7		μA
I_{SD}	Shutdown current from VIN	EN = L			1	μA
EN LOGIC AND SOFT START						
V_{EN_H}	EN rising threshold	2.3V≤V_{IN}≤5.5V	0.825			V
V_{EN_L}	EN logic low threshold	2.3V≤V_{IN}≤5.5V			0.325	V
R_{EN}	EN pull-down Resister			1.4		MΩ
FEEDBACK AND OUTPUT						
V_{FB}	Internal reference voltage	TA=-40~85°C	0.594	0.6	0.606	V
I_{FB}	Feedback input bias current	VFB=0.6V			20	nA
R_{DIS}	Output discharge resistor	EN=Low V_{OUT}=1.8V		40		Ω
T_{SS}	Soft-start time	10% to 90% V_{OUT}		500		μs
DRIVER AND POWER SWITCH						
R_{DSON_HS}	High side MOS on resistance			100		mΩ
R_{DSON_LS}	Low side MOS on resistance			60		mΩ
f_{SW}	Switching frequency			2.2		MHz
T_{MIN_ON}	MIN on time of high side			60		ns
T_{OFF_ON}	MIN off time of high side			60		ns
PROTECTIONS						
I_{LIM-2A}	Current limit threshold	Peak current limit		3.5		A
		Valley current limit		2.6		A
T_{HICC_OFF}	Off cycle time during hiccup protection			600		μs
THERMAL SHUTDOWN						
T_{JSD}	Thermal shutdown temperature	Rising edge		150		°C
		hysteresis		20		°C

7.6 Typical Characteristics

V_{IN} = 3.6V, V_{OUT} = 1.2V, Fsw = 2.2MHz, L = 1μH, C_{OUT} = 20μF, unless otherwise noted.

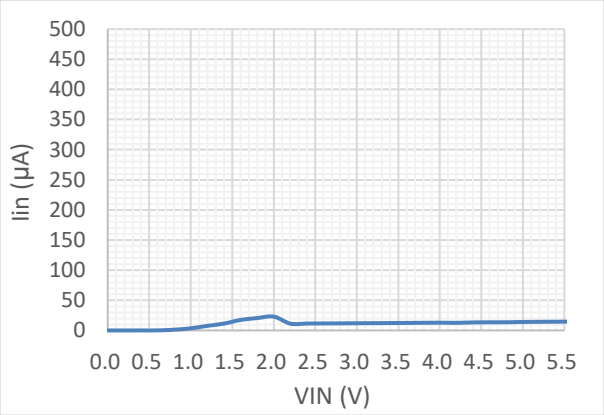


Figure.1 V_{OUT}=1.2V Standby Input Current

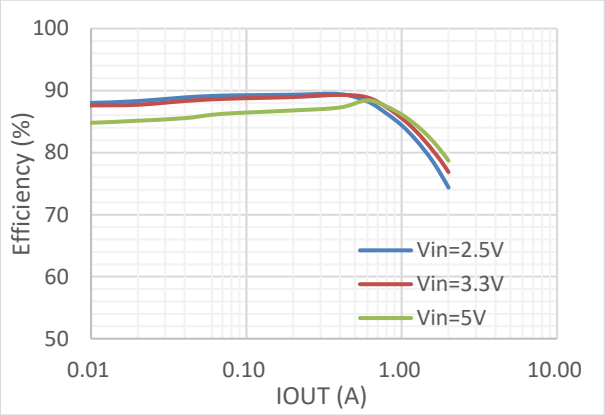


Figure.2 V_{OUT}=1.2V Efficiency Curve
Fsw=2.2MHz, L=1μH (DCR=42mΩ)

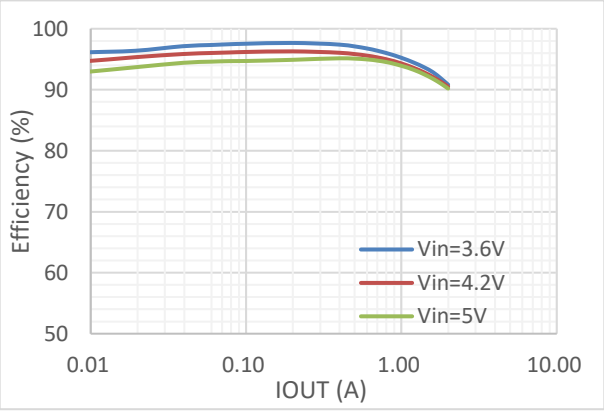


Figure.3 V_{OUT}=3.3V Efficiency Curve
Fsw=2.2MHz, L=1μH (DCR=42mΩ)

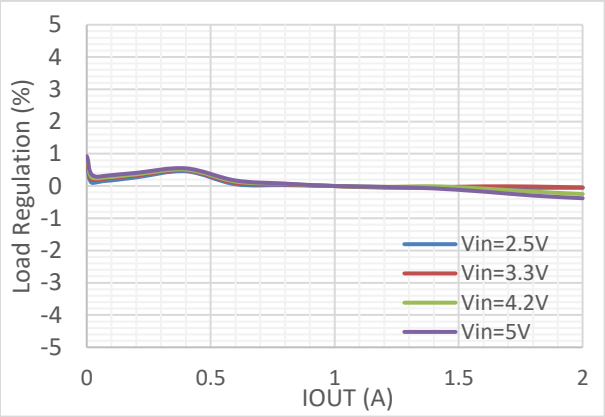


Figure.4 Load Regulation

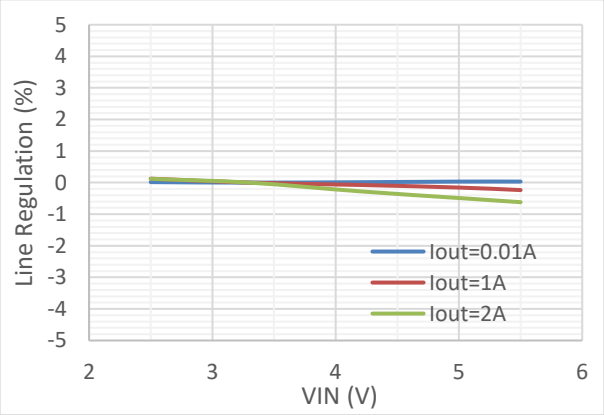


Figure.5 Line Regulation

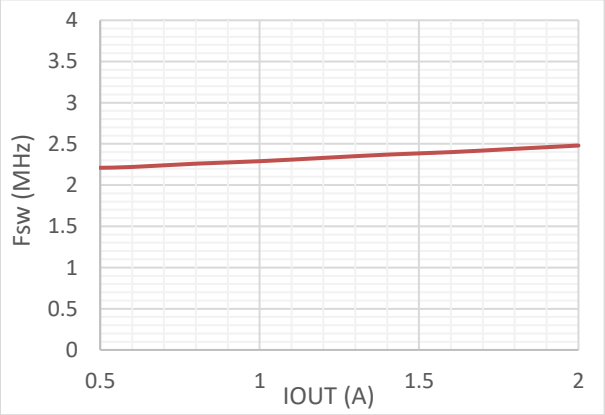


Figure.6 Frequency vs. Load Current

7.6 Typical Characteristics (Continued)

V_{IN} = 3.6V, V_{OUT} = 1.2V, Fsw = 2.2MHz, L = 1μH, C_{OUT} = 20μF, unless otherwise noted.

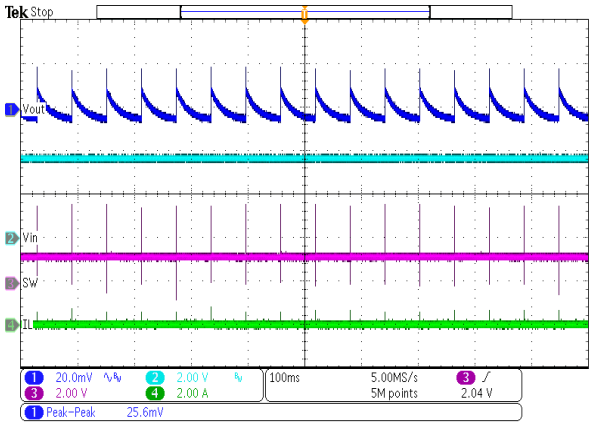


Figure.7 V_{IN}=3.6V I_{OUT}=0A Steady State

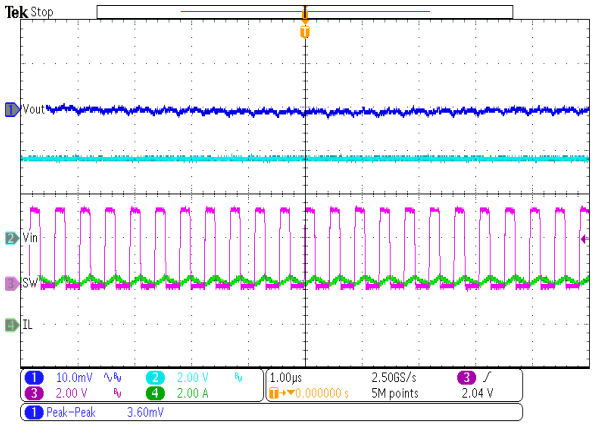


Figure.8 V_{IN}=3.6V I_{OUT}=2A Steady State

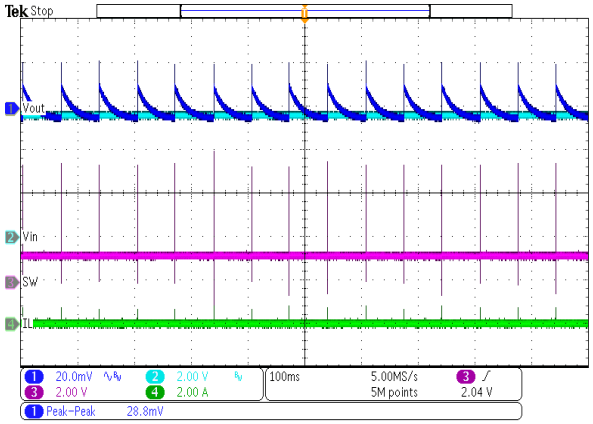


Figure.9 V_{IN}=5.5V I_{OUT}=0A Steady State

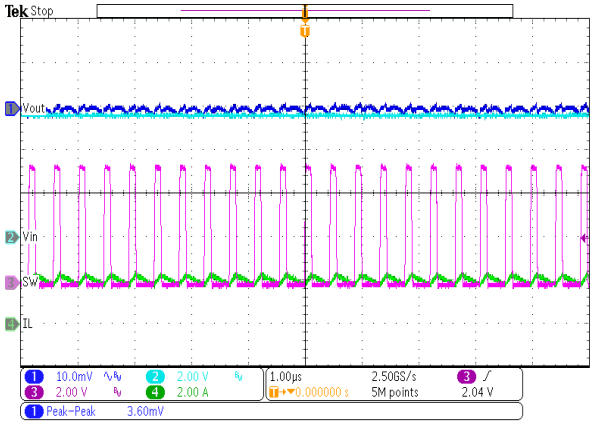


Figure.10 V_{IN}=5.5V I_{OUT}=2A Steady State

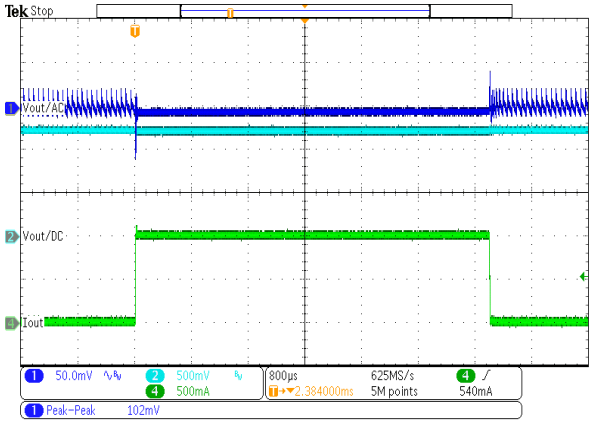


Figure.11 I_{OUT}=0 to 1A, 0.2A/μs

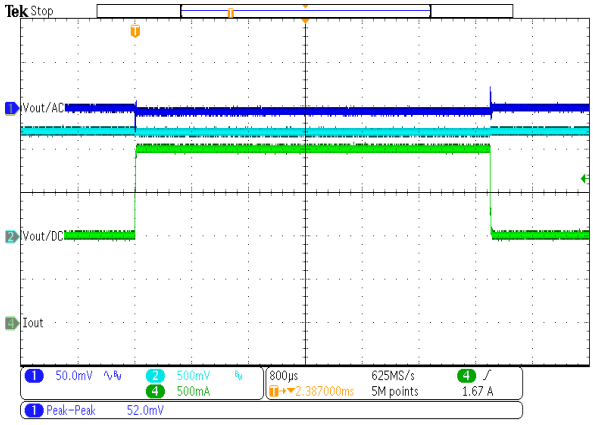


Figure.12 I_{OUT}=1A to 2A, 0.2A/μs

7.6 Typical Characteristics (Continued)

V_{IN} = 3.6V, V_{OUT} = 1.2V, Fsw = 2.2MHz, L = 1μH, C_{OUT} = 20μF, unless otherwise noted.

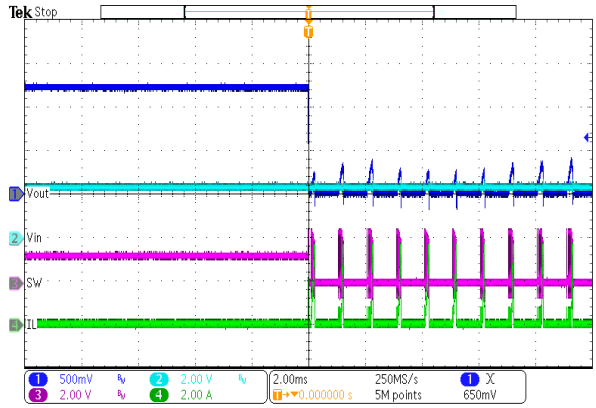


Figure.13 V_{IN}=2.3V, SCP Entry

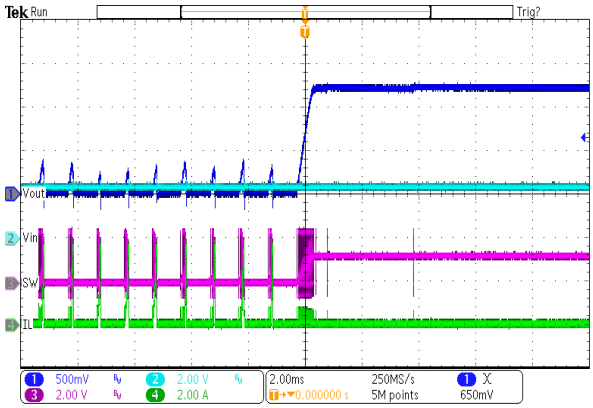


Figure.14 V_{IN}=2.3V, SCP Recovery

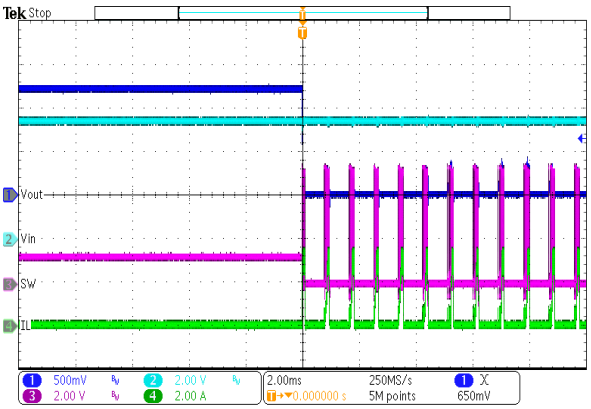


Figure.15 V_{IN}=5.5V, SCP Entry

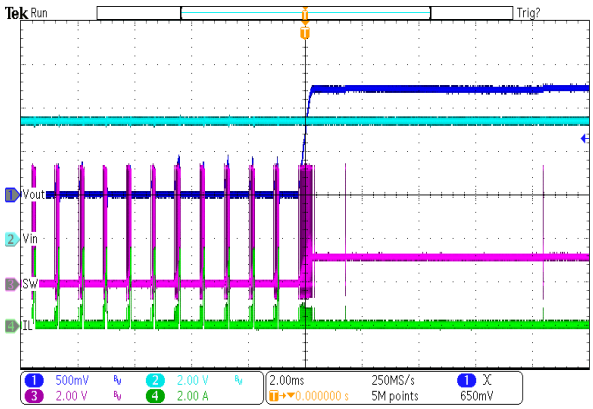


Figure.16 V_{IN}=5.5V, SCP Recovery

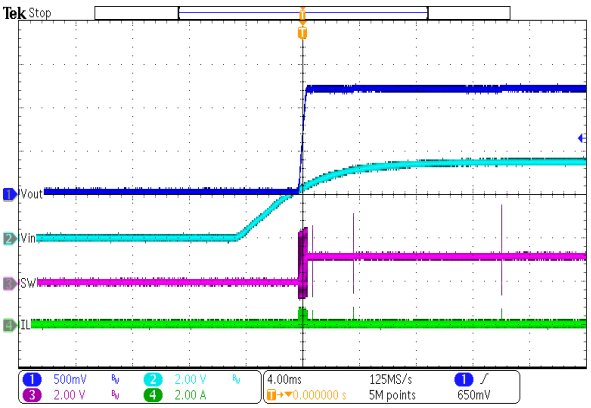


Figure.17 I_{OUT}=0A, V_{IN} Power Up

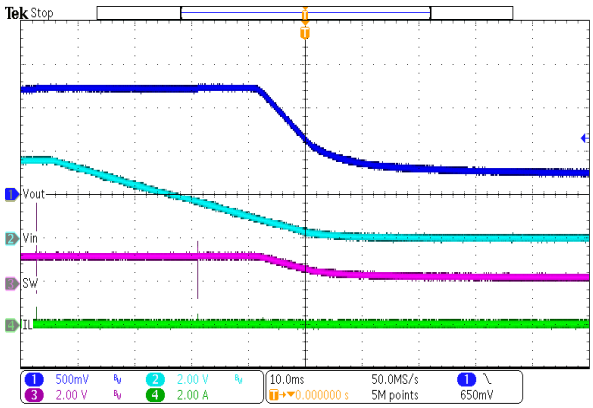


Figure.18 I_{OUT}=0A, V_{IN} Shutdown

7.6 Typical Characteristics (Continued)

V_{IN} = 3.6V, V_{OUT} =1.2V, Fsw = 2.2MHz, L = 1μH, C_{OUT} = 20μF, unless otherwise noted.

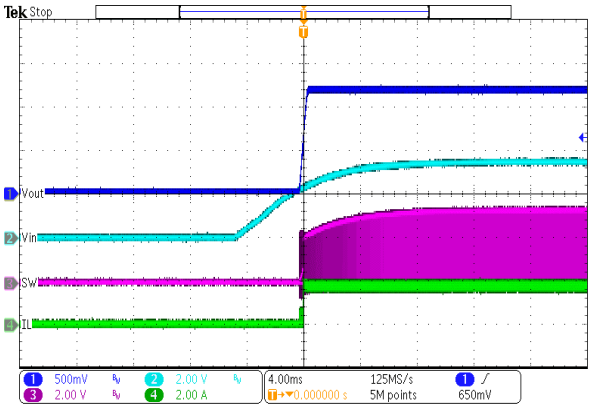


Figure.19 I_{OUT}=2A, VIN Power Up

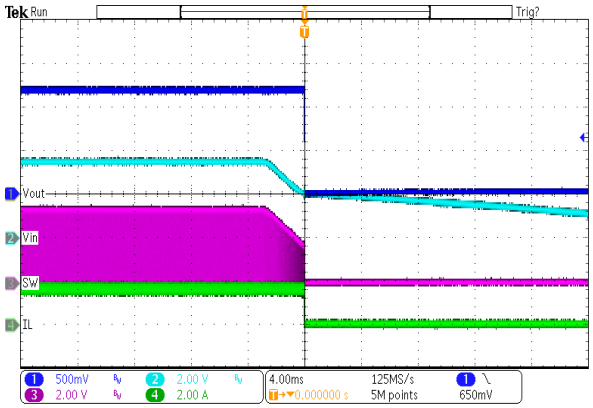


Figure.20 I_{OUT}=2A, VIN Shutdown

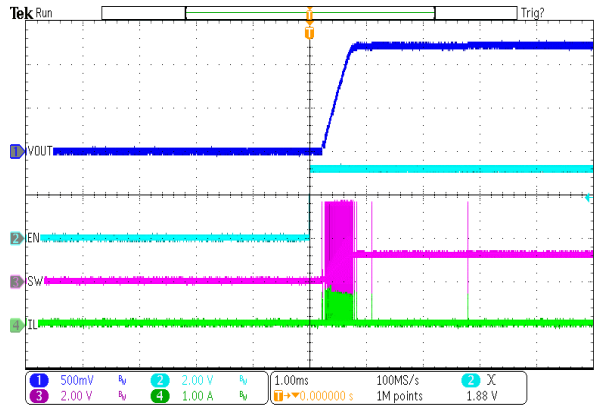


Figure.21 I_{OUT}=0A, EN On

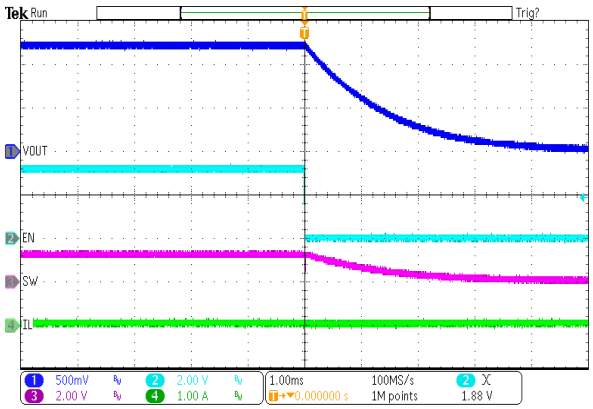


Figure.22 I_{OUT}=0A, EN Off

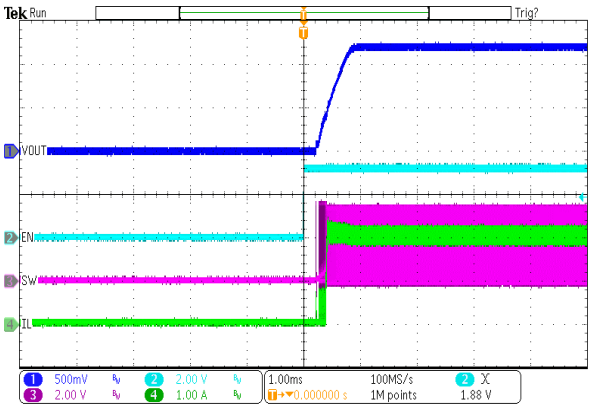


Figure.23 I_{OUT}=2A, EN On

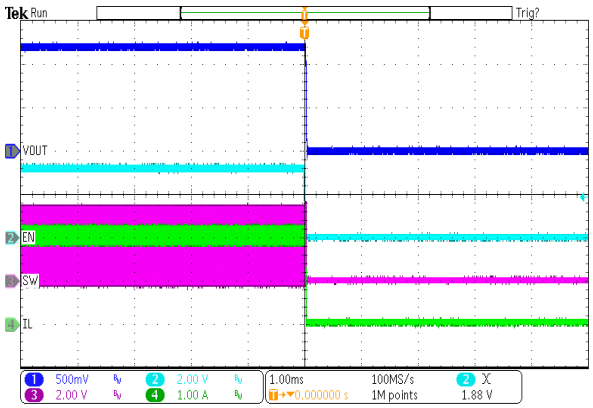
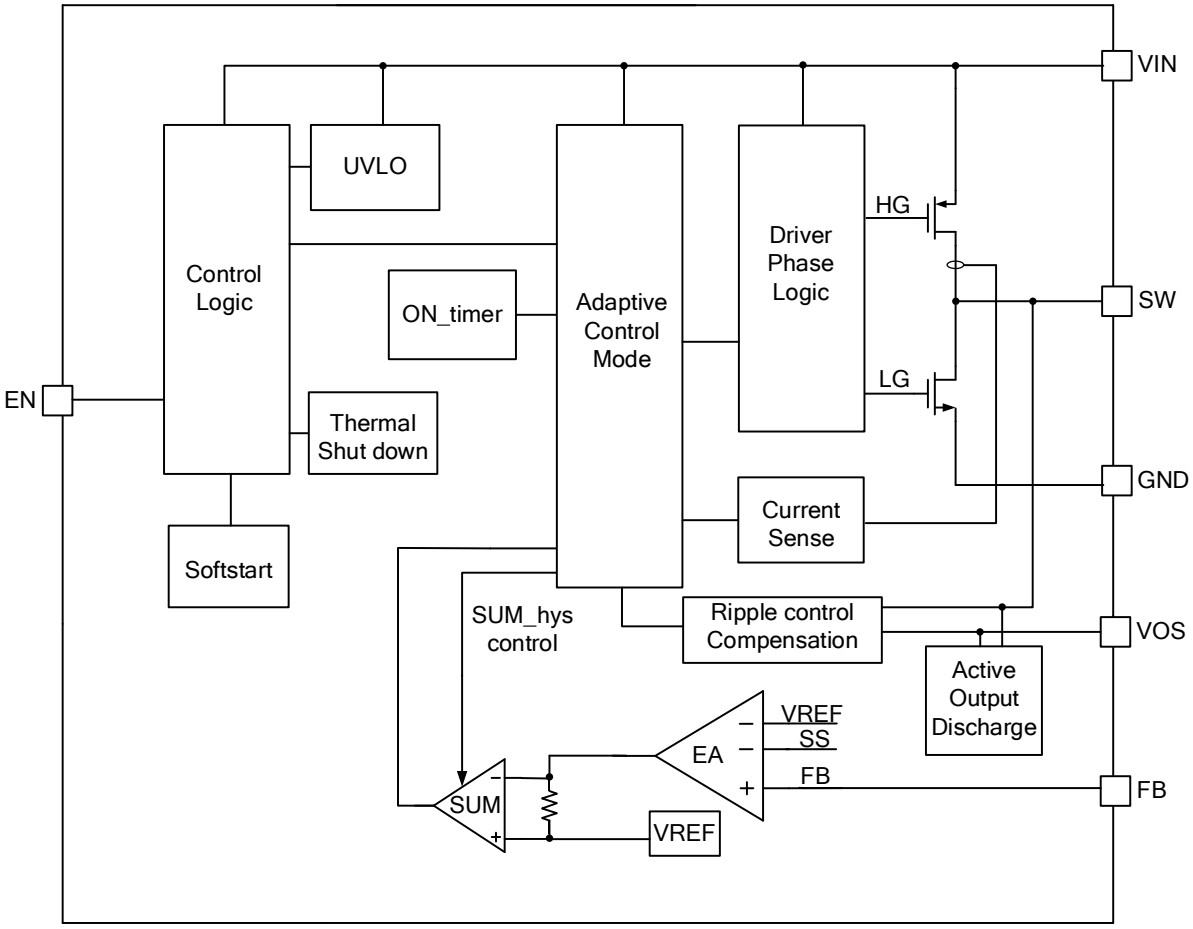


Figure.24 I_{OUT}=2A, EN Off

8 Terminal Configuration and Functions



9 Feature Description

9.1 Enable and Disable

SC8105B has an enable control pin EN. The device is enabled when VIN rises above 2.3V and the EN pin voltage exceeds the enable threshold of 0.825V. When the device is enabled, the converter starts switching and regulates the output voltage to the target. If the enable control function is not needed, tie this pin to the VIN pin directly.

9.2 Soft Start

The IC adopts a soft start feature to prevent inrush input current and output voltage overshoot during startup. The soft-start time is typically at 500μs. It also supports a safe pre-biased startup.

9.3 Output Discharge

SC8105B integrates a discharge function with a 40Ω discharge resistor to discharge the output capacitors through SW and VOS pin when the device is disabled by EN pin.

9.4 PWM/PSM Operation

SC8105B adopts a constant on-time control mode with a fixed switching frequency. The device operates in PWM mode at middle or heavy load with a typical switching frequency of 2.2MHz and automatically switches into a power-save mode (PSM) when the load decrease. In PWM mode, the output voltage ripple is minimized by a fixed and stable switching frequency; In PSM mode, the switching frequency decrease with the load current decrease, and the light load efficiency is improved by reducing switching loss. The device provides a seamless transition between PSM and PWM.

9.5 100% Duty Cycle Operation

The device supports 100% duty cycle operation to minimum voltage drop from V_{IN} to V_{OUT} when V_{IN} is equal to or lower than the programmed output voltage. In this mode, the high-side MOSFET is continuously turned on and the low-side MOSFET is turned off.

This function is designed for battery-powered applications to achieve the longest operation time by taking full advantage of the battery voltage range.

The minimum input voltage to maintain the output target depends on the load current and equivalent resistance from V_{IN} to V_{OUT}:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{MOS} + R_L)$$

Where:

I_{OUT_MAX} is the maximum output current;

R_{MOS} is the on-resistance of the high-side PMOS;

R_L is the equivalent resistance of the power inductor;

9.6 Protections

9.6.1 Input Under Voltage Lock Out

SC8105B features an input under-voltage lockout (UVLO) function to stop the operation of the converter when the input voltage drops below the typical UVLO threshold of 2V. The IC resumes normal operation when the rising voltage at the VIN pin is 200mV above the UVLO threshold.

9.6.2 Over Current and Hiccup Protection

SC8105B supports cycle-by-cycle current limits on both the high side and low side MOSFET and prevents the device from high currents such as overload, output short circuit, or inductor saturation. If the high side current limit occurs, the high side MOSFET turns off immediately and the low side MOSFET turns on to prevent the inductor current from running away. When the inductor current drops down to the low side current limit, the low side MOSFET turns off and the high side MOSFET turns on again.

To prevent this function from false triggers by switching noise, a minimum on-time of 60ns is adopted, the actual inductor current may exceed the high side current limit threshold because of this feature.

When the high side current limit is triggered 32 times, the device stops switching and automatically starts a new startup after a typical delay time of 600μs. This protection mode is especially useful when the output is dead-shorted to the ground. The average short-circuit current is greatly reduced to alleviate the thermal issue and to protect the converter. Once the short-circuit condition is removed, SC8105B exits hiccup mode and returns to normal operation.

9.6.3 Over Temperature Protection

The device integrates over-temperature protection to protect the junction temperature from overheating. Once the IC detects the chip junction temperature exceeds the threshold (150°C typical), the IC goes into thermal shutdown and stops switching. The IC resumes operation when the junction temperature falls below the typical 130°C.

10 Application Information

10.1 Output Voltage

The output voltage can be configured for customized valuesusing external feedback resistors and can be calculated as below.

$$V_{OUT} = V_{REF} \times (\frac{R_U+R_D}{R_D})$$

Where:

V_{REF} is the internal reference voltage 0.6V;

R_U and R_D are the resistors connected from VOUT to GND.

Use 1% tolerance or higher accuracy resistors and keep the feedback resistors close to the FB pin on the PCB layout.

There is no strict limitation on the feedback resistors. The current flowing through RD is at least 100 times larger than I_{FB}. The R_U is typically between 40KΩ to 500KΩ for consideration of accuracy and standby loss.

10.2 Inductor Selection

The device switches at a typical frequency of 2.2MHz. A 1μH or 2.2μH inductor with a small DCR is best for high-performance applications. The switching frequency, input voltage, output voltage, and output ripple determine the inductor value:

$$\mathrm{L} = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Choose the inductor current ΔI_L to be approximately 30% of the maximum load current. The inductor saturation current I_{SAT} should be higher than the inductor peak current I_{PEAK} with a sufficient margin.

$$I_{PEAK} = 0.5\Delta I_L + I_{OUT\_MAX}$$

10.3 Input Capacitor Selection

The input current of the Buck converter is discontinuous and the input capacitor should be carefully selected. A low ESR input capacitor close to IC's VIN pin and GND pin is the best choice, such as an X5R or X7R ceramic capacitor. A 10μF~22μF with sufficient voltage rating capacitor is required for small input voltage ripple and stability.

The input voltage ripple caused by the capacitance can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

10.4 Output Capacitor Selection

Since ceramic capacitor has low ESR and good high-frequency filtering, the X7S or X7R ceramic capacitor is recommended for the best ripple performance across temperature and input voltage variations. The output voltage ripple is estimated as the following equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Based on the voltage coefficient of ceramic, it normally loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate effective capacitance. Larger capacitors cause lower output voltage ripple and higher load transient performance.

11 Layout Guide

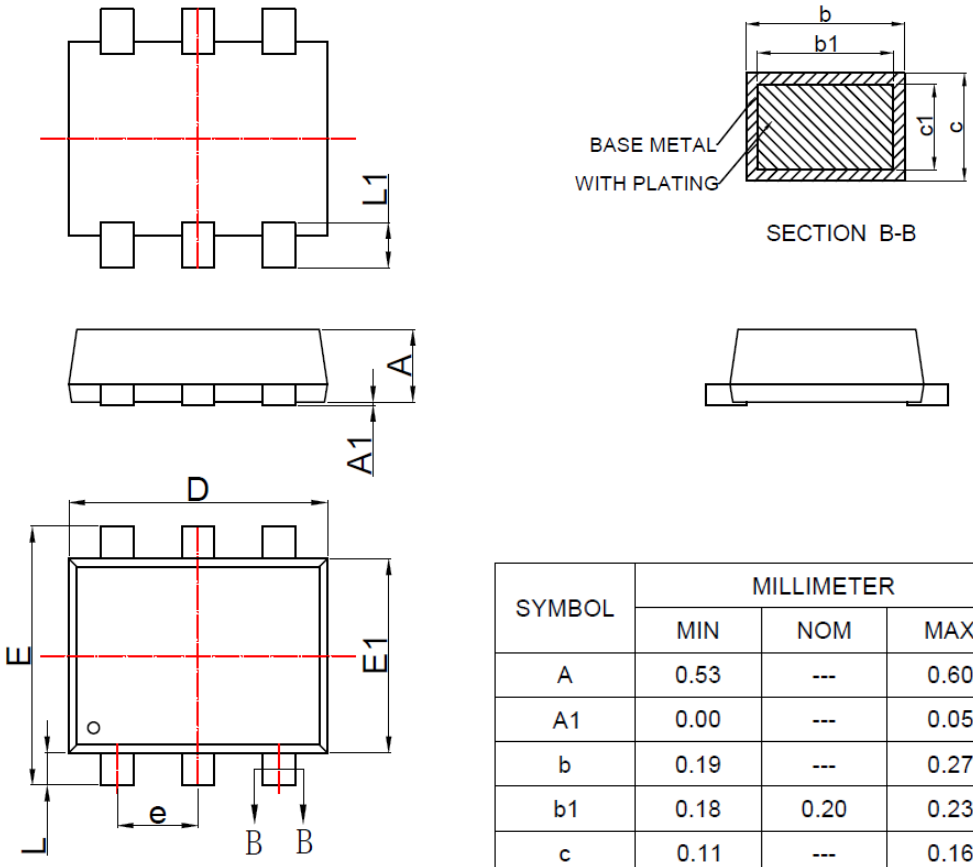
For best performance, the PCB layout should be carefully designed to avoid instability, switching noise interference, and EMI issues. Minimizing the area of alternating current and voltage loops in the layout helps reduce EMI.

Here show some guidelines for reference:

1) The input capacitor (C_{VIN}, MLCC) should be close to IC to minimize the critical path area and make sure the current flows through the C_{VIN} first, then the VIN pin. The PCB trace should be wide and short.
2) The FB feedback resistor should be close to the FB pin and be away from the switching node.
3) The VOS pin connection should be short and away from the switching node.
4) Keep the switching node SW with a short trace.
5) Use a wide and short GND trace to minimize ground independence which causes VOUT droop during heavy load.
6) Use a ground plane in one of the middle layers as a noise shielding and a heat-sinking PCB ground plane. Connect these ground traces and planes with proper vias.

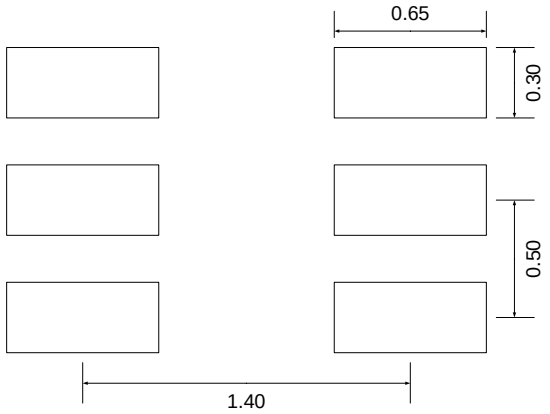
MECHANICAL DATA

FCSOT563 (1.6 x 1.6 x 0.6 mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.53	---	0.60
A1	0.00	---	0.05
b	0.19	---	0.27
b1	0.18	0.20	0.23
c	0.11	---	0.16
c1	0.10	0.11	0.12
D	1.50	1.60	1.70
E	1.503	1.60	1.70
E1	1.10	1.20	1.30
e	0.50BSC		
L	0.10	0.20	0.30
L1	0.20	0.30	0.40

RECOMMENDED FOOTPRINT

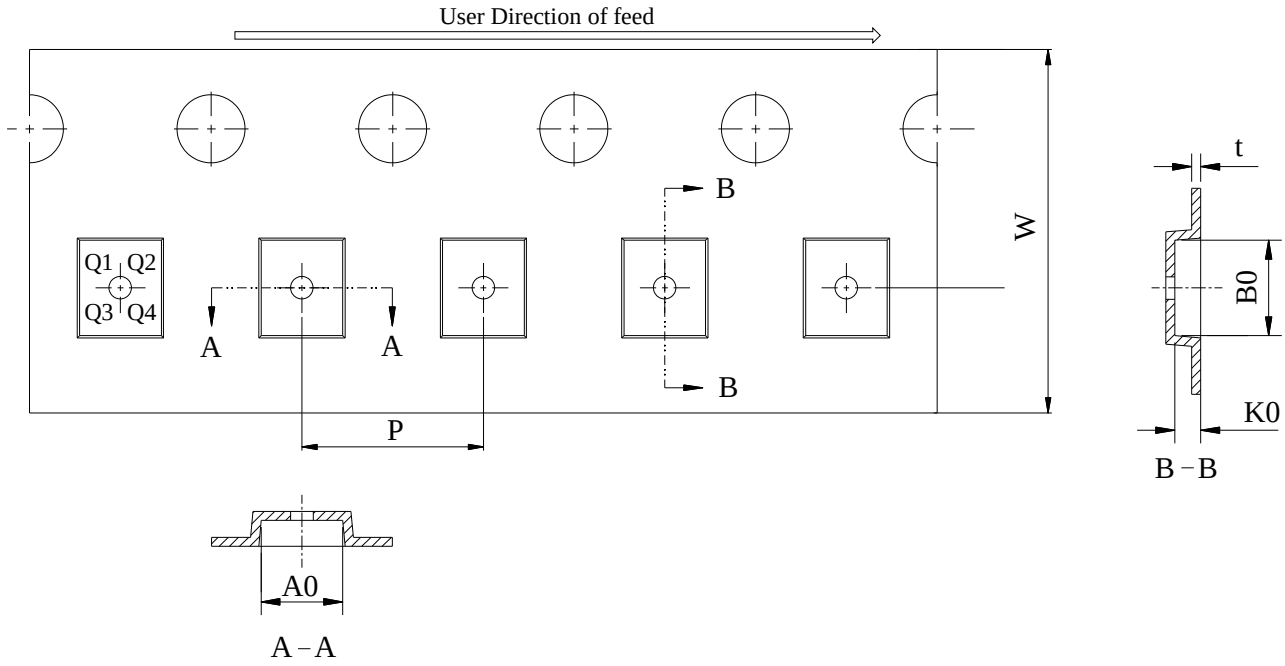


Unit: mm

Recommended PCB Layout

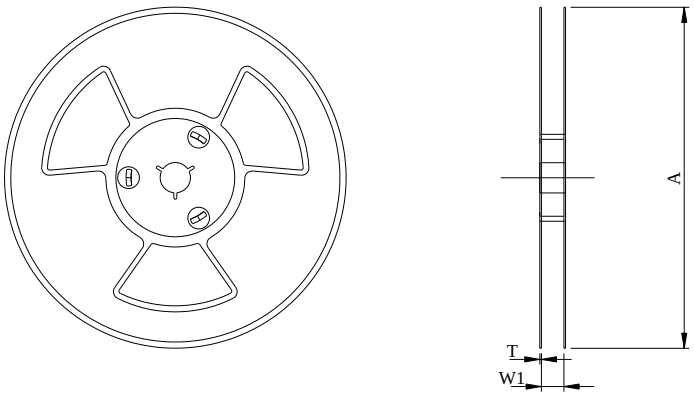
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	8.00±0.10	4±0.10	3.26±0.10	3.30±0.10	1.05±0.10	0.20±0.02	Q3

REEL



Item	A	W1	T
Size (mm)	180±1.0	8.6+1.0/-0	1.4±0.3

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