SC71702Q, Dual-Channel Automotive Antenna LDO with Current Sense

1 Descriptions

The SC71702Q is a dual-channel low-dropout regulator (LDO) family, designed to operate for a wide input voltage range from 4.5-V to 36-V (40-V load dump capability). The LDO family is suitable to supply automotive active antenna, camera modules and microphone applications through coax cables with 400-mA current capability per channel.

The SC71702Q is designed to indicate full diagnostics through current sense and error pins to MCU. Therefore, current sense is multiplexed to report a proportional analog output to the sensed load current and provide fault indications without external calibrations. In addition, one current sense can be manually selected to report another channel's information, which helps save analog-to-digital (ADC) resources. The current limit of individual channel is adjustable by a resistor on ILIMX pin.

Implementing Back-to-Back (B2B) FET structure, SC71702Q is able to protect against reverse current and reverse battery polarity failures without extra input diode. The LDO also offers thermal shutdown (TSD) and output short-to-battery (STB) protection. An internal inductive clamp diode is integrated for each channel to protect the device during shutdown with a long inductive cable on output.

The SC71702Q is available in HTSSOP-16 package.

2 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: T_A range: -40°C to 125 °C
- 4.5-V to 36-V wide input voltage range, 40-V load dump capability
- Excellent output performance
  - 1.5-V to 22-V adjustable output voltage range
  - Up to 400-mA current capability per channel
- Single and dual-channel LDO in same package
- Adjustable current limit for each channel
- High current sense accuracy to detect very light load condition: ±10% at 5-mA load and ±50% at 1-mA load
- High Power Supply Rejection Ratio (PSRR): Typical 70dB at 100-Hz
- 500-mV (max) dropout voltage at 100-mA load
- Multiplexing current sense to save ADC resource
- Power switch mode when FB is short to GND
- Full diagnostics and integrated protection for robust design
  - Input undervoltage lockout (UVLO)
  - Reverse battery polarity protection
  - Reverse current protection (RCP)
  - Output short-to-battery (STB) protection
  - Output inductive load clamp
  - Output short-circuit protection (SCP)
  - Thermal shutdown (TSD)
- HTSSOP-16 Package with thermal pad
- SC71702Q has same package with
  - SC71701Q (Single-channel)

3 Applications

- Automotive active antenna power
- Automotive camera module and sensor power
- Automotive microphone power

4 Device Information

ORDER NUMBER	CHANNEL	Fault Logic	PACKAGE	BODY SIZE
SC71702QSJER	Dual-channel	Latch-off	HTSSOP-16	5mm x 6.4mm x 1.2mm
SC71702AQSJER	Dual-channel	Auto-retry	HTSSOP-16	5mm x 6.4mm x 1.2mm
SC71702DQSJER	Dual-channel	Latch-off	HTSSOP-16	5mm x 6.4mm x 1.2mm
SC71702EQSJER	Dual-channel	Auto-retry	HTSSOP-16	5mm x 6.4mm x 1.2mm

5 Revision History

Revision	Date	Page(s) changed	Changes Description
V1.0.0	2023/8	/	Initial Version
V1.0.1	2024/1	19	Updated Auto-retry Logic Description
V1.0.2	2025/9	29	Updated Example Stencil Design
V1.0.3	2025/12	1	Updated Device Information

6 Typical Application Circuit

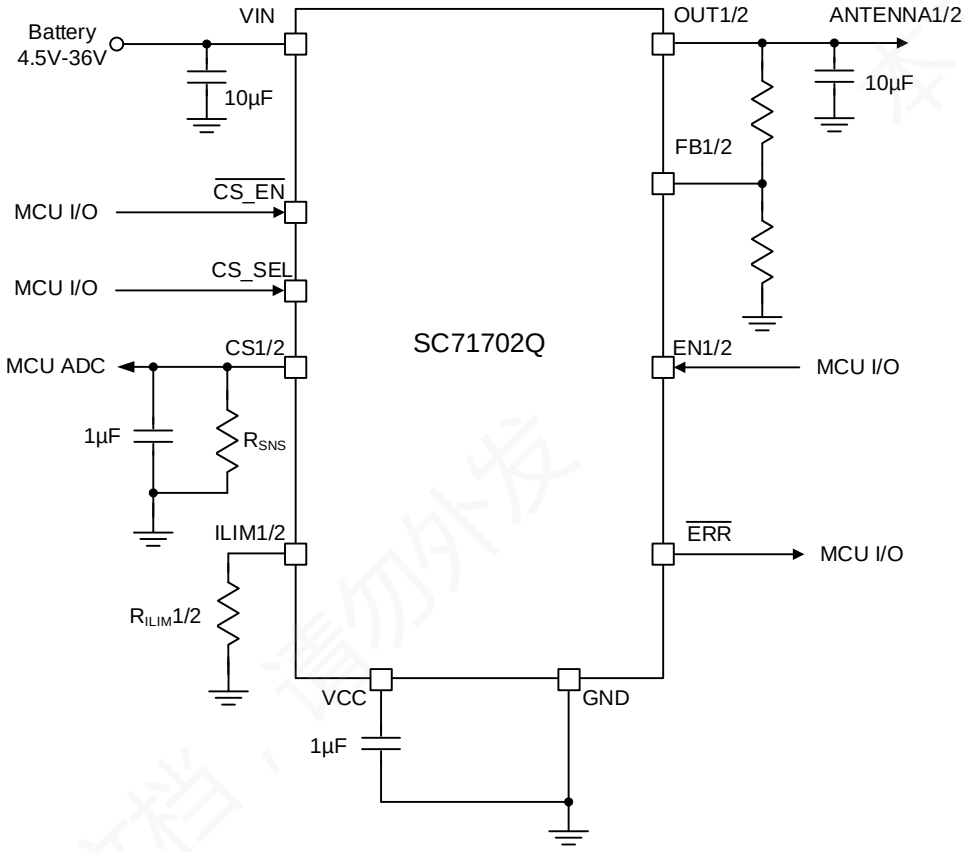
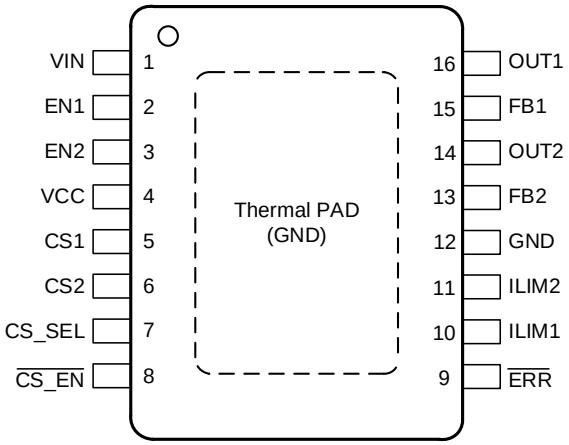


Figure 6-1 Typical Application Circuit

7 Terminal Configuration and Functions

TOP VIEW



Pin Map of SC71702Q

TERMINAL		I/O	DESCRIPTION
PIN NUMBER	PIN-NAME		
1	VIN	I	Power supply input.
2	EN1	I	Active high enable input for OUT1. LDO1 is enabled when EN1 goes high, and is disabled when EN1 goes low. This pin has internal pull-down to GND. This pin can be short to GND or floating if not used.
3	EN2	I	Active high enable input for OUT2. LDO2 is enabled when EN2 goes high, and is disabled when EN2 goes low. This pin has internal pull-down to GND. This pin can be short to GND or floating if not used.
4	VCC	O	Internal 4.5-V regulator output. Used to supply internal control circuitry. Connect a 1-µF ceramic capacitor between VCC and GND.
5	CS1	O	Output of sensed load current. When CS_SEL and $\overline{\text{CS\_EN}}$ are both set to low, CS1's output current is proportional to current through OUT1. A resistor should be connected between CS1 and GND to get appropriate CS1 output voltage level. A 1-µF ceramic capacitor from CS1 and GND is needed for compensation of current sense loop. This pin can be short to GND or floating if not used.
6	CS2	O	Output of sensed load current. When CS_SEL and $\overline{\text{CS\_EN}}$ are both set to low, CS2's output current is proportional to current through OUT2. A resistor should be connected between CS2 and GND to get appropriate CS2 output voltage level. A 1-µF ceramic capacitor from CS2 and GND is needed for compensation of current sense loop. This pin can be short to GND or floating if not used.
7	CS_SEL	I	The CS_SEL selects current sense between LDO1 and LDO2 when $\overline{\text{CS\_EN}}$ is low. Refer to **Table 1** CSX Multiplexing Logic for more details. When not used, short this pin to GND or leave it floating.
8	$\overline{\text{CS\_EN}}$	I	The $\overline{\text{CS\_EN}}$ enables and disables the current sense multiplexing feature. This pin is active low. When not used, short this pin to GND or leave it floating.
9	$\overline{\text{ERR}}$	O	This pin is an Open-drain (OD) fault indicator. Used to report faults. This pin can be connected to GND or floating if not used.
10	ILIM1	I	Connect a resistor between this pin to GND to program current limit for LDO1. Short this pin to GND will set current limit to internal current limit.

11	ILIM2	I	Connect a resistor between this pin to GND to program current limit for LDO2. Short this pin to GND will set current limit to internal current limit.
12	GND	G	Ground reference. Connect this pin directly to the thermal PAD on PCB.
13	FB2	I	Feedback input for LDO2's output voltage setting. This pin can be connected to GND for current limited power switch mode operation.
14	OUT2	O	Output of LDO2
15	FB1	I	Feedback input for LDO1's output voltage setting. This pin can be connected to GND for current limited power switch mode operation.
16	OUT1	O	Output of LDO1

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals (2)	Unregulated input, VIN to GND	-40	40	V
	EN1, EN2 to GND	-0.3	40	V
	OUT1, OUT2 to GND (3)	-0.3	40	V
	FB1, FB2 to GND	-0.3	40	V
	VCC	-0.3	6	V
	CS1, CS2 to GND	-0.3	VCC+ 0.3	V
	ILIM1, ILIM2, CS_SEL, $\overline{CS\_EN}$, $\overline{ERR}$	-0.3	7	V
T_J	Operating junction temperature range	-40	150	°C
T_A	IC operating ambient temperature range	-40	125	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) There is an internal diode connecting between the OUTX and GND pin with 400mA DC current capability for inductive clamp protection.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage (2), per AEC Q100-002	-2	2	kV
	Charged device model (CDM) ESD stress voltage (3), per AEC Q100-011	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	4.5		36	V
V_{OUT}	Output voltage. Regulated LDO mode	1.5		22	V
	Output voltage. Power switch mode	1.5		36	V
C_{OUT}	Output capacitance range for loop stability	2.2		100	μF
$C_{OUT(ESR)}$	Output capacitor's ESR range for stability	0		5	Ω
T_J	Operating junction temperature range	-40		150	°C
T_A	Operating ambient temperature range	-40		125	°C

8.4 Thermal Information

THERMAL RESISTANCE(1)		HTSSOP-16	UNIT
Θ_{JA}	Junction to ambient thermal resistance	41	°C/W
$\Theta_{JC(top)}$	Junction to case (top) thermal resistance	26	°C/W
Θ_{JB}	Junction-to-board thermal resistance	19.75	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.11	°C/W
$\Theta_{JC(bot)}$	Junction to case (bottom) thermal resistance	3	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

8.5 Electrical Characteristics

T_J = -40°C to 150°C, V_{IN} = 14V. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4.5		36	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising		4.2	4.5	V
		V_{IN} falling		3.7	4	V
I_Q	Quiescent current	V_{IN} = 4.5V to 36V, $V_{EN1} \geq 2V$ and $V_{EN2} \geq 2V$, I_{OUT1} = I_{OUT2} = 0.1mA, V_{OUT1} = V_{OUT2} = 8V, GND current		0.6	1	mA
I_{SD}	Shutdown current	EN1 = EN2 = GND, GND current		2.5	5	μA
I_{OP}	Operating current	$V_{EN1} \geq 2V$ and $V_{EN2} \geq 2V$, $I_{OUT1} \leq$ 400mA and $I_{OUT2} \leq$ 400mA, V_{OUT1} = V_{OUT2}= 8V, GND current			7	mA

VCC					
V_{CC}	Internal regulator output	V_{IN} = 5.5V to 36V, I_{CC} = 0mA		4.5	V
I_{CC_MAX}	Internal regulator current limit		15	70	mA
LOGIC INPUTS					
V_{IL}	Logic input low level	EN1, EN2, CS_SEL and $\overline{CS\_EN}$		0.7	V
V_{IH}	Logic input high level	EN1, EN2, CS_SEL and $\overline{CS\_EN}$	2		V
I_{CS_EN}	Input current into $\overline{CS\_EN}$	$\overline{CS\_EN}$ = 5V, V_{ENx} ≥ 2V		10	μA
I_{CS_SEL}	Input current into CS_SEL	CS_SEL = 5V, V_{ENx} ≥ 2V		10	μA
I_{ENX}	Leakage current into ENx pin	V_{ENx} ≤ 36V, EN1 and EN2		15	μA
R_{ENX}	Enable pull-down resistor	V_{ENx} ≤ 36V, EN1 and EN2	500		kΩ
OUTPUT PERFORMANCE					
V_{OUT}(2)	Output accuracy in LDO mode	36V ≥ V_{IN} ≥ V_{OUT}+1.5V and V_{IN} ≥ 4.5V, I_{OUT} = 1mA to 400mA	-2	2	%
R_{on}	On-resistance in power switch mode	I_{OUT} = 100mA		5	Ω
$\Delta V_{OUT(\Delta VIN)}$	Output voltage line regulation	36V ≥ V_{IN} ≥ V_{OUT}+1.5V and V_{IN} ≥ 6V, I_{OUT} = 10mA, voltage variation on FB		10	mV
$\Delta V_{OUT(\Delta IOUT)}$	Output voltage load regulation	I_{OUT} = 1mA to 400mA, voltage variation on FB		20	mV
V_{DO}	Output dropout voltage	I_{OUT} = 100mA		500	mV
I_{OUT}	Output current range	V_{OUT} in regulation	0	400	mA
PSRR(1)	Power supply rejection ratio	I_{OUT} = 100mA, C_{OUT} = 2.2μF, *f* = 10Hz	70		dB
R_{OUTX}	Pull down resistor for OUT1 and OUT2	EN1 and EN2 = GND	50		kΩ
CURRENT SENSE					
I_{OUT}/I_{CS}	OUTX to CSX current sense ratio	V_{IN} = 4.5V to 36V, I_{OUT} = 1mA to 400mA	198		
M_{CS}	Current sense ratio accuracy	100mA≤I_{OUT}≤400mA	-3	3	%
		50mA≤I_{OUT}<100mA	-5	5	%
		5mA≤I_{OUT}<50mA	-10	10	%
		I_{OUT} = 4mA	-15	15	%
		I_{OUT} = 3mA	-20	20	%
		I_{OUT} = 2mA	-25	25	%
		I_{OUT} = 1mA	-50	50	%

I_{CS_LK}	CS1, CS2 leakage current	EN2 and EN2 = GND, T_A = 25°C			2	μA
V_{CS_OCL}	Current sense voltage in over current limit fault	When device is in over current limit	2.4	2.55	2.65	V
V_{CS_TSD}	Current sense voltage in thermal shutdown fault	When device is in thermal shutdown	2.7	2.85	3	V
V_{CS_STB}	Current sense voltage in short to battery fault	When device detects short to battery fault	3.05	3.2	3.3	V
I_{CS_FT}	Current sense fault condition current	When device is in OCL, TSD or STB fault	3.3			mA
CURRENT LIMIT						
I_{OUT}/I_{LIM}	OUTX to ILIMX current ratio	V_{IN} = 4.5V to 36V, I_{LIM} = 1mA to 400mA		198		
M_{LIM}	Current limit accuracy	V_{IN} = 4.5V to 36V, 100mA≤I_{ILIM}≤400mA	-5		5	%
		V_{IN} = 4.5V to 36V, 50mA≤I_{ILIM}<100mA	-8		8	%
I_{LIM_MAX}	Maximum current limit	ILIM1 or ILIM2 = GND	400	500	550	mA
I_{LIM_LK}	ILIM, ILIM1, ILIM2 leakage current	EN1 and EN2 = GND, T_A =25°C			2	μA
V_{LIM}	Current limit threshold	Voltage on ILIM1, ILIM2 pins when device enters current limit		1.233		V
FEEDBACK						
V_{FB}	Reference voltage for FB1 and FB2	Device is in LDO mode		1.233		V
M_{FB}	Reference voltage accuracy	Device is in LDO mode	-2		2	%
I_{FB}	Leakage current into FB pin				130	nA
FAULTS						
V_{STB_TH}	Short to battery fault detection threshold	V_{OUTX} − V_{IN}, check during turn-on sequence	-500	-55	110	mV
I_{REV}	Reverse current protection threshold	Device is in LDO mode or power switch mode	-100	-40	-1	mA
I_{REV_LK}	Reverse leakage current	-40V ≤ V_{IN} ≤ 0V, reverse current to V_{IN}		0.1		mA
T_{SD}	Thermal shutdown threshold	Junction temperature rise		175		°C
T_{SD_HYS}	Thermal shutdown hysteresis			15		°C
V_{ERR_OL}	Low effective $\overline{ERR}$ voltage	I_{SINK} = 5mA, $\overline{ERR}$ is low			0.4	V
I_{ERR_LK}	$\overline{ERR}$ open-drain leakage current	$\overline{ERR}$ high impedance, 5V pull-up voltage			1	μA
TIMING						

$t_{d\_CS\_SEL\_R}$(1)	Current-sense delay from the rising edge of CS_SEL	V_{ENX} ≥ 2V, $\overline{CS\_EN}$ = GND, CS_SEL rises from 0V to 5V	10	μs
$t_{d\_CS\_SEL\_F}$(1)	Current-sense delay from the falling edge of CS_SEL	V_{ENX} ≥ 2V, $\overline{CS\_EN}$ = GND, CS_SEL falls from 5V to 0V	10	μs
$t_{d\_CS\_EN\_R}$(1)	Current-sense delays from the rising edge of $\overline{CS\_EN}$	V_{ENX} ≥ 2V, $\overline{CS\_EN}$ rises from 0V to 5V	10	μs
$t_{d\_CS\_EN\_F}$(1)	Current-sense delay from the falling edge of $\overline{CS\_EN}$	V_{ENX} ≥ 2V, $\overline{CS\_EN}$ falls from 5V to 0V	10	μs
t_{RC_BLK}	Reverse current blanking time	Blanking time for reverse current protection after power up, rising edge of enable and OCL is released.	16	ms
t_{RC_DGT}(1)	Reverse current (short to battery) shut down deglitch time	Delay to shut down the device when it detects negative current on pass elements. I_{OUT} = -200mA (typ.), T_A=25°C	5	μs
t_{STB_BLK}	STB blanking time and detection window	STB blanking time and detection window after ENX is pulled high	16	ms
t_{STB_DGT}	STB deglitch time	Time counting from STB release to STB_STAT=0	16	ms
t_{HICCUP}(1)	Hiccup off timer (for auto-retry version only)		30	ms

(1) Guarantee by Design; not production tested.

(2) Not consider external feedback resistor's accuracy

8.6 Typical Characteristics

V_{IN} = 14V, V_{OUT1}=8.5V, V_{OUT2}=5V, unless otherwise noted.

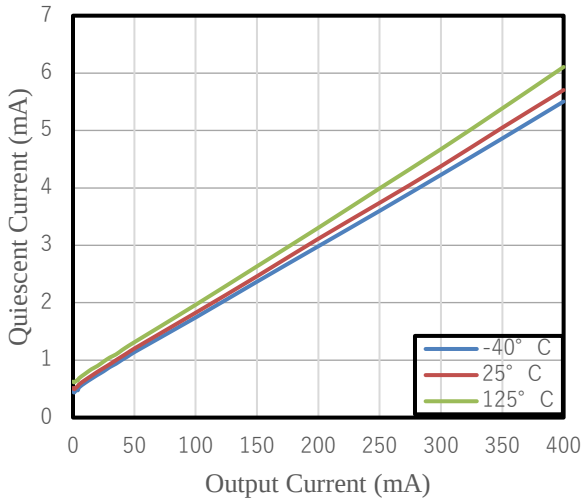


Figure 8-1 Quiescent current vs output current

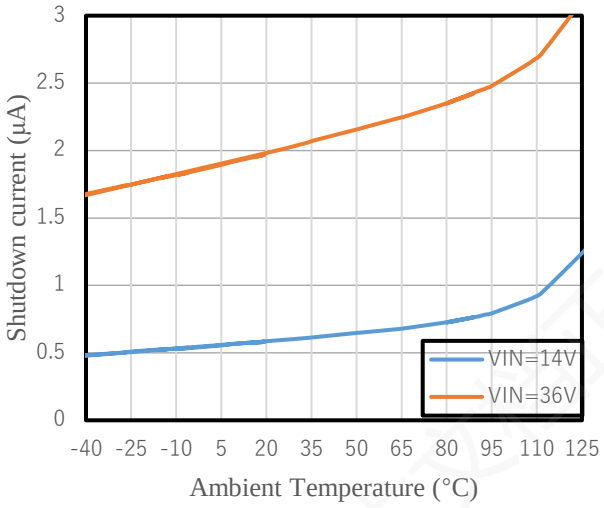
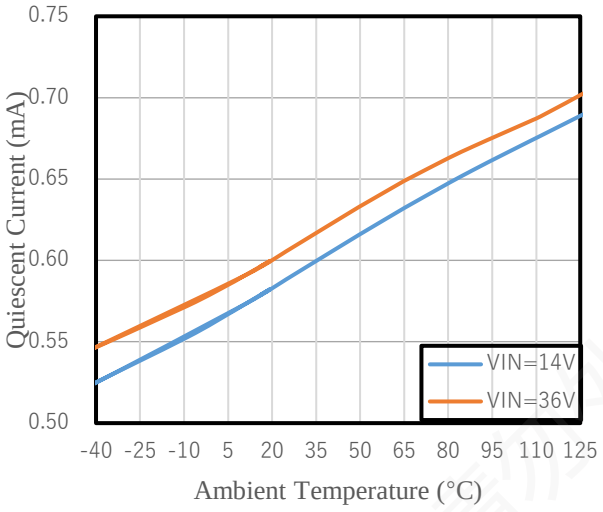
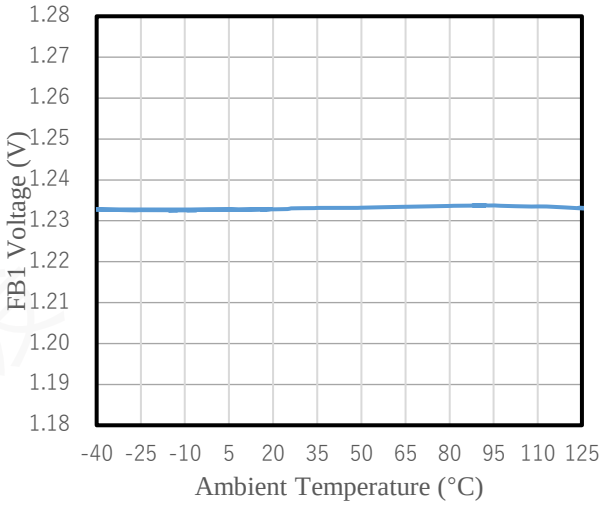


Figure 8-2 Shutdown current vs ambient temp



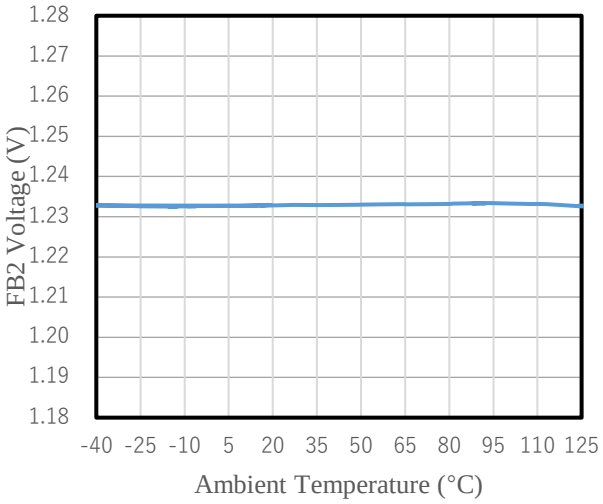
I_O=0.1mA

Figure 8-3 Quiescent current vs ambient temperature



I_{O1}=0.1mA

Figure 8-4 FB1 voltage vs ambient temperature



I_{O2}=10mA

Figure 8-5 FB2 voltage vs ambient temperature

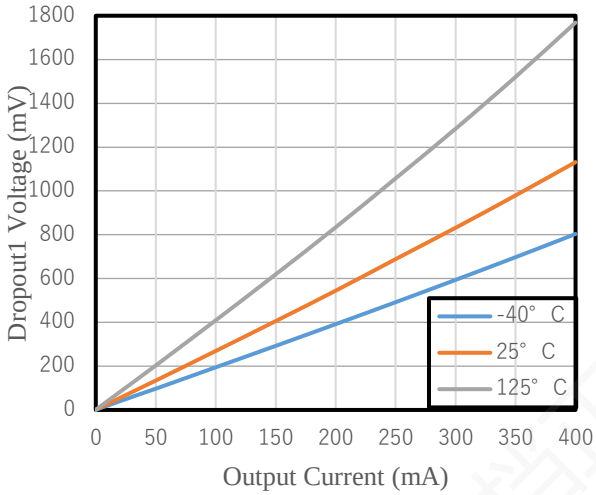


Figure 8-6 Dropout1 voltage vs output current

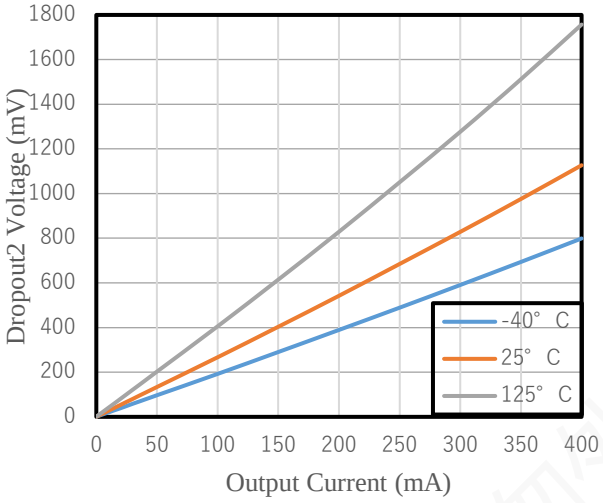


Figure 8-7 Dropout2 voltage vs output current

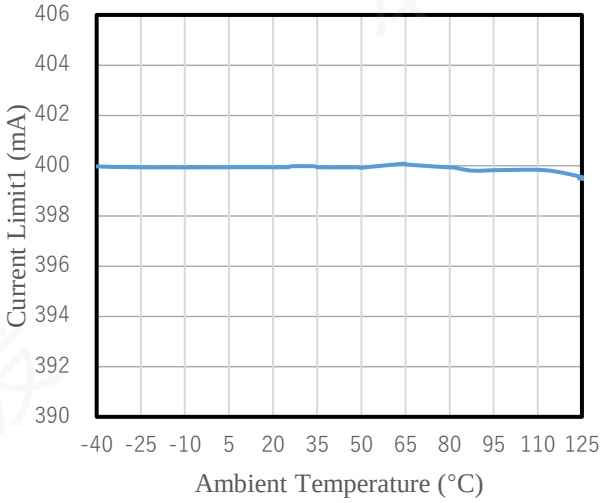


Figure 8-8 Current limit1 vs ambient temperature

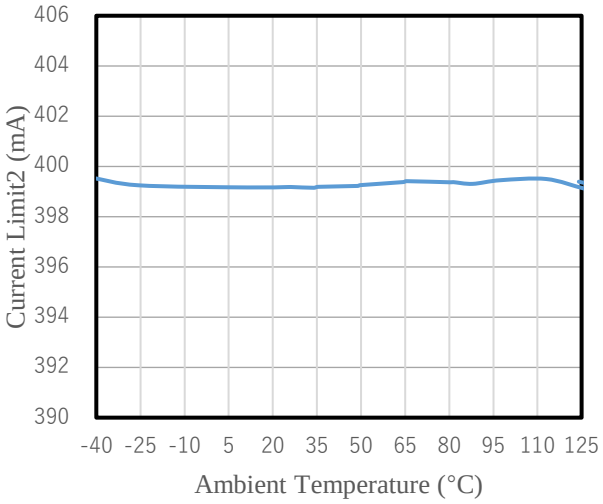


Figure 8-9 Current limit2 vs ambient temperature

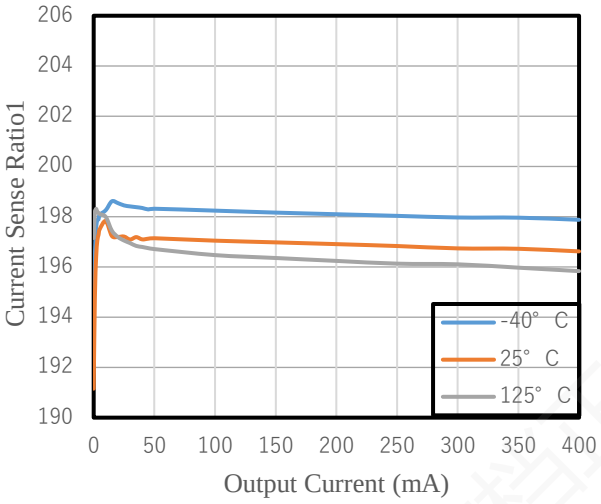


Figure 8-10 Current sense1 ratio vs output1 current (I_{OUT1}/I_{CS1})

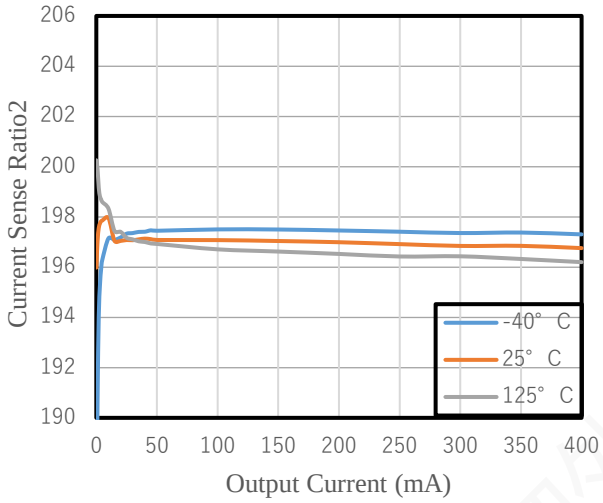


Figure 8-11 Current sense2 ratio vs output2 current (I_{OUT2}/I_{CS2})

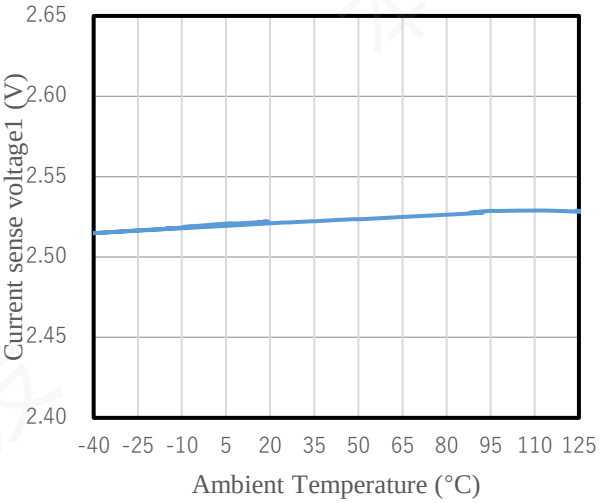


Figure 8-12 Current sense1 voltage at CL vs temperature

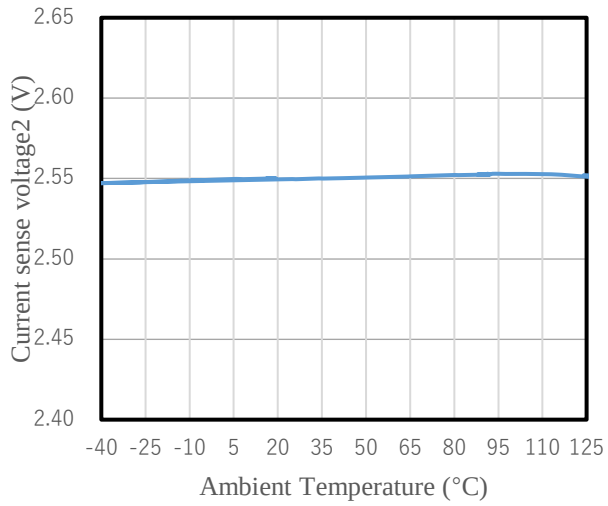


Figure 8-13 Current sense2 voltage at CL vs temperature

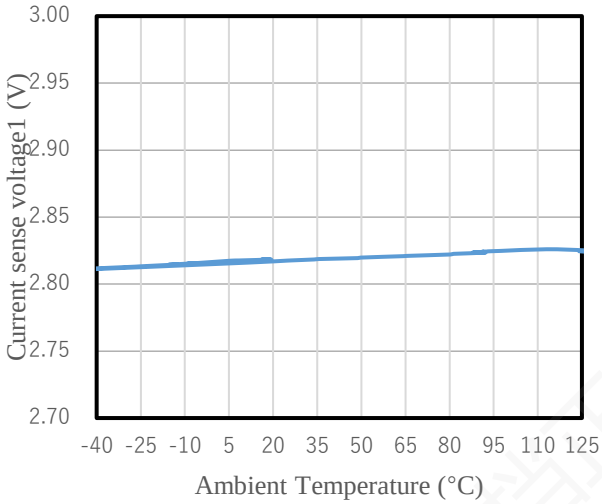


Figure 8-14 Current sense1 voltage at TSD vs temperature

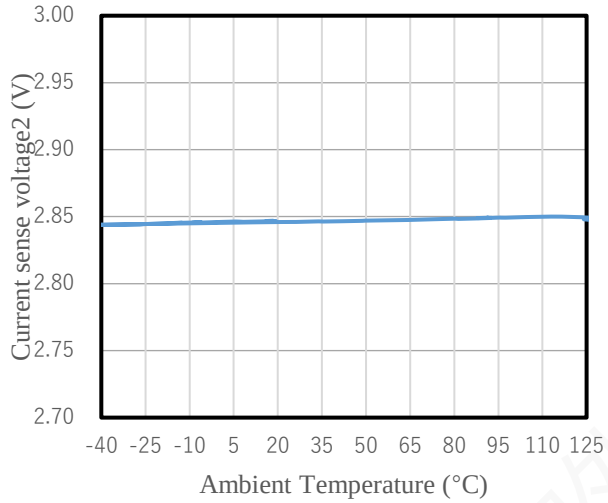


Figure 8-15 Current sense2 voltage at TSD vs temperature

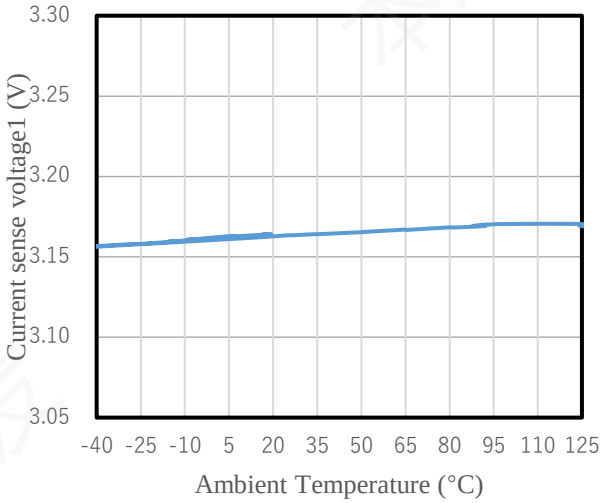


Figure 8-16 Current sense1 voltage at STB vs temperature

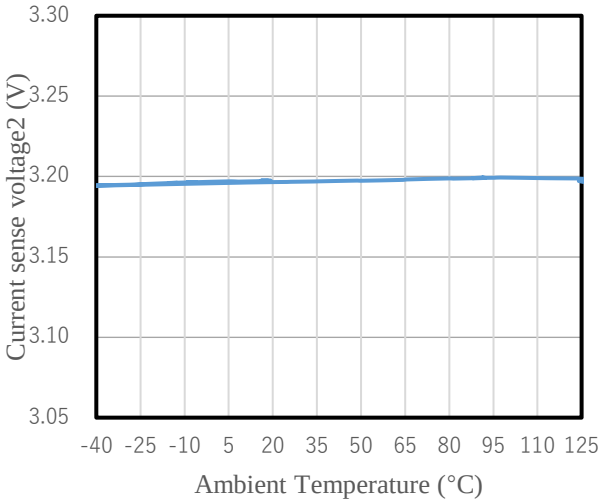


Figure 8-17 Current sense2 voltage at STB vs temperature

9 Functional Block Diagram

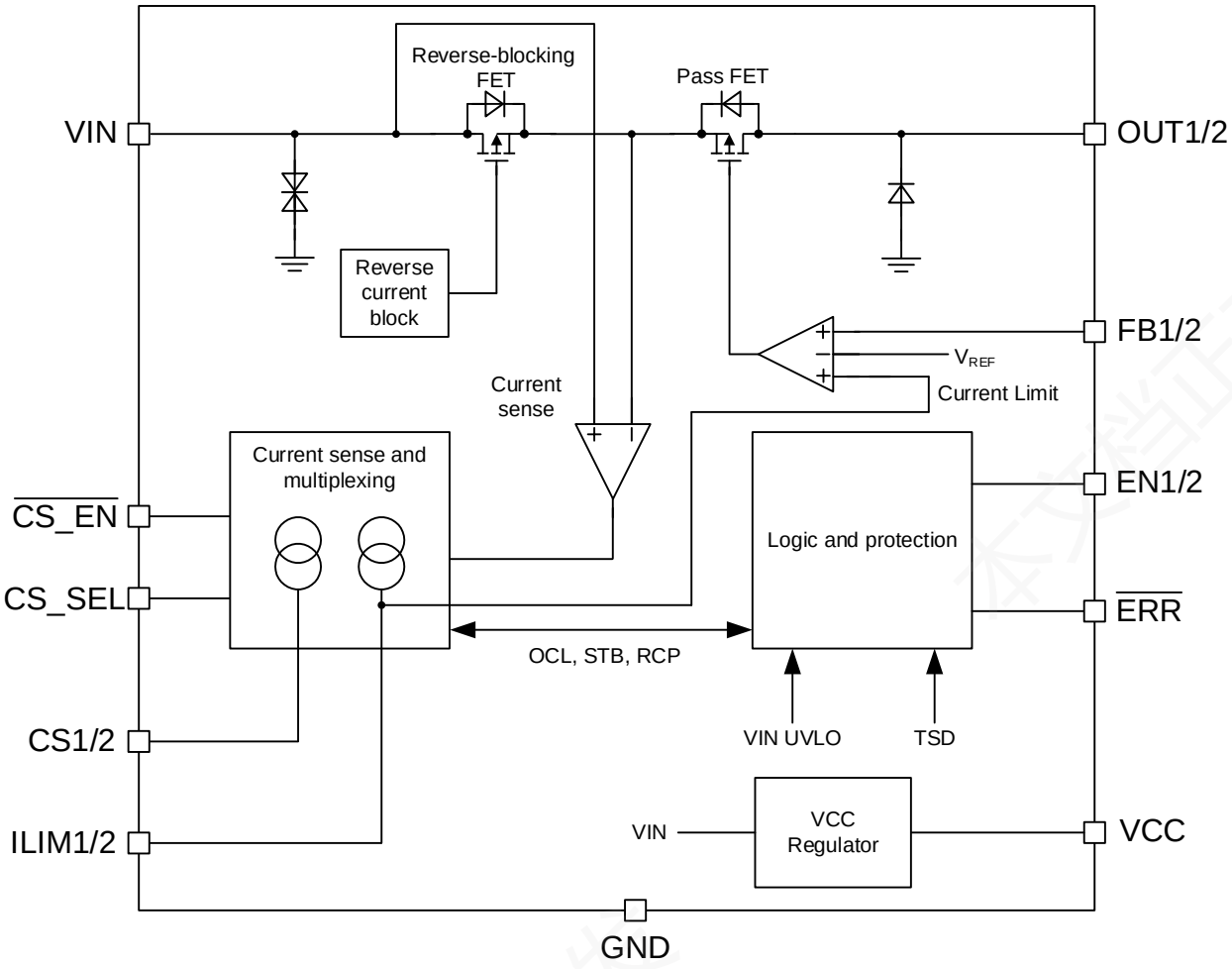
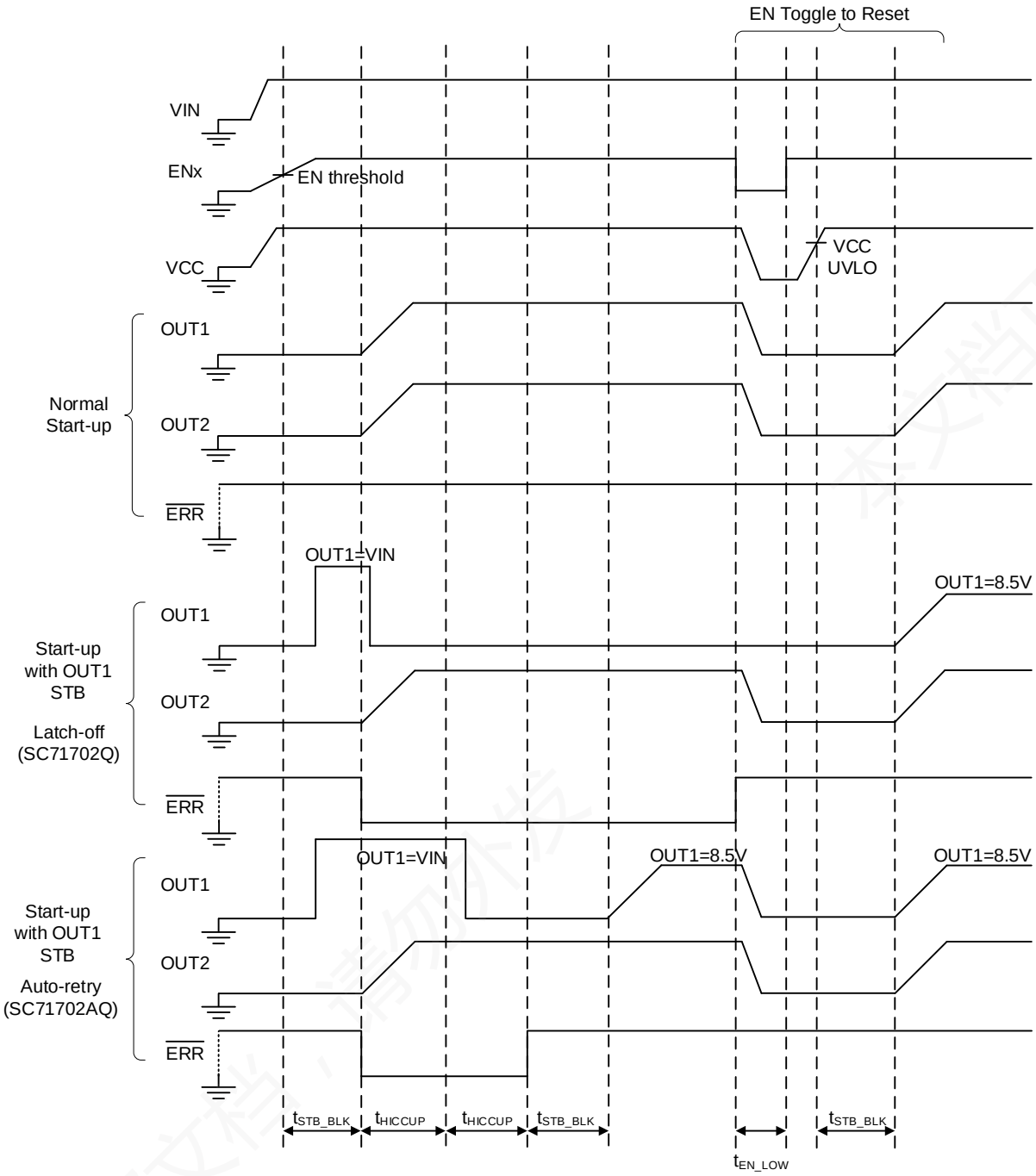


Figure 9-1 Functional Block Diagram

10 Timing Sequence



/ERR pin is pulled up by external power supply.

Figure 10-1 Timing Sequence for Start-up, Latch-off and Auto-retry

11 Feature Description

11.1 Overview

The SC71702Q is a dual-channel low-dropout regulator (LDO) family, designed to operate for a wide input voltage range from 4.5-V to 36-V (40-V load dump capability). Capable to supply 400-mA per channel, SC71702Q provides full protection and diagnostics of automotive off-board loads and applications. In addition, 1.5-V to 22-V output voltage range and configurable power switch mode make SC71702Q very flexible. The current limit is also adjustable through ILIMX (ILIM1 and ILIM2) pins.

Through implementing CSX (CS1 and CS2) pins, SC71702Q is able to report accurate current information per channel. The CSX pins are also used to report faults of open-circuit, Over Current Limit (OCL), Short Circuit Protection (SCP), Short-to-Battery (STB), Reverse Current Protection (RCP) and thermal shutdown (TSD) to MCU by pulling up its voltage to different level. In order to save ADC resources, the current sense is multiplexed between channels per options of CS_SEL an $\overline{\text{CS\_EN}}$.

The devices integrate Back-to-Back (B2B) FET structure, which eliminates the need of extra input diode. The internal diode between OUTX (OUT1 and OUT2) and GND provides inductive clamp protection in case of inductive loads during shut-down.

11.2 Fault Detection and Diagnostics

SC71702Q integrates both analog pins CSX (CS1 and CS2) and digital pins $\overline{\text{ERR}}$ to diagnose and report faults in different operating conditions.

The CSX pins are multiplexed to be either precise current sense of interested channel, or full diagnostics of different faults in relevant conditions. Before entering current limit, the CSX pins source out current which is linearly proportional to the according channel's load current. With resistors R_{SNS} on CSX pins, the CSX's voltage is also proportional to the load current. After device enters current limit mode, CSX pin's voltage is clamped to V_{CS_OCL}.

When device enters thermal shutdown mode or short to battery (STB)/Reverse current protection (RCP) mode, the CSX pin's voltage is set to the fault voltage level V_{CS_TSD} and V_{CS_STB}, respectively. Refer to **Figure 11-1** for detailed demonstration of SC71702Q's current sense, fault detection and diagnostics.

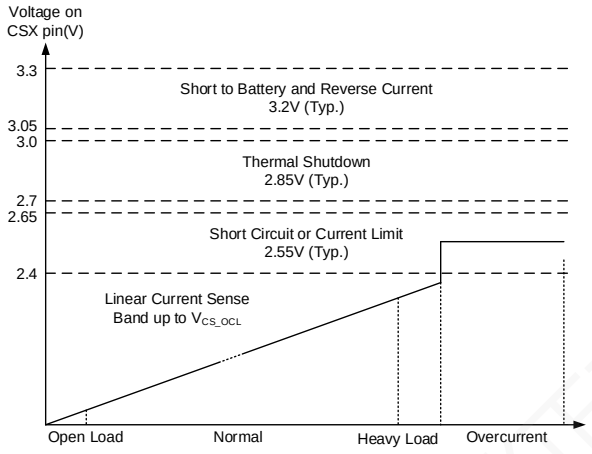


Figure 11-1 Current-sense Output and Its Multiplexing

11.2.1 Current Sense and Multiplexing

SC71702Q provides individual current sense pins CSX (CS1 and CS2), in order to provide load information as well as fault reporting to MCU. Through implementing CS_SEL an $\overline{\text{CS\_EN}}$ pins, the device can help save ADC resources to report both channel's current and fault information by CS1.

In linear current sense band, before device enters current limit, CSX (CS1 and CS2) pins output current is proportional to the output current at the OUTX (OUT1 and OUT2) with a factor of 1/198. A current sense resistor R_{SNSX}, must be tied between CSX and GND to generate current sense voltage to MCU's ADC. To make current sense loop stable, a 1-µF high quality ceramic capacitor needs to be used and is parallel to R_{SNSX}. Refer to **Figure 11-2** for current sense configuration. **Equation 1** can be used to calculate the voltage generated at CSX pins.

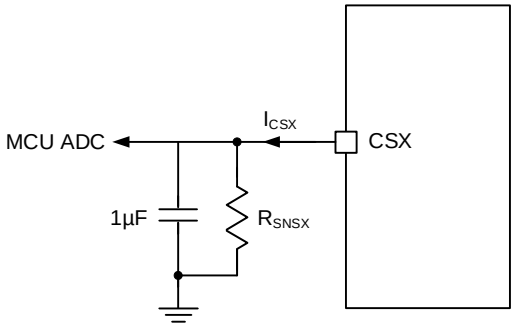


Figure 11-2 Current Sense Configuration

$$V_{CSX}=I_{CSX}\times R_{SNSX} \quad (1)$$

In **Equation 1**, the relationship between CSX current output I_{CSX} and individual channel's output current I_{OUTX} is:

$$I_{CSX}=\frac{I_{OUTX}}{198} \quad (2)$$

To avoid overlap between linear current sense band and short circuit and current limit band, **Equation 3** can be used to determine the R_{SNSX}'s maximum value R_{SNS_MAX}.

In equation:

- 198 is the output current to CSX output current ratio;
- 2.4V is the minimum possible voltage at the CSX pin when device is operating in overcurrent limit;
- I_{OUT_MAX} is the maximum possible output current in normal operation.

$$R_{SNS\_MAX}=\frac{198\times 2.4V}{I_{OUT\_MAX}} \quad (3)$$

The CS_SEL and $\overline{CS\_EN}$ pins (SC71702Q Only) configure CS1 and CS2 to monitor channel's load current. The $\overline{CS\_EN}$ enables and disables the CSX pins, allowing current sense multiplexing between chips. This can help MCU monitor multi-channel's current and fault information between multi-chips with only one ADC used. When CS1 is tied to an ADC, the current flow through both channels can be sensed and reported by changing the CS_SEL.

See **Table 1** for detailed CS_SEL and $\overline{CS\_EN}$ logic for selection of CSX pins reporting.

$\overline{CS\_EN}$	CS_SEL	CS1	CS2
LOW	LOW	CH1	CH2
LOW	HIGH	CH2	HIGH Impedance
HIGH	X	HIGH Impedance	HIGH Impedance

Table 1 CSX Multiplexing Logic

Figure 11-3 shows the application scheme of two-chip, four-channel output monitoring using only one ADC.

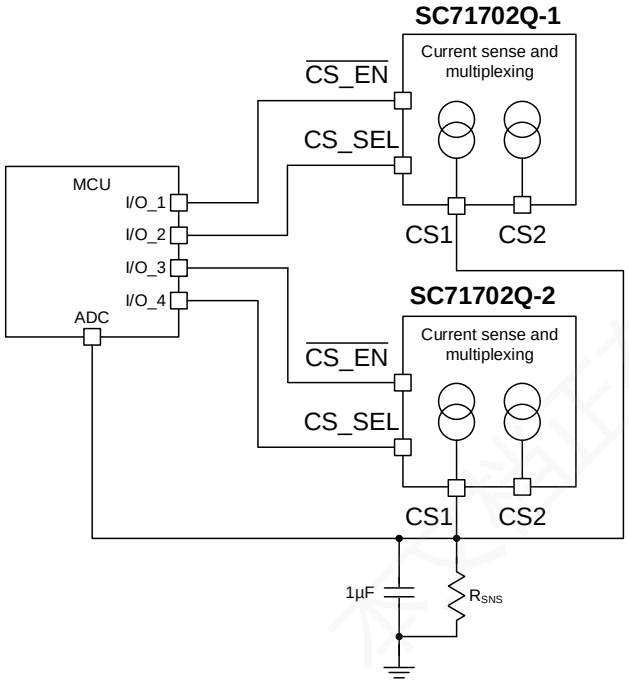


Figure 11-3 Current Sense Multiplexing Scheme

11.2.2 Over Current Limit and Short Circuit Protection

SC71702Q devices integrates current limit to protect the down-streaming loads from short circuit. The current limit threshold can be programmed through an external resistor R_{ILIM} on ILIMX (ILIM1 and ILIM2) pins. The voltage on ILIMX pins is compared with the internal voltage reference. When the threshold is exceeded, the current limit is triggered. The output current of the channel continues to remain on but is limited.

In current limit operation, the $\overline{ERR}$ pin asserts low and the according fault channel's CSX (CS1, CS2) pin's voltage is pulled up to the current limit band, i.e. 2.4V to 2.65V as what has been demonstrated in **Figure 11-1**. Therefore, the $\overline{ERR}$ and CSX pins can be used to report fault. The MCU should monitor device's pins and turn off relevant channel by pulling ENX (EN1 and EN2) low. If the current limit persists, die temperature may rise high. Thermal shutdown then can be triggered to further protect the device.

11.2.3 Short-to-battery Fault Detection

Shorting the output to the battery because of a fault in an off-board system is possible. SC71702Q provides short-to-battery fault detection through comparing the voltage between the OUTX (OUT1 and OUT2) pins and VIN pin before the LDO switch is turning on. When the device is enabled on the rising edge of the ENX (EN, EN1 and EN2) pins, VCC UVLO releasing or during the exiting of the thermal shutdown, a 15-ms(typ.) short-to-battery fault

detection window starts. In the detection window if at any moment the device detects the short-to-battery fault, short-to-battery fault is triggered. The device then latches off its LDO switch, or starts auto-retry cycles, depending on the default fault logic setting. In addition, the $\overline{ERR}$ pin is asserted low and the associated fault channel's CSX pin voltage is pulled up internally to short-to-battery and reverse current band i.e. 3.05V to 3.3V. The other channel which does not have fault is not influenced and starts up normally. **Figure 11-4** shows detailed short-to-battery detection mechanism.

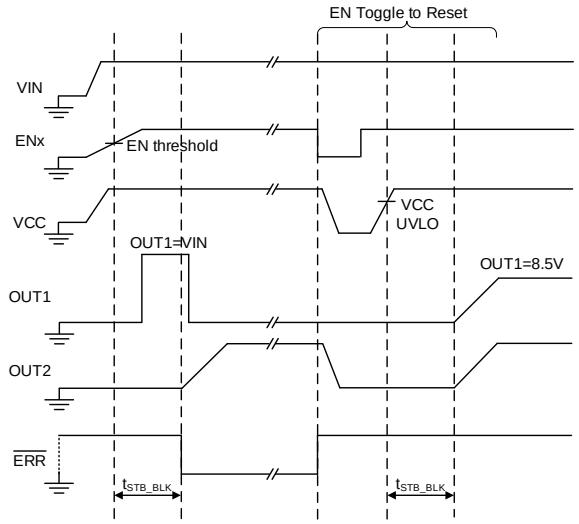


Figure 11-4 Short-to-battery Detection Window

If the fault condition is removed, for latch-off version (SC71702Q), the device needs to toggle EN or recycle the VIN in order to recover from latched off state.

11.2.4 Auto-retry Logic (For SC71702AQ only)

The customer option SC71702AQ provides auto-retry feature which restarts the device automatically without EN or VIN toggle, after short-to-battery and reverse current failure is cleared. **Figure 11-5** describes detailed mechanism of auto-retry.

In order to prevent failed short-to-battery detection when there is large inductance on output cable, a signal STB_STAT and STB deglitch time t_{STB_DGT} are introduced. STB_STAT is pulled high when V_{OUT1}-V_{IN} is higher than V_{STB_TH}. At the end of STB detection window t_{STB_BLK}, STB is detected and $\overline{ERR}$ is asserted low. After that, a 30-ms(typ.) hiccup off timer t_{HICCUP} starts. If STB is cleared (V_{OUT1}-V_{IN} is lower than V_{STB_TH}) early so that STB_STAT is pulled low with a deglitch time t_{STB_BLK} before hiccup off timer t_{HICCUP} ends, device restarts after a STB detection window t_{STB_BLK} and $\overline{ERR}$ recovers.

The **Figure 11-6** shows another example. If STB is cleared (V_{OUT1}-V_{IN} is lower than V_{STB_TH}) late so that STB_STAT is pulled low with a deglitch time t_{STB_BLK} after hiccup off timer t_{HICCUP} ends, another hiccup off timer starts. If at the end of the last hiccup off time the STB_STAT is low, the device restarts after a STB detection window t_{STB_BLK}.

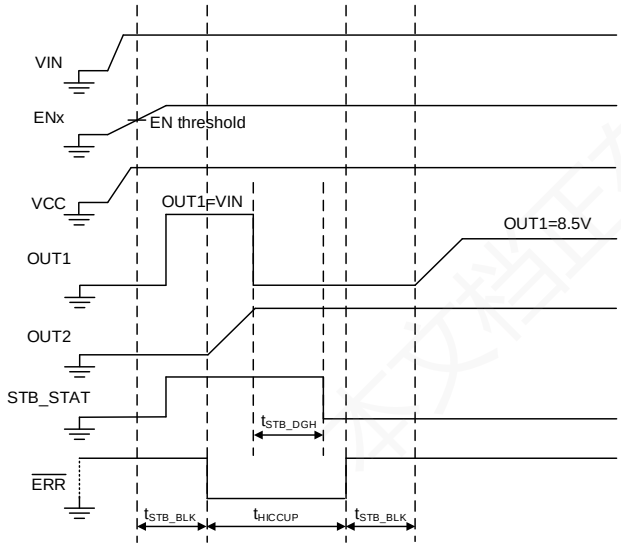


Figure 11-5 Auto-retry Mechanism_1

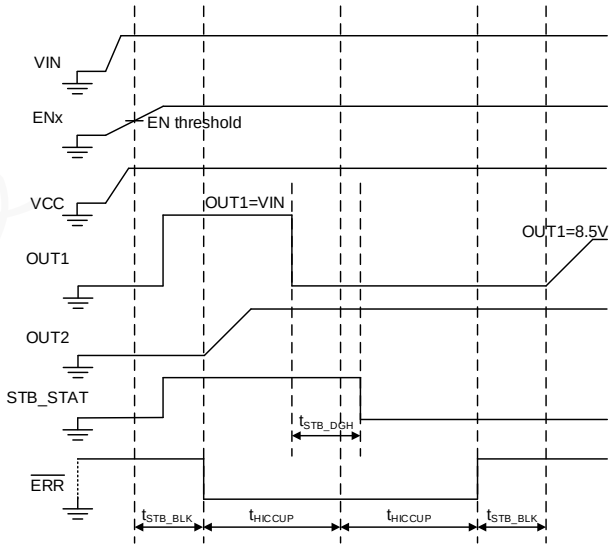


Figure 11-6 Auto-retry Mechanism_2

11.2.5 Reverse Current Protection

Series inductance and the output capacitor can produce L-C ringing during power up or recovery from current limit, which introduces output voltage that temporarily exceeds the input voltage. There is a 15-ms(typ.) t_{RC_BLK} reverse current blanking time to filer this ringing.

For SC71702Q, if both channels are enabled and one channel is shorted to ground after power up, the current

drawn from input capacitor can lead to voltage dip in the input voltage, which can trigger reverse current protection. A 3-µs(typ.) t_{RC_DGT} reverse current deglitch time is implemented to help filter this false protection event.

However, the deglitch time may not be long enough to filter all false trigger scenarios. For example, if one channel is set in switch mode and has no load, while another channel is suddenly short to ground, the reverse current can last longer than t_{RC_DGT} and still triggers reverse current protection. Therefore, it is strongly recommended to increase input capacitance to avoid false trigger event while selecting input capacitors.

11.2.6 Thermal Shutdown

The device integrates thermal shutdown feature in order to protect the device from overheat. If the junction temperature rises above 175-°C(typ.) T_{SD} threshold, the LDO switch is turned off. After junction temperature decreases by T_{SD_HYS}, the device tries to start up again. The CSX (CS1 and CS2)'s voltage is pulled up between 2.7-V and 3.3V when device is in thermal shutdown.

It should be noted that thermal shutdown is designed to protect device from overload conditions and is not intended to replace proper heat-sink. Continuously running the device into thermal shutdown state degrades device long-term reliability.

11.3 Integrated Reverse Polarity Protection

The devices integrate Back-to-Back (B2B) FET structure, which implements a reverse connected PMOS in series of pass FET. This structure blocks reverse current during reverse input polarity and short-to-battery failures, and eliminates the need of input diode, which helps save BOM cost and solution size. **Figure 11-7** describes simplified B2B structure.

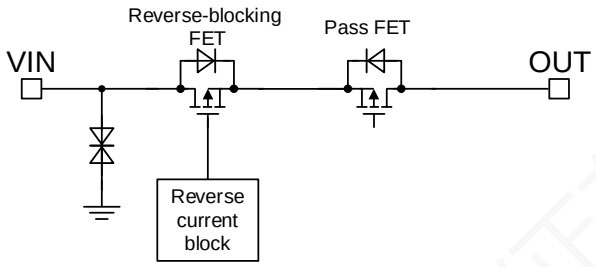


Figure 11-7 Back-to-Back FET Structure

11.4 Integrated Inductive Clamp

After output is turned off, the cable inductance continuous to source the current output of the device. In order to provide robust operation and protect the device, SC71702Q integrates an inductive clamp to help dissipate the inductive energy stored in cable lines. This structure is achieved by placing an internal diode between OUTX and GND pins with 400-mA DC current capability.

11.5 Under Voltage Lock-out

Device integrates input under voltage lock-out feature to protect the device from insufficient input supply. There is about 500-mV(typ.) hysteresis to help filter input ringing during and after start-up.

Table 2 Fault Table

Fault Mode	V_{CSX}	$\overline{ERR}$	LDO Switch output	Latch Version	Auto-retry Version
Open load	$\frac{I_{OUTX} \times R_{SNSX}}{198}$	HIGH	Enabled	No	No
Normal		HIGH	Enabled	No	No
Heavy load		HIGH	Enabled	No	No
Short-circuit or current limit	2.4 to 2.65V	LOW	Enabled	No	No
Thermal shutdown	2.7 to 3V	LOW	Disabled	No	No
Output short-to-battery	3.05 to 3.3V	LOW	Disabled	Latched	Auto Retry
Reverse current	3.05 to 3.3V	LOW	Disabled	Latched	Auto Retry

11.6 Enable and Disable

SC71702Q integrates ENX (EN1 and EN2) pins to provide user-programmable enable and disable function for relevant output channel. ENX pins have 500-kΩ pull-down resistance. Once ENX is pulled high, the current into ENX pins is limited below 10-μA (max.).

11.7 FB and Output Voltage Setting

Output voltage can be adjusted externally through feedback divider network on FB pin, as what has been shown in **Figure 11-8**. In LDO mode, output voltage can be adjusted from 1.5-V to 22-V by selecting feedback divider resistance from **Equation 4**. The SC71702Q can also be used as a current-limited switch by connecting the FB pin to the GND pin (switch mode) to fully turn on LDO switches. The output voltage of switch mode in no load is same as input voltage, and can be above 22-V.

$$1.233=\frac{R_2}{R_1+R_2}\cdot V_{OUT} \quad (4)$$

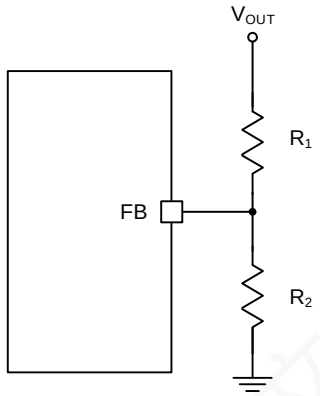


Figure 11-8 Feedback Network

12 Application Information

The SC71702Q, as a dual-channel low-dropout regulator (LDO) family, is specifically designed for automotive off-battery power applications, such as automotive antenna, camera and microphones, providing reliable and accurate current sense, current limit and fault diagnostics functionalities.

Figure 6-1 demonstrates typical application circuits of SC71702Q.

12.1 Design Procedure

The following sections describe detail design procedure for parameters listed in **Table 3** as an example.

Table 3 Example Design Parameters

PARAMETERS	VALUE EXAMPLE
Input voltage range	9V to 16V, battery supplied
Output voltage	8.5V for OUT1 5V for OUT2
Maximum output current	100mA for OUT1 200mA for OUT2
Output current limit	200mA for OUT1 300mA for OUT2

12.1.1 Input Capacitor

Input decoupling capacitors are needed for the device, depending on different applications. Typical value for input capacitor is 10μF. There are mainly considerations in capacitor selections.

The first one is voltage rating. The voltage rating for the capacitor should always be larger than application's maximum input voltage. In terms of automotive battery supplied application, voltage rating higher than 36V is usually needed.

When one channel is configured in switch mode and another channel is suddenly short to GND, input voltage can have a temporary drop. If the input capacitor capacitance is not enough, voltage drop can result in reverse current protection triggered for the switch mode channel. This is especially more severe if the channel in switch mode has very light load. Increase capacitor's actual capacitance, or add bulk capacitor can help reduce the voltage drop and prevent false reverse current protection triggering.

In this design example, a 10μF rating capacitance, X7R/50V, automotive capacitor is selected.

12.1.2 Output Capacitor

The device needs output capacitor to make loop stable. The output capacitance range is between 2.2μF to 100μF with ESR from 0Ω to 5Ω. It is recommended to select a low ESR capacitor with higher capacitance rating if load transient performance is important.

In addition, a 100nF high quality ceramic capacitor is recommended to be used to increase PSRR at high frequency band.

If any line inductance at output lines, output capacitors must be placed close to IC so that loop stability is not disturbed by output inductance in lines.

In this design case, one 100nF/X7R/50V automotive ceramic capacitor and one 10μF/X7R/50V automotive ceramic capacitor are used for each output channel.

12.1.3 Current Sense Resistor Selection

The device reports output current through CS1 and CS2 pins. CS1 and CS2 pins' output current are proportional to the output current at the OUT1 and OUT2 with a factor of 1/198. Therefore, an output resistor R_{SNS} must be used between CSX and GND to convert current to voltage for external ADC to sample. Refer to **Section 12.2.1** for detailed R_{SNS} calculation.

In this example, maximum output current is 100mA for OUT1 and 200mA for OUT2. Therefore, the maximum R_{SNS} for OUT1 and OUT2 are:

$$R_{SNS1\_MAX}=\frac{198\times 2.4V}{100mA}=4.752k\Omega$$

$$R_{SNS2\_MAX}=\frac{198\times 2.4V}{200mA}=2.376k\Omega$$

The nearest resistor value of 4.7kΩ for R_{SNS1} and 2.2kΩ for R_{SNS2} are selected.

Table 4 lists current sense accuracy across temperature.

Table 4 Output Current Sense Accuracy Summary

OUTPUT CURRENT	SENSE ACCURACY
1mA	±50%
2mA	±25%
3mA	±20%
4mA	±15%
$5mA\le I_{OUT}<50mA$	±10%
$50mA\le I_{OUT}<100mA$	±5%
$100mA\le I_{OUT}\le 400mA$	±3%

12.1.4 Current Limit Resistor Selection

The device reports output current limit status through ILIM 1 and ILIM2 pins. ILIM 1 and ILIM2 pins' output current are proportional to the output current at the OUT1 and OUT2 pins and is internally connected to a current-limit comparator referenced to 1.233 V. Therefore, a resistor $R_{LIM}X$ could be selected between ILIMX and GND to program the current limit of OUTX pin. The internal current limit of the device is set by shorting the ILIMX pin to ground.

In this example, output current limit is 200mA for OUT1 and 300mA for OUT2. Therefore, the $R_{LIM}X$ for OUT1 and OUT2 are:

$$R_{ILIM1}=\frac{198\times1.233V}{200mA}=1.220k\Omega$$

$$R_{ILIM2}=\frac{198\times1.233V}{300mA}=0.813k\Omega$$

The nearest resistor value of 1.2kΩ for R_{LIM1} and 0.82kΩ for R_{LIM2} are selected.

12.2 Application Curves

V_{IN} = 14V, V_{OUT1}=8.5V, V_{OUT2}=5V, unless otherwise noted.

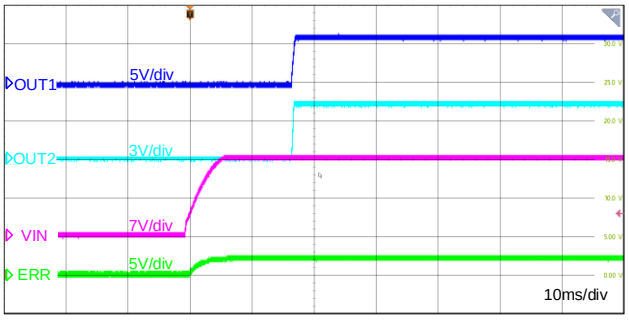


Figure 12-1 Power Up (V_{IN}=14V，IO = 100 mA)

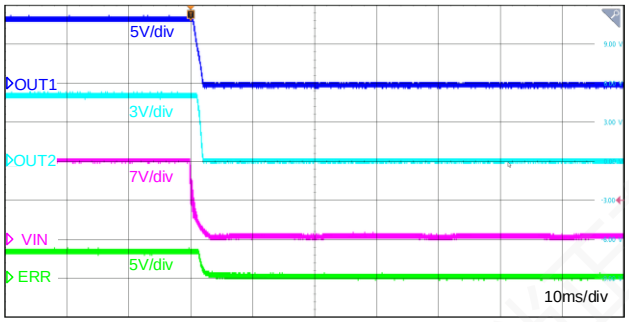


Figure 12-2 Power Down (V_{IN}=14V，IO = 100 mA)

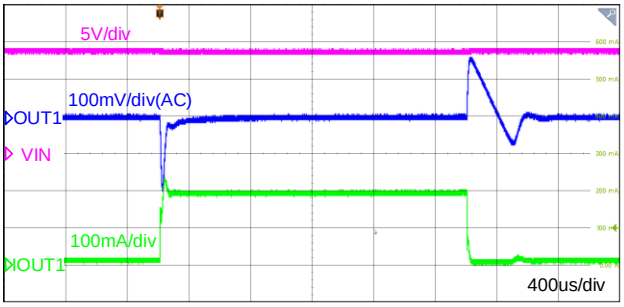


Figure 12-3 I_{OUT1}=10-mA to 200-mA Load Transient

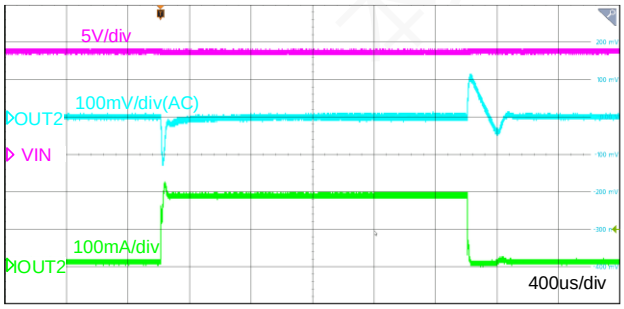


Figure 12-4 I_{OUT2}=10-mA to 200-mA Load Transient

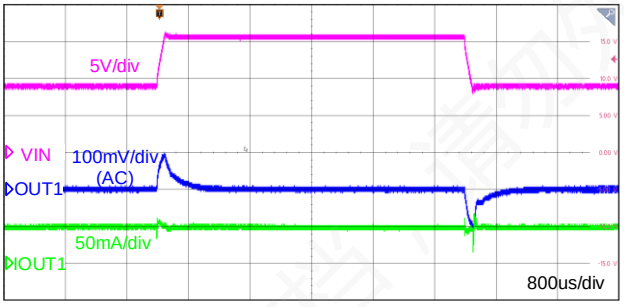


Figure 12-5 9-V to 16-V Line Transient (I_{OUT1}=50mA)

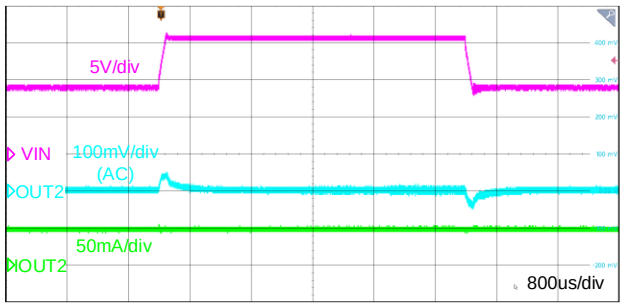


Figure 12-6 9-V to 16-V Line Transient (I_{OUT2}=50mA)

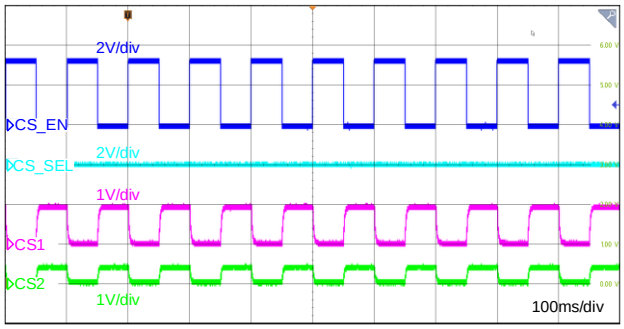


Figure 12-7 Current Sense Enable and disable

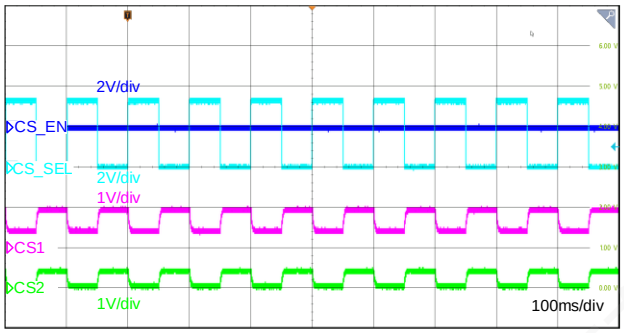


Figure 12-8 Current Sense Multiplexing

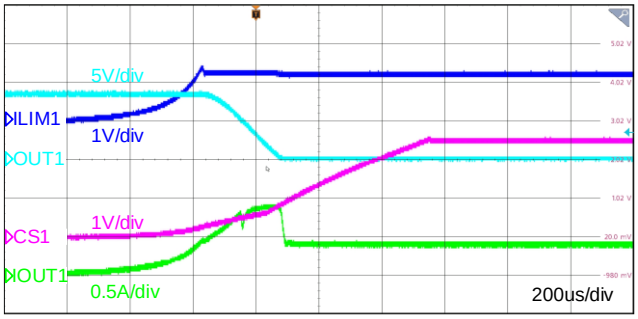


Figure 12-9 Current Limit

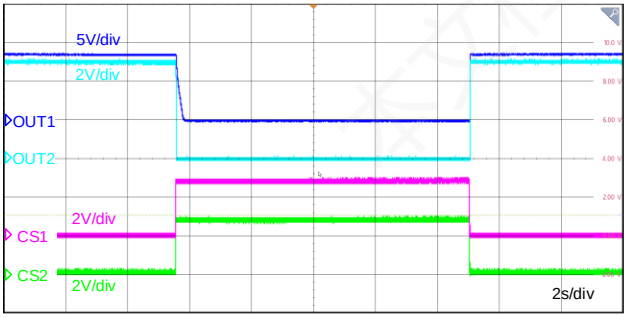


Figure 12-10 Thermal Shutdown Protection

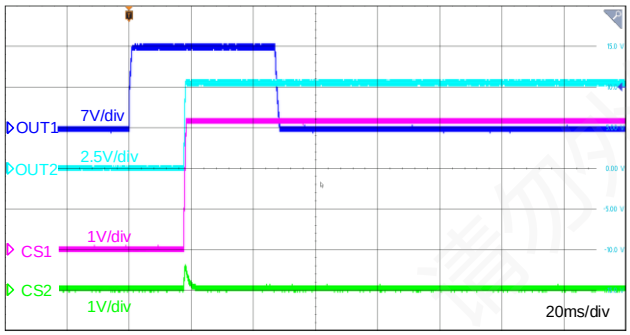


Figure 12-11 Short-to-battery Protection(Latch)

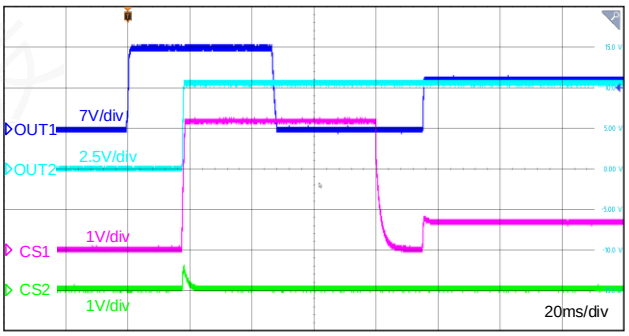


Figure 12-12 Short-to-battery Protection(Retry)

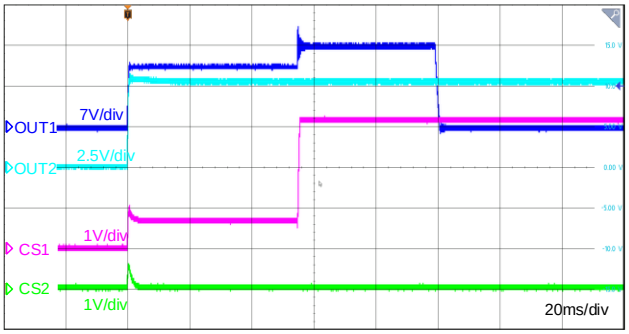


Figure 12-13 Reverse Current Protection(Latch)

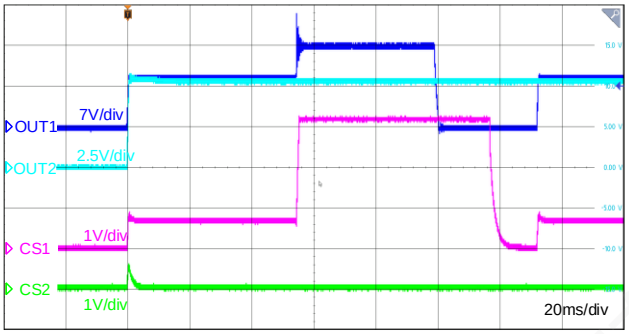


Figure 12-14 Reverse Current Protection(Retry)

13 Layout Guide

For the layout of SC71702Q device, the layout guide recommends are as followed:

- Place any of the capacitors on the same side of the PCB from where the regulator is installed.
- Place every capacitor as close as possible to the device.
- Put some via holes surrounding the device to enhance the thermal performance.

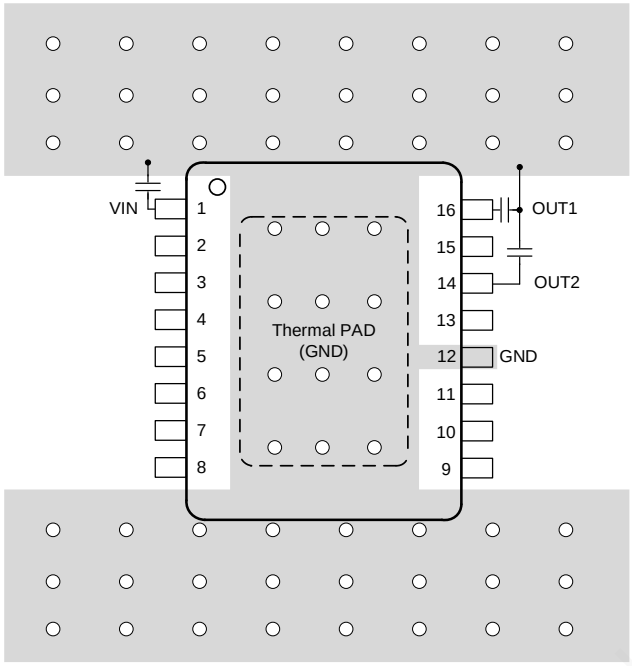
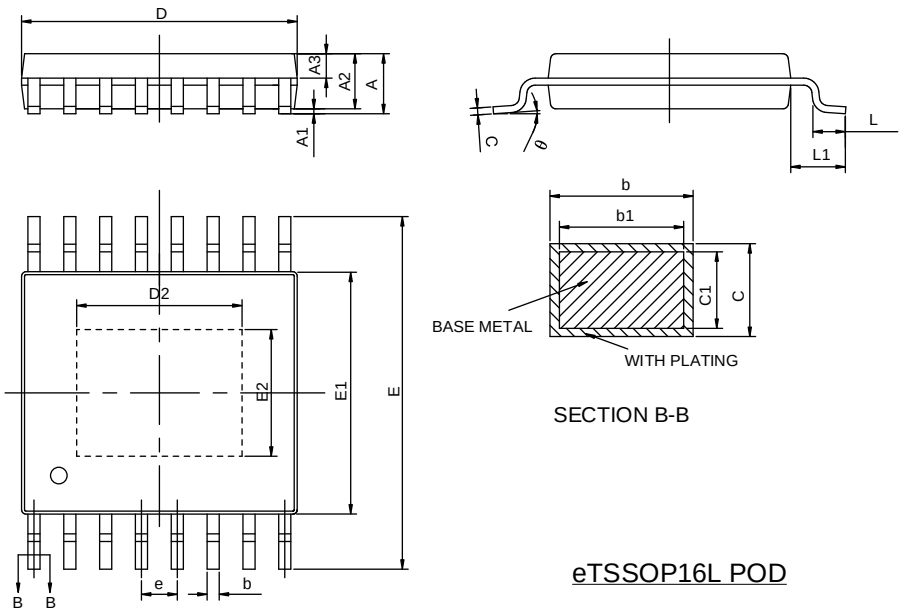


Figure 13-1 PCB Layout Example

14 PACKAGING INFORMATION

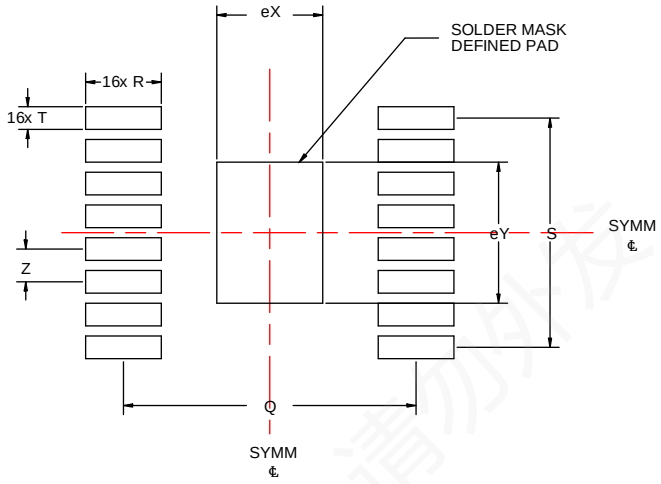


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.00	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	-	0.75
L1	1.00BSC		
θ	0	-	8°

L/F Size(mil) \ Size(mm)	D2	E2
91*118	2.80REF	2.10REF

eTSSOP16L POD

Unit：mm

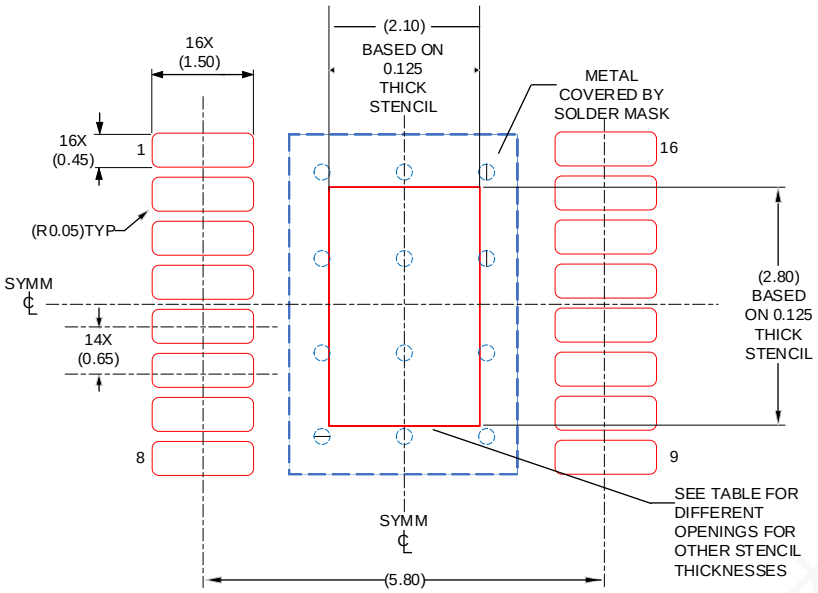


SYMBOL	TYPICAL
S	4.55
Q	5.80
R	1.50
T	0.45
Z	0.65 BSC
eX	2.10
eY	2.80

eTSSOP16L Land Pattern

Unit：mm

Example Stencil Design



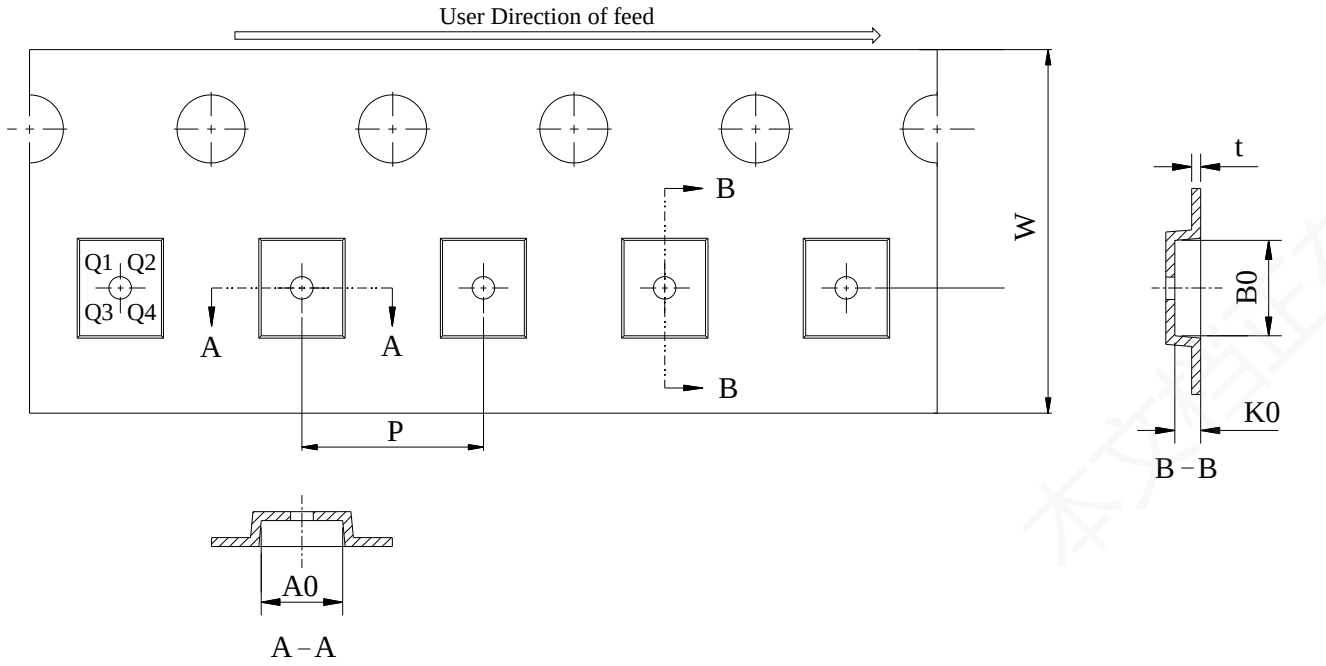
SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE: 10X

Unit: mm

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

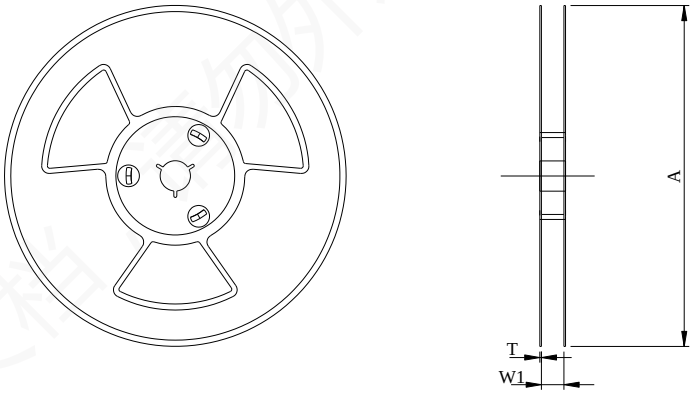
15 TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.0 ±0.1	8.0 ±0.1	6.8 ±0.1	5.4 ±0.1	1.3 ±0.1	0.3 ±0.05	Q1

REEL



Item	A	W1	T
Size (mm)	330±1	12.4 +1/-0	1.5±0.3

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