# Analog Signal Input Monaural, Filter Less 3.0W Class-D Amplifier

## FEATURES (Typical value, Ta=25°C)

- Supply voltage ($R_L$≥3.6Ω) 1.8V to 5.5V
- High Power ($V^+$=5V, THD+N=10%)
  - $R_L$=8Ω 1.7W
  - $R_L$=4Ω 3.0W
- Output LC Filterless Architecture
- Built-in Pop noise reduction(Turn on/Turn off)
- Analog Differential Input / PWM Output
- Low Supply Current ($V^+$=3.6V) 2.7mA
  - Standby Current 1μA max.
- Protection
  - Short-Circuit
  - Thermal Shut Down
  - Under Voltage Lock Out (UVLO)
- Space Saving Package
  - 1.45mm x 1.45mm WCSP9

## DESCRIPTION

The NJU8759 is an analog signal input monaural filterless class-D power amplifier. Operating voltage from 1.8V to 5.5V single supply can be used with 2-cell batteries.

NJU8759 features Class-D operation with high output capability, is 1.7W output (8Ω load) and 3.0W output (4Ω load). The BTL output configuration can reduce the coupling capacitor. Furthermore, the output LC filterless architecture, which was not available in conventional class-D, reduces external parts and PCB size.

The NJU8759 operates from a single power supply of 1.8 V and 1 μA maximum standby current, and is ideal for small portable devices and portable audio devices, as well as alarm devices and security devices that require low power and high output.

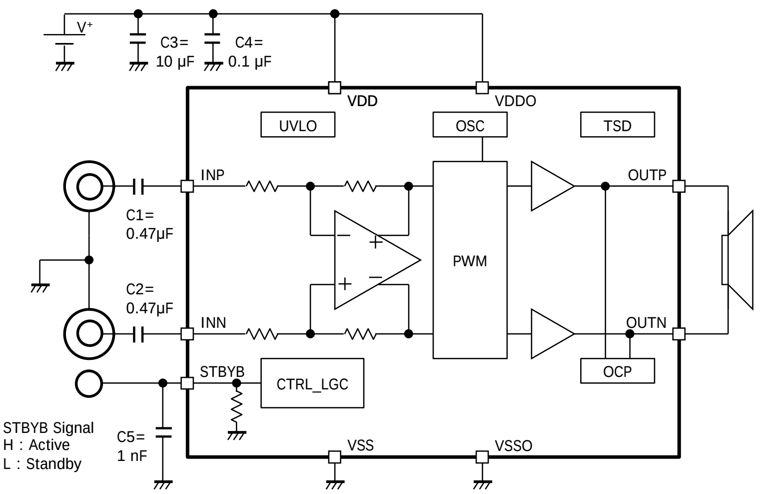
## APPLICATIONS

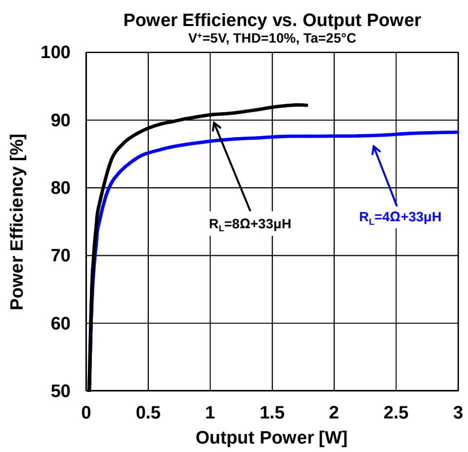
- Security equipment
- Portable Equipment
- Portable Audio

### MONAURAL POWER AMPLIFIER VARIATION

| PRODUCT NAME | Description |
|---|---|
| NJU72060 | 0.5W Class-AB Power Amp |
| NJU7089 | 1.2W 1.8V Class-AB Power Amp |
| NJU8759AGM1 | 3.0W Filter Less Class-D Amplifier with HSOP8 |

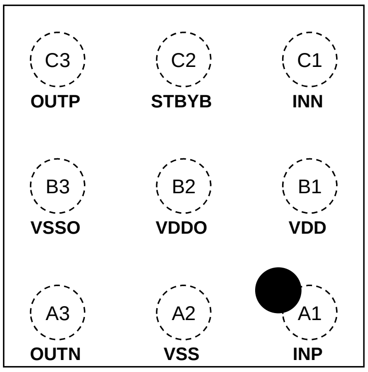
## ■ APPLICATION CIRCUIT



## ■ PIN CONFIGURATIONS

Top View




| PIN No. | SYMBOL | FUNCTION |
|---|---|---|
| A1 | INP | Positive input |
| A2 | VSS | Analog GND |
| A3 | OUTN | Negative output |
| B1 | VDD | Power supply |
| B2 | VDDO | Output power supply |
| B3 | VSSO | Power GND |
| C1 | INN | Negative input |
| C2 | STBYB | Standby control |
| C3 | OUTP | Positive output |

## ■ PRODUCT NAME INFORMATION

NJU8759 WLC1 (TE1)

Part Number / Package / Taping Form

## ■ ORDERING INFORMATION

| PRODUCT NAME | PACKAGE | RoHS | HALOGEN-FREE | TERMINAL FINISH | MARKING | WEIGHT (mg) | MOQ (pcs) |
|---|---|---|---|---|---|---|---|
| NJU8759WLC1 | WCSP9 | Yes | Yes | SnAgCu | 8759 | 1.9 | 3000 |

## ■ ABSOLUTE MAXIMUM RATINGS

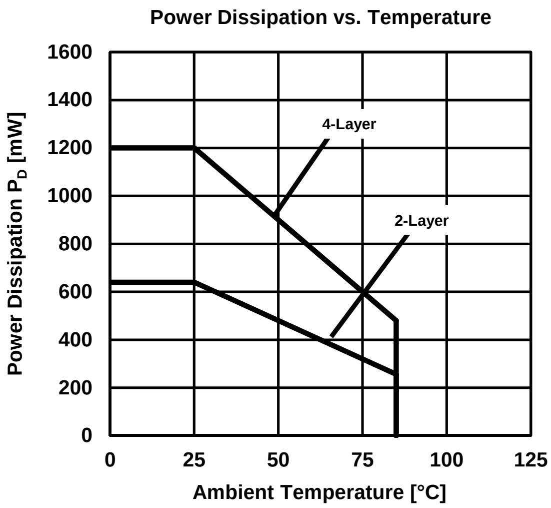
| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V^+ - V^-$ | 7 | V |
| Input Voltage | $V_{IN}$ | 0 to $V^+$ | V |
| Load Resistance | $R_L$ | ≥3.4Ω | Ω |
| Power Dissipation (Ta=25°C) WCSP9 | $P_D$ | 2-Layer / 4-Layer(1) 640 / 1200 | mW |
| Storage Temperature Range | $T_{stg}$ | -40 to 125 | °C |
| Maximum Junction Temperature | Tjmax | 125 | °C |

## ■ THERMAL CHARACTERISTICS

| PACKAGE | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Junction-to-Ambient Thermal Resistance WCSP9 | Θja | 2-Layer / 4-Layer(1) 156.6 / 83.4 | °C/W |

(1) 2-layer: Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2-layer FR-4, with Exposed Pad)
4-layer: Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4-layer FR-4, with Exposed Pad)
*For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



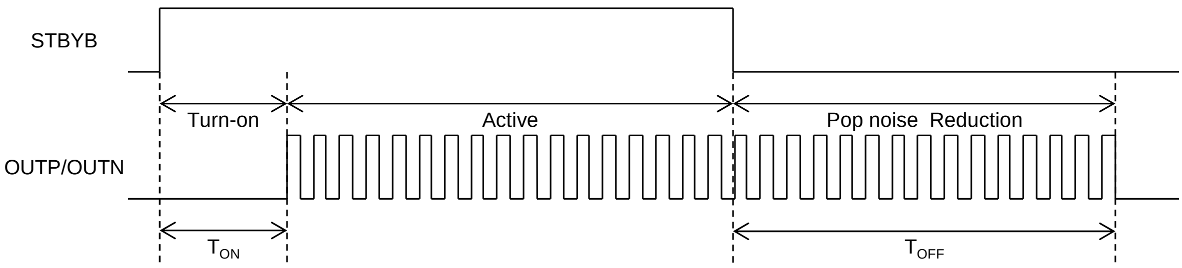

## ■ RECOMMENDED OPERATING CONDITIONS (VDD=VDDO=V+, VSS=VSSO=GND)

| PARAMETER | SYMBOL | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| Supply Voltage | $V^+$ | $R_L$≥3.6Ω | 1.8 to 5.5 | V |
| | | $R_L$≥3.4Ω | 2.0 to 5.5 | V |
| Operating Temperature Range | $T_{opr}$ | $R_L$≥3.6Ω | -40 to 85 | °C |
| | | $R_L$≥3.4Ω | -40 to 80 | °C |

■ **ELECTRICAL CHARACTERISTICS** ($V^+$=3.6V, Ta=25°C, unless otherwise noted.)

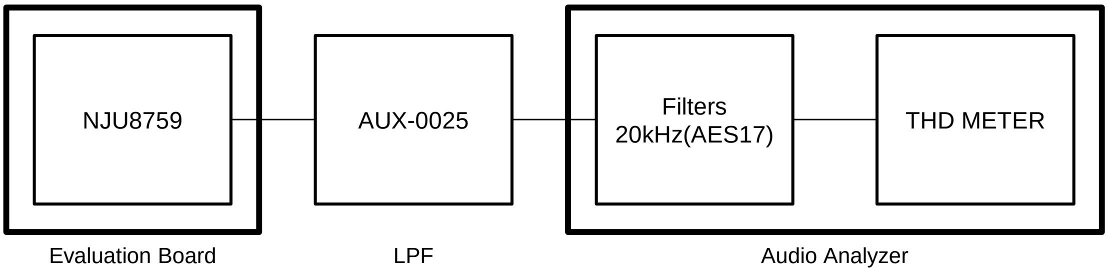
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| Standby Current | $I_{ST}$ | | - | - | 1.0 | μA |
| Supply Current | $I_Q$ | | - | 2.7 | - | mA |
| UVLO Detect Voltage | $V_{DDDET}$ | | 1.1 | 1.4 | 1.7 | V |
| UVLO Hysteresis Voltage | $V_{DDHYS}$ | | - | 0.05 | - | V |
| Digital Input Voltage | $V_{IH}$ | | 1.5 | - | VDD | V |
| | $V_{IL}$ | | 0 | - | 0.3 | V |
| Pull Down Resistance | $R_{DWN}$ | STBYB Terminal | - | 100 | - | kΩ |
| Input Resistance | $R_{IN}$ | INP, INN Terminal | - | 30 | - | kΩ |
| Switching Frequency | $f_{OSC}$ | | 100 | 250 | 395 | kHz |
| Turn On Time | $T_{ON}$ | | 10 | 16 | 40 | ms |
| Turn Off Time | $T_{OFF}$ | | 10 | 16 | 40 | ms |
| Voltage Gain | $A_V$ | | 17.5 | 18 | 18.5 | dB |
| Output Offset Voltage at Turn-ON / Turn-OFF | $V_{OS}$ | | -20 | - | 20 | mV |
| **AC CHARACTERISTICS** ($R_L$=8Ω,BW=20Hz to 20kHz, fin=1kHz, unless otherwise noted.) | | | | | | |
| Output Power | Po | $V^+$=5V, THD+N=10%, $R_L$=8Ω | - | 1.7 | - | W |
| | | $V^+$=5V, THD+N=10%, $R_L$=4Ω | - | 3.0 | - | W |
| Output Power Efficiency | η | $V^+$=5V, THD+N=10%, $R_L$=8Ω+33μH | - | 93 | - | % |
| Total Harmonic Distortion + Noise | THD+N | Po=0.5W | - | 0.05 | - | % |
| | | $V^+$=5V, Po=1.0W | - | 0.035 | - | % |
| Supply Voltage Rejection Ratio | PSRR | fin=217Hz, ripple=200m$V_{PP}$ | - | -55 | - | dB |
| Common-Mode Rejection Ratio | CMRR | fin=217Hz, Vinc=1$V_{PP}$ | - | -55 | - | dB |
| Output Voltage Noise | $V_{NO}$ | A-weighting | - | 62 | - | μV |

## ■ TURN ON / TURN OFF SEQUENCE

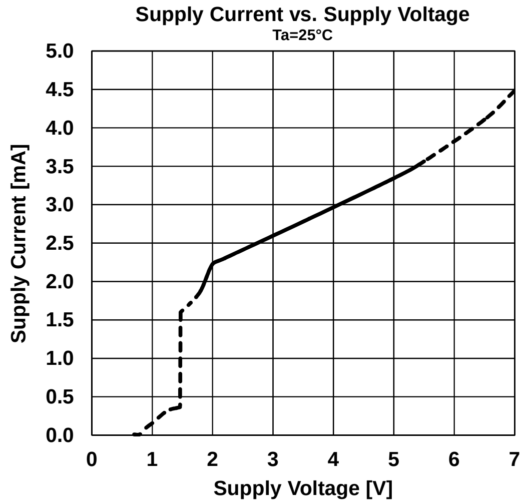


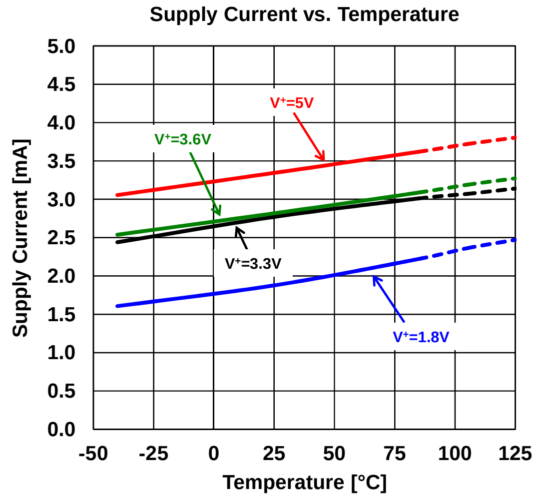

When STBYB is set to "H" in the TOFF, it shifts to Active mode immediately.

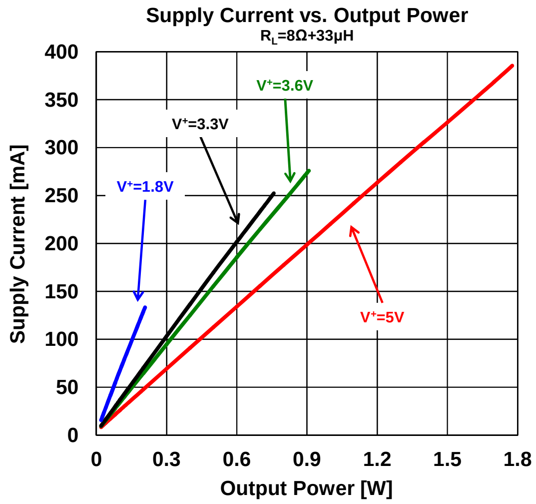
## ■ TEST SYSTEM OF THE OUTPUT THD+N

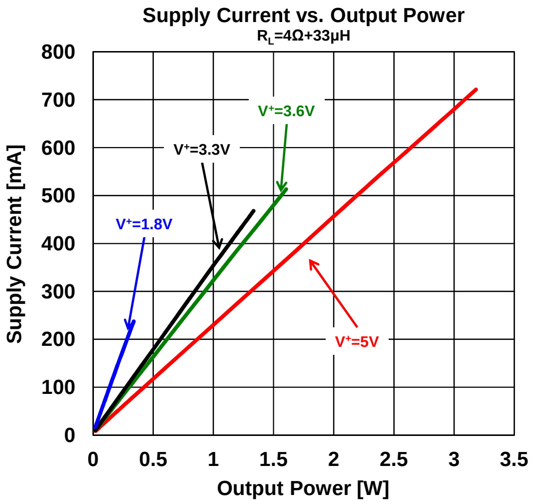


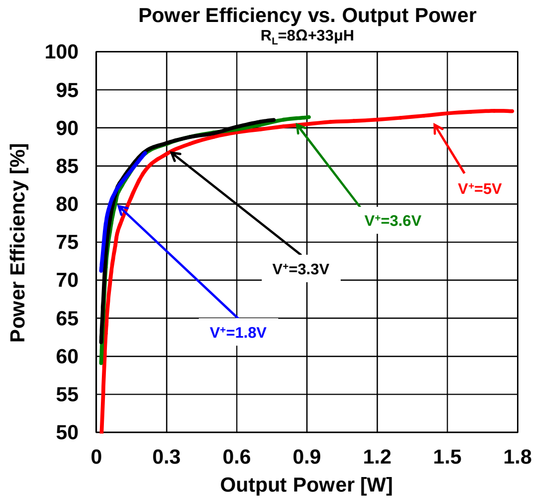
## ■ TYPICAL CHARACTERISTICS

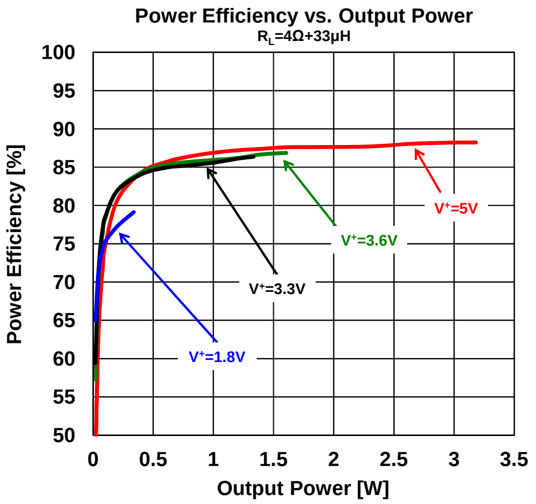


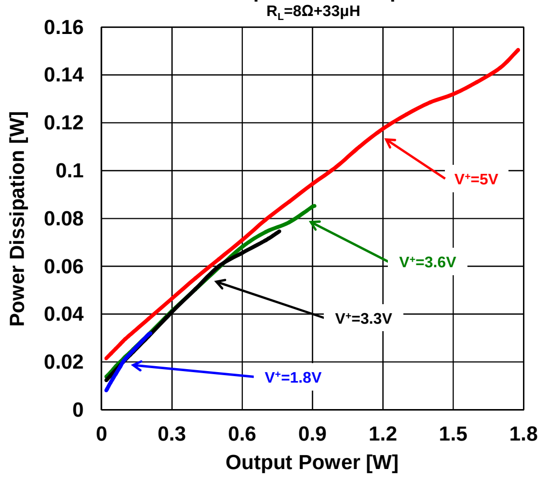



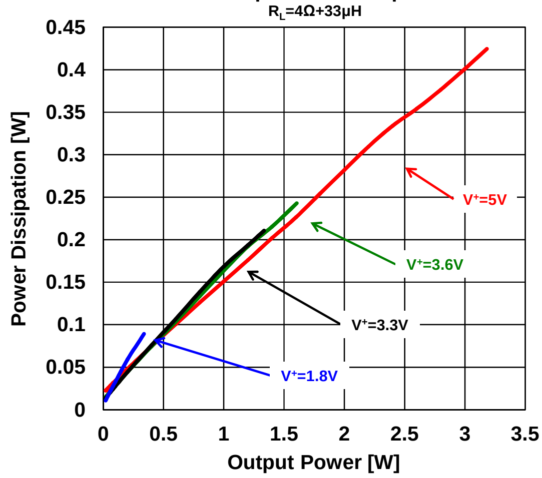



## ■ TYPICAL CHARACTERISTICS

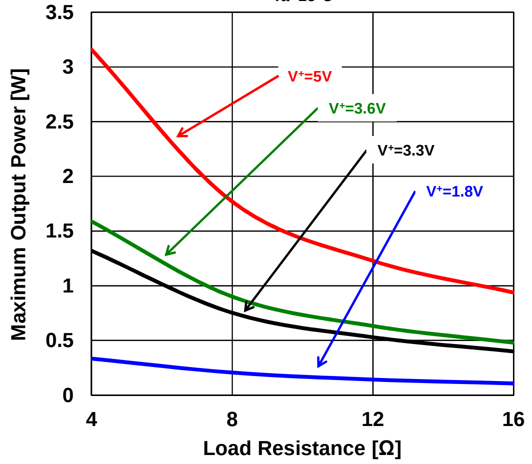
**Power Dissipation vs. Output Power**
$R_L$=8Ω+33μH



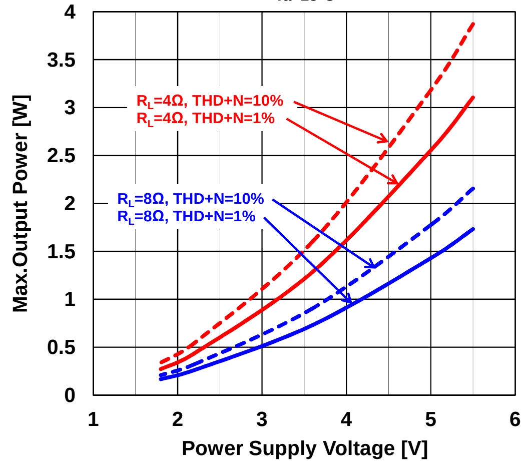

**Power Dissipation vs. Output Power**
$R_L$=4Ω+33μH



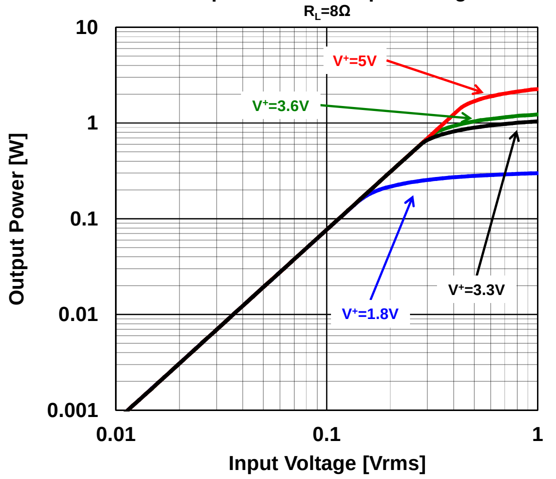

**Maximum Output Power vs. Load Resistance**
Ta=25°C



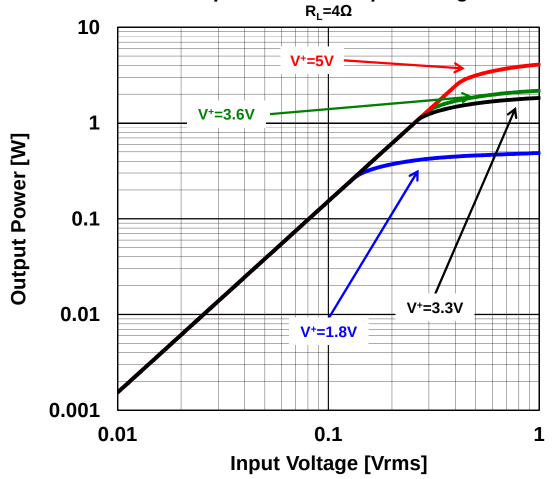

**MAX Output Power vs. Supply Voltage**
Ta=25°C




**Output Power vs. Input Voltage**
$R_L$=8Ω

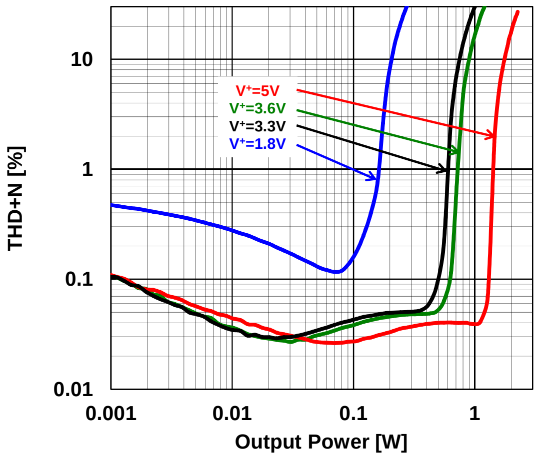



**Output Power vs. Input Voltage**
$R_L$=4Ω

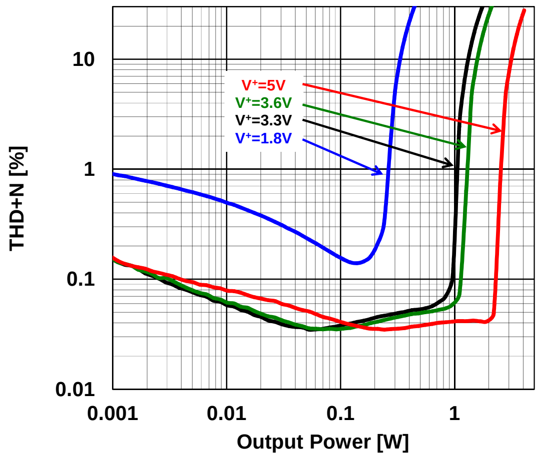


## ■ TYPICAL CHARACTERISTICS

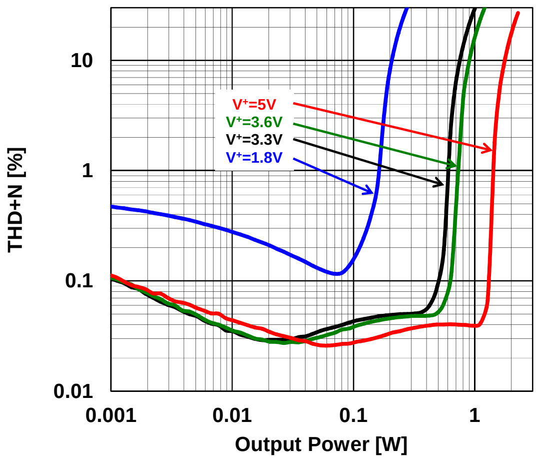
**THD+N vs. Output Power**
$R_L$=8Ω, Differential Input, Ta=25℃



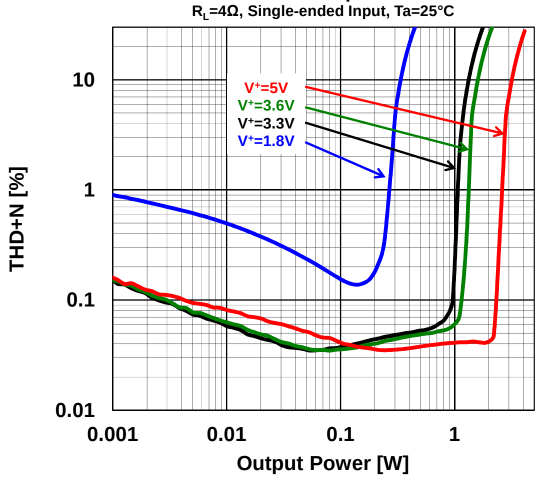

**THD+N vs. Output Power**
$R_L$=4Ω, Differential Input, Ta=25°C



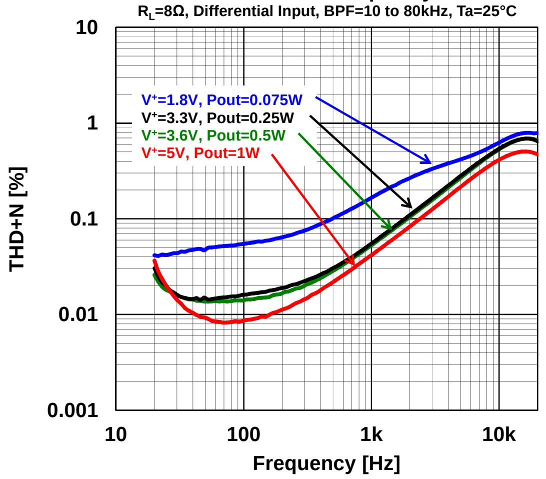

**THD+N vs. Output Power**
$R_L$=8Ω, Single-ended Input, Ta=25℃



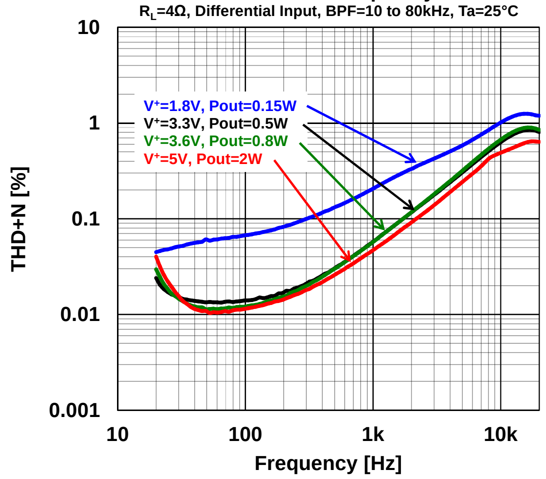

**THD+N vs. Output Power**
$R_L$=4Ω, Single-ended Input, Ta=25°C



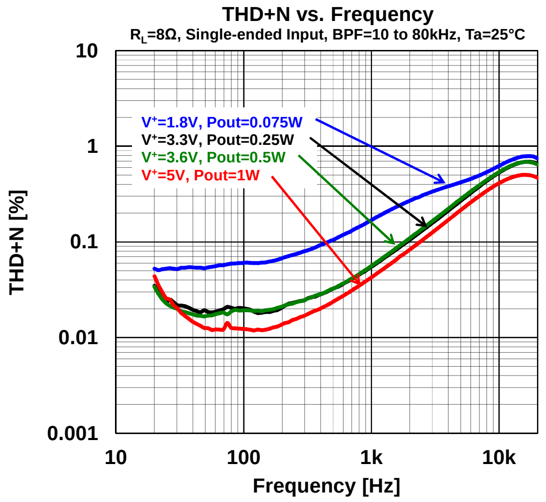

**THD+N vs. Frequency**
$R_L$=8Ω, Differential Input, BPF=10 to 80kHz, Ta=25°C

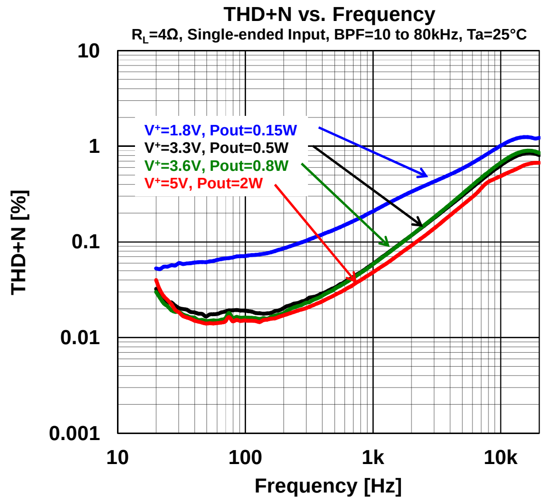


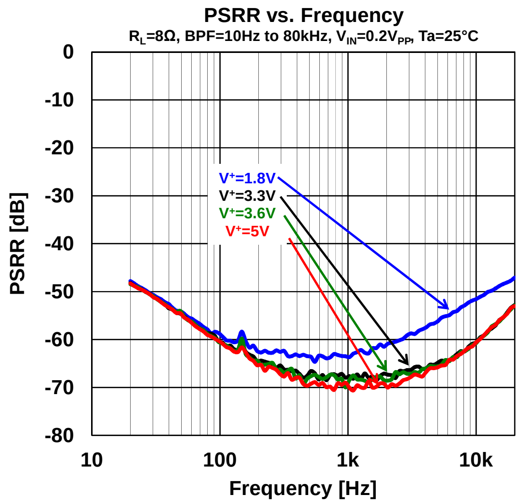

**THD+N vs. Frequency**
$R_L$=4Ω, Differential Input, BPF=10 to 80kHz, Ta=25°C

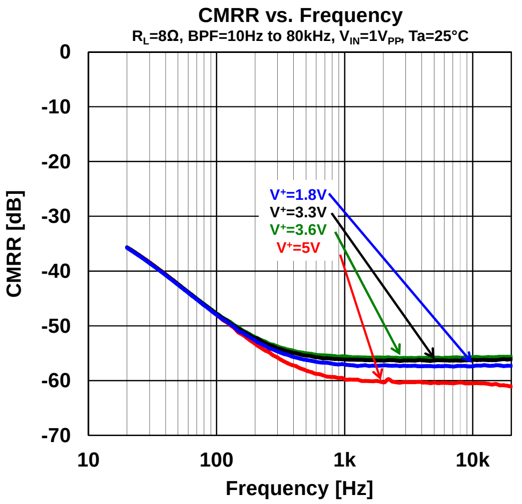


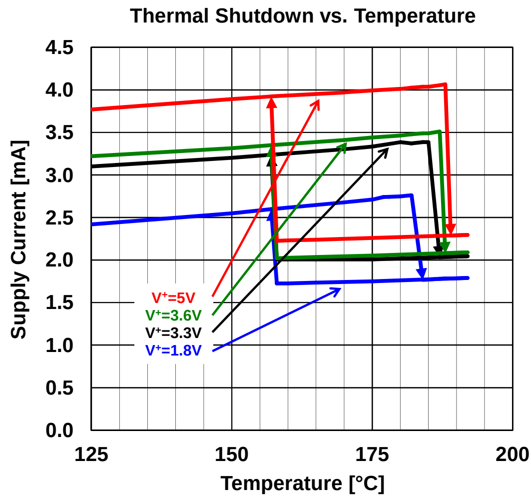
■ TYPICAL CHARACTERISTICS

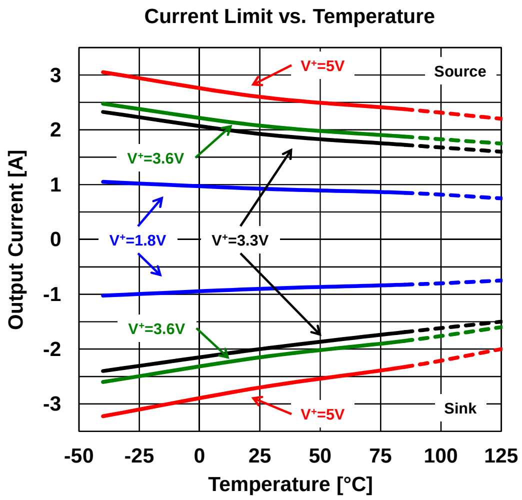


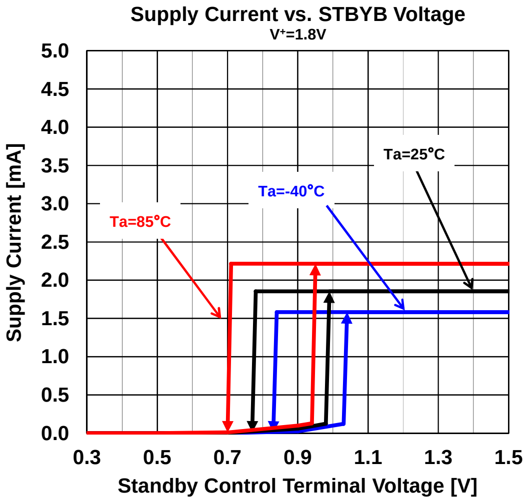



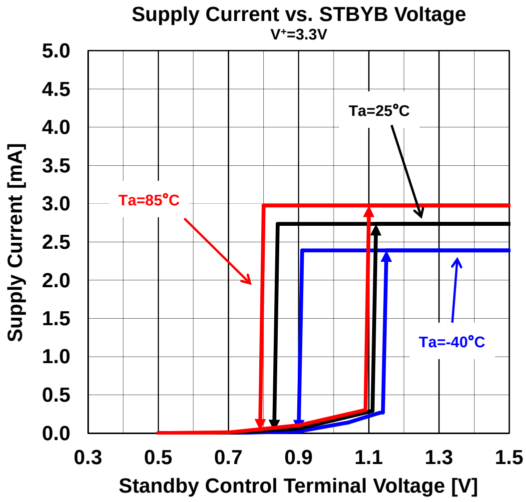



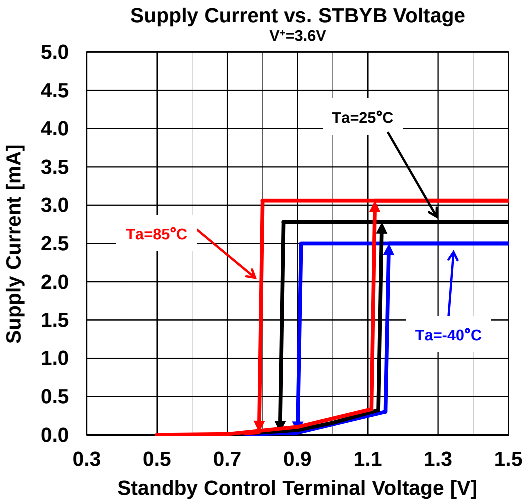



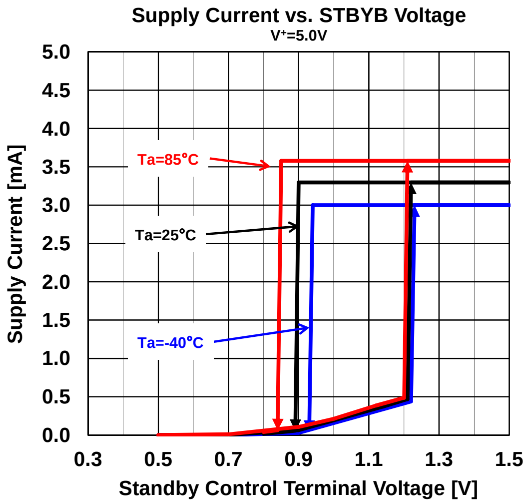



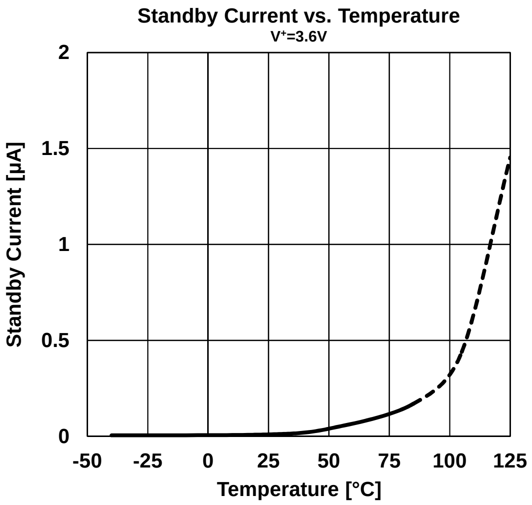
■ TYPICAL CHARACTERISTICS

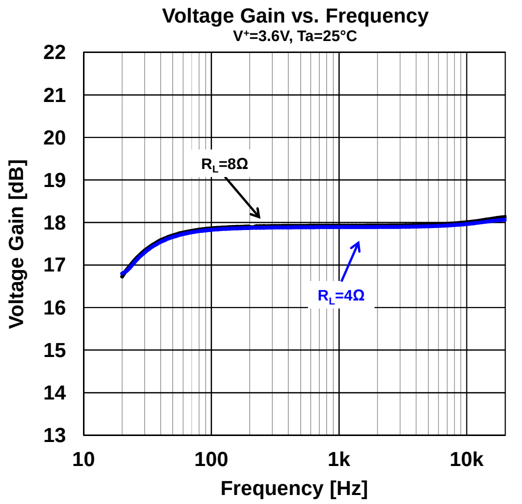


## ■ APPLICATION NOTE

The NJU8759 is an analog signal input monaural filterless class-D power amplifier. Operating voltage from 1.8V to 5.5V single supply can be used with 2-cell batteries. NJU8759 features Class-D operation with high output capability, is 1.7W output (8Ω load) and 3.0W output (4Ω load). The BTL output configuration can reduce the coupling capacitor. Furthermore, the output LC filterless architecture reduces external parts and PCB size.

### 1. OPERATING PRINCIPLE

Figure 1-1 shows the NJU8759 block diagram. The NJU8759 consists of a Class-D Amplifier, an Under Voltage Lockout, a Thermal Shut Down and Output Short Protections.

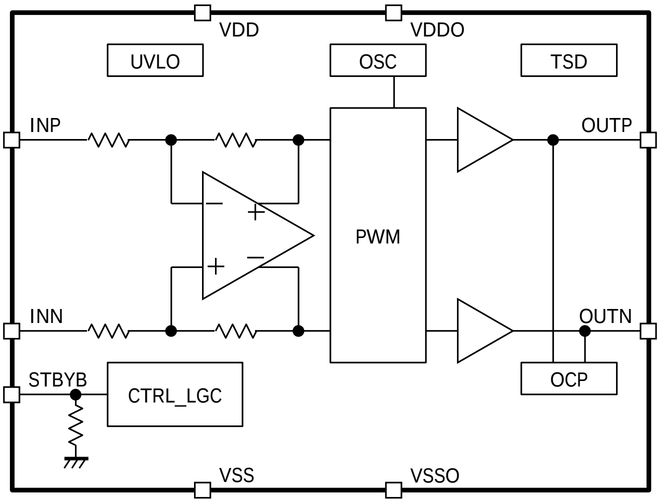



Figure 1-1 the NJU8759 block diagram

### 2. FUNCTIONAL DESCRIPTION

#### 2.1. Audio Signals

Differential analog signals are input into INP and INN as Figure 2-1 (a). The voltage gain is shown by

$$Av = \frac{V_{OUTP} - V_{OUTN}}{V_{INP} - V_{INN}} = 18dB$$

In case of a single-ended input signal application, an analog signal is input into INP as Figure 2-1 (b).

Some troubles may be caused by the input signal voltage over power supply voltage. So design the input signal voltage under 600mVrms. Also, same troubles may be caused in case of floating input pins. For preventing floating input pins, design former audio IC active mode before releasing NJU8759 stand-by mode, or connect 1 MΩ pull-down resistors shown as Figure 2-2.

PWM signals are output from OUTP and OUTN. Connect a dynamic speaker between OUTP and OUTN. The NJU8759 does not require OUTPUT LC filters which a traditional class-D amplifier needed. The output power is shown below.

$$P_{OUT} = \frac{[Av(V_{INP} - V_{INN})]^2}{R_L} \ [W]$$

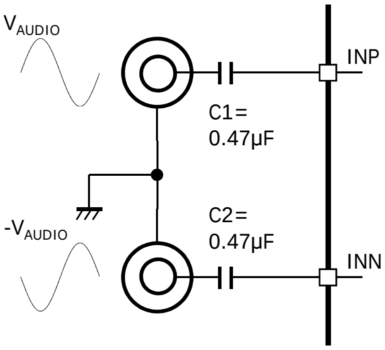
As mentioned below, the NJU8759 operates cancelling output offset voltage during turn-on and turn-off time. In case of an application that audio signals are input during turn-on and turn-off time, evaluate a pop-noise adequately.
The input capacitors and input resistors set a high-pass filter. Its corner frequency is given by

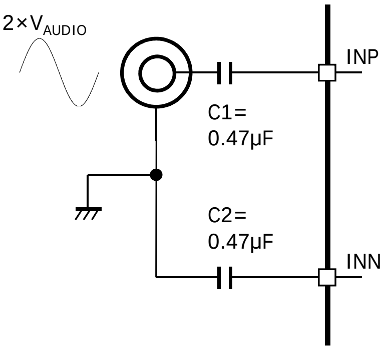
$$fc = \frac{1}{2\pi \times 30k\Omega(typ.) \times C1}$$

The recommended capacitor value is under 0.47μF.

■ APPLICATION NOTE

**2.1. Audio Signals (Continued)**




(a) a differential input signal application (b) a single-ended input signal application

Figure 2-1 How to input audio signals

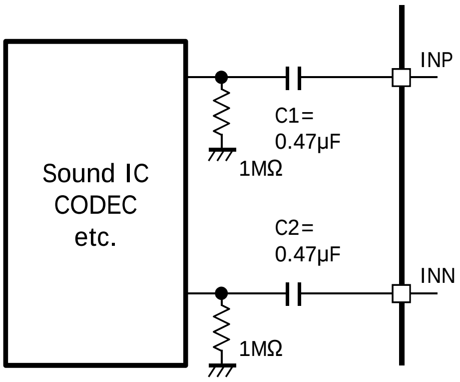



Figure 2-2 How to prevent floating input pins

**2.2. Thermal Design**

The output power is restricted by maximum rating.
Maximum package power dissipation at any ambient temperature is given by

$$P_{DMAX} = \frac{125[°C] - T_a[°C]}{\theta_{ja}[°C / W]}$$

Where $P_{DMAX}$: maximum power dissipation [W], $T_a$: ambient temperature [°C], $\theta_{ja}$: thermal resistance [°C/W]

The IC power dissipation referred to figure 2-3 is a difference between supply power and output power shown by

$$P_D = \left(V^+[V] \times I_{supply}[A]\right) - P_{OUT}[W]$$

Design so that the IC power dissipation $P_D$ does not exceed the maximum package power dissipation $P_{DMAX}$.
For the power dissipation and thermal resistance of each package, refer to the absolute maximum ratings and thermal resistance in the data sheet.

■ **APPLICATION NOTE**

**2.2. Thermal Design (Continued)**

Ex.) Ta=50°C, $V^+$=5V, $I_{SUPPLY}$=560mA、$P_{OUT}$=2.5W、WCSP9 package, 4-layer PCB

Power dissipation $P_D = (5[V] \times 560[mA]) - 2.5[W] = 300[mW]$

Maximum package power dissipation $P_{DMAX}$ at Ta=50°C

$$P_{DMAX} = \frac{125[°C] - 50[°C]}{83.4[°C/W]} = 900[mW]$$

The power dissipation $P_D$ is within the maximum package power dissipation $P_{DMAX}$.

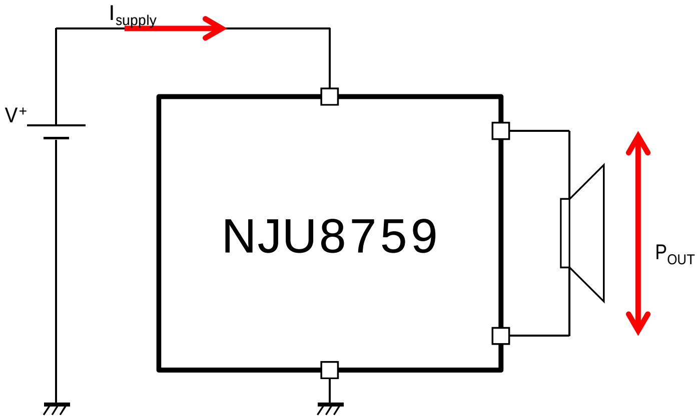



Figure 2-3 a power dissipation model

■ APPLICATION NOTE

**2.3. Stand-by Control**

Input the stand-by control signal into “STBYB” terminal with 100kΩ pull down resistor.
The NJU8759 operates if "STBYB" voltage over H level digital voltage is applied and after turn-on time (16ms typ.), an audio signal is output.
The NJU8759 shuts down if "STBYB" voltage under L level digital voltage is applied and after turn-off time (16ms typ.), it goes to the stand-by mode.

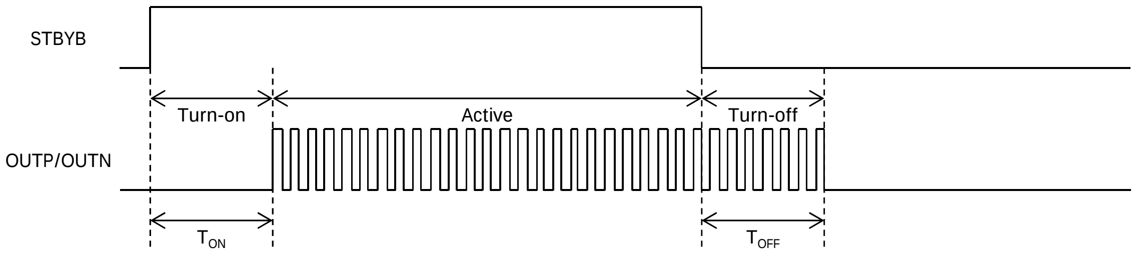



Figure 2-4Timing chart

**2.4. Under Voltage Lock Out**

When the power-supply voltage drops down under UVLO detecting voltage, OUTP and OUTN become high impedance. When the power-supply voltage increases to over UVLO detecting voltage summing hysteresis voltage, it restarts after the turn-on time.

**2.5. Short Protection**

The short-circuit protection circuit operates at the condition of the following.

-Short between OUTP and OUTN
- GND fault of OUTP terminal
- GND fault of OUTN terminal
- $V^+$ fault of OUTP terminal
- $V^+$ fault of OUTN terminal

When short-circuit protection circuit operates, the OUTP and OUTN become “high impedance”. It restarts by turn –on sequence.
The detectable current and the period for the protection depend on the power supply voltage and temperature. And the short protector is not effective for a long term short-circuit current but for an instantaneous accident.
Continuous high current may cause permanent damage to the NJU8759.

**2.6. Thermal Shut Downs**

When IC junction temperature is higher than detecting temperature, the OUTP and OUTN become high impedance. It restarts if IC junction temperature is lower than releasing temperature.

■ **APPLICATION NOTE**

**2.7. EMI Restriction**

If it is necessary to restrict EMI, design the short traces from the amplifier to the speaker. If you need more restriction, design the short traces with ferrite beads shown as Figure 2-5

Figure 2-6 is the measurement result on equivalent VCCI CLASS-B 3m with 100mm traces from the amplifier to the speaker.

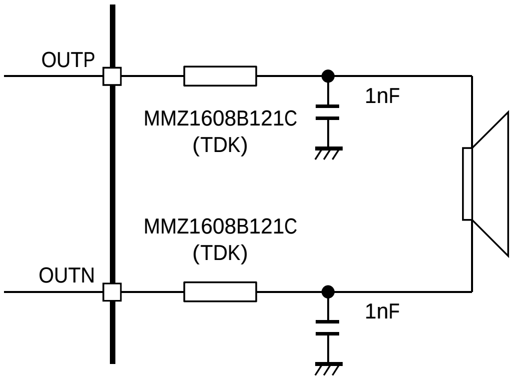
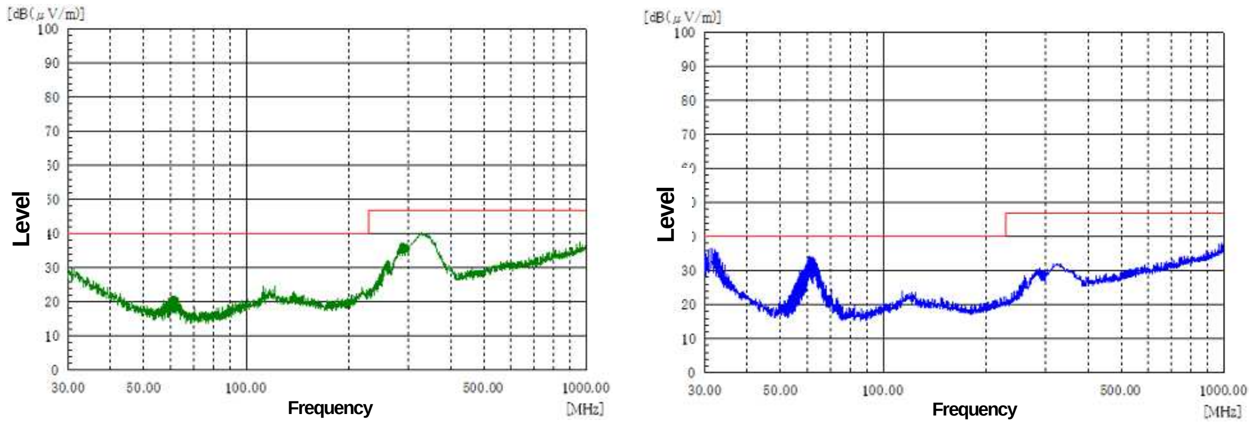



Figure 2-5 an EMI restriction model




(a) horizontal (b) vertical

Figure 2-6 EMI result on equivalent VCCI CLASS-B 3m

■ **APPLICATION NOTE**

**2.8. PCB Layout**

Figure 2-7 shows an example for 4-layer PCB Layout around the NJU8759.
For VDDO, VSSO, OUTP, and OUTN through which a large current flows, lay out with the maximum width allowed by the wiring rules. The power supply of NJU8759 must operate stably against the sink or source current that is generated by the audio signal and the output stage. Chip ceramic capacitors are recommended for bypass capacitors between $V^+$ and GND. It is recommended the 0.1μF capacitor sets near VDD, VDDO, VSS and VSSO pin for the restricting ripple.
If the standby control signal is noisy, the standby mode may not be controlled properly. In such cases, a capacitor of 1nF or more placed near the IC to eliminate then noise of standby control signal.

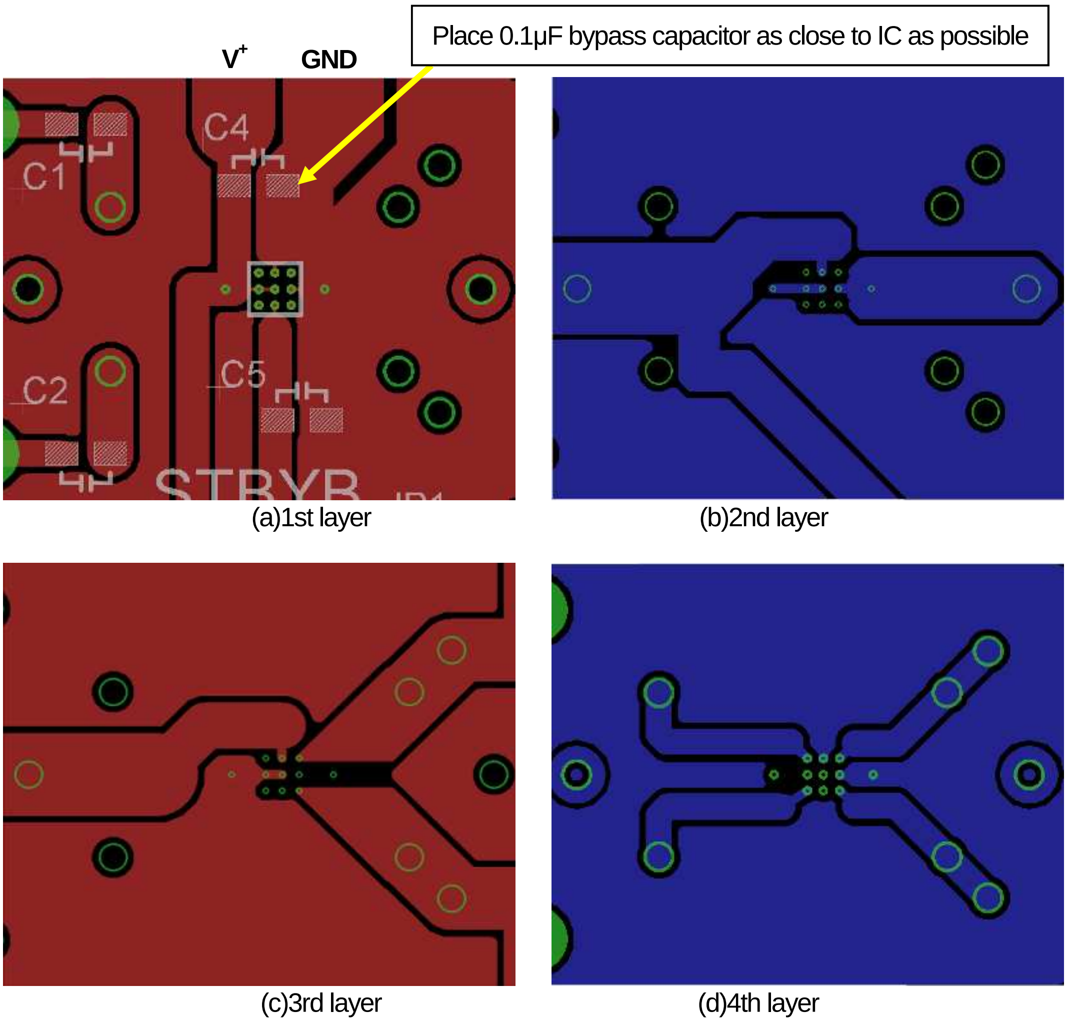
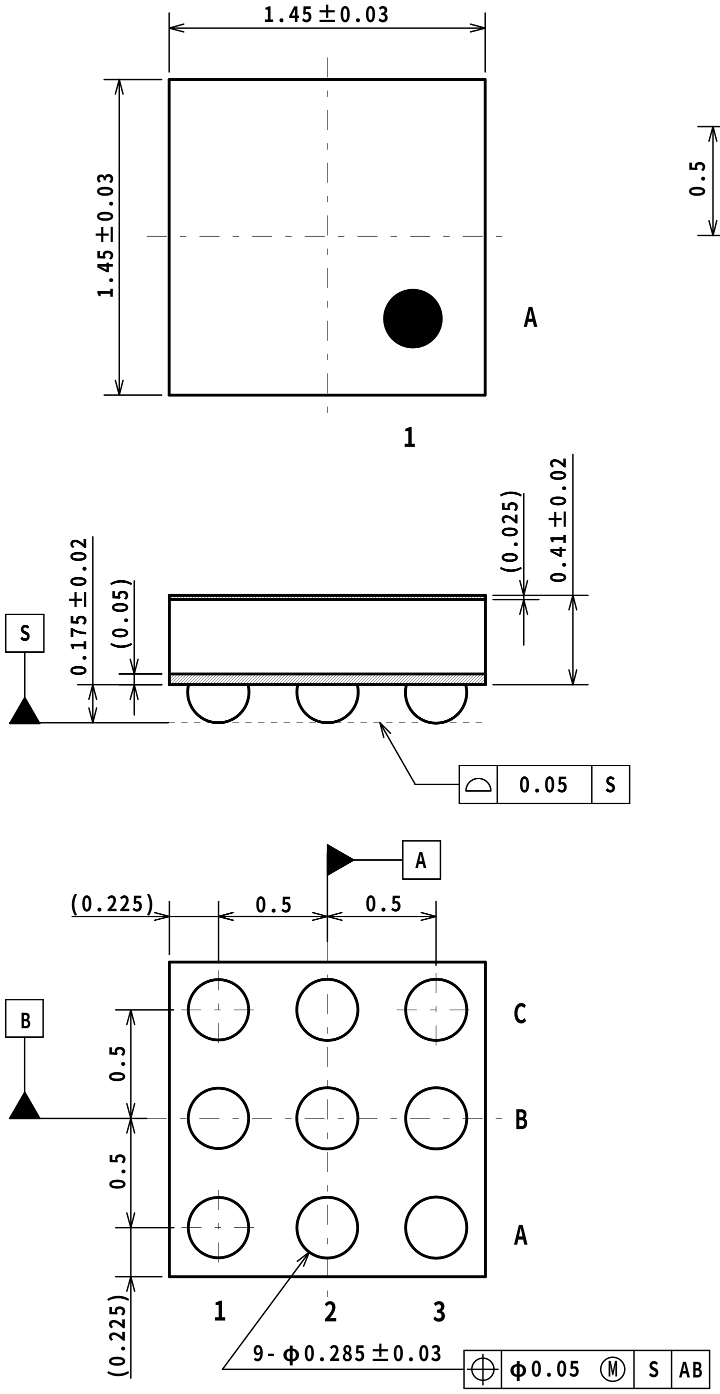



Figure 2-7 an example for 4 layer PCB Layout around the NJU8759

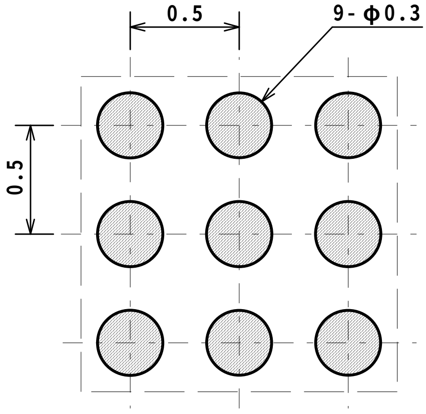
# WCSP9

Unit: mm

■ PACKAGE DIMENSIONS




■ EXAMPLE OF SOLDER PADS DIMENSIONS

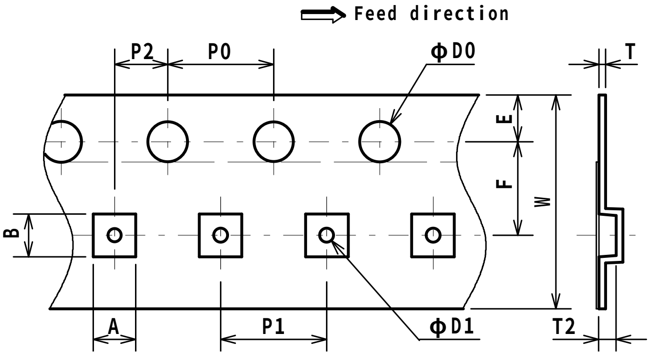


# WCSP9

## ■ PACKING SPEC

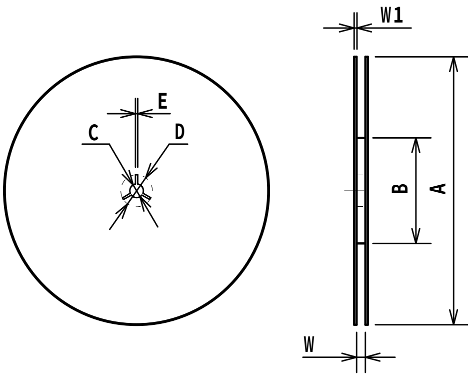
Unit: mm

### TAPING DIMENSIONS



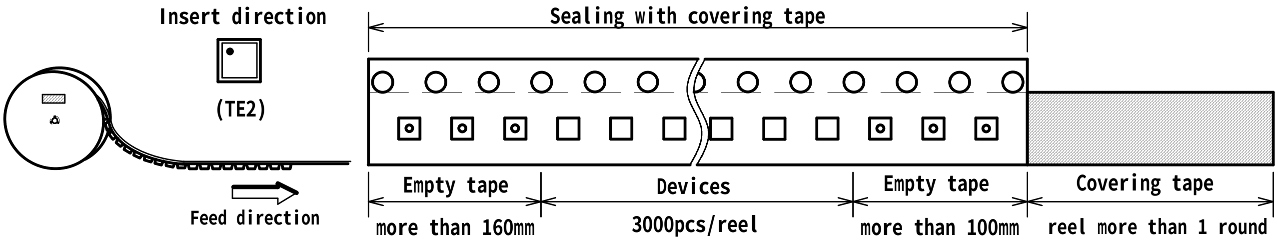

| SYMBOL | DIMENSION | REMARKS |
|---|---|---|
| A | 1.55±0.05 | BOTTOM DIMENSION |
| B | 1.55±0.05 | BOTTOM DIMENSION |
| D0 | 1.5 $^{+0.1}_{0}$ | |
| D1 | 0.5±0.1 | |
| E | 1.75±0.1 | |
| F | 3.5±0.05 | |
| P0 | 4.0±0.1 | |
| P1 | 4.0±0.1 | |
| P2 | 2.0±0.05 | |
| T | 0.25±0.05 | |
| T2 | 0.7±0.05 | |
| W | 8.0 $^{+0.3}_{-0.1}$ | |

### REEL DIMENSIONS

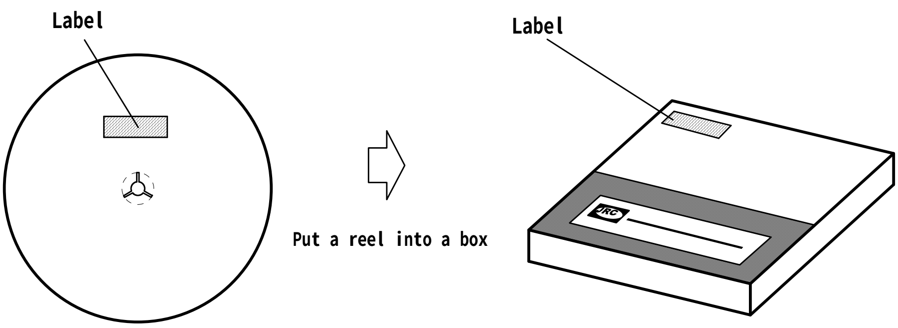



| SYMBOL | DIMENSION |
|---|---|
| A | φ180 $^{0}_{-1.5}$ |
| B | φ 60 $^{+1}_{0}$ |
| C | φ 13±0.2 |
| D | φ 21±0.8 |
| E | 2±0.5 |
| W | 9 $^{+1}_{0}$ |
| W1 | 1.2±0.2 |

### TAPING STATE

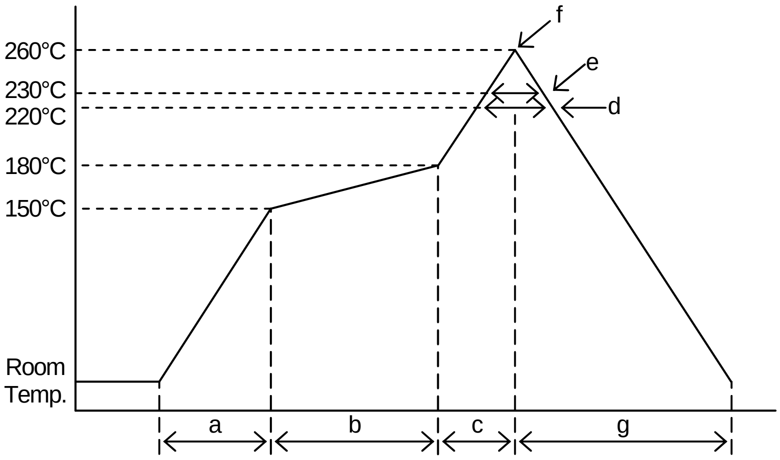



### PACKING STATE



## ■ RECOMMENDED MOUNTING METHOD

### INFRARED REFLOW SOLDERING PROFILE




| | | |
|---|---|---|
| a | Temperature ramping rate | 1 to 4°C/s |
| b | Pre-heating temperature<br>Pre-heating time | 150 to 180°C<br>60 to 120s |
| c | Temperature ramp rate | 1 to 4°C/s |
| d | 220°C or higher time | shorter than 60s |
| e | 230°C or higher time | shorter than 40s |
| f | Peak temperature | lower than 260°C |
| g | Temperature ramping rate | 1 to 6°C/s |

The temperature indicates at the surface of mold package.

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