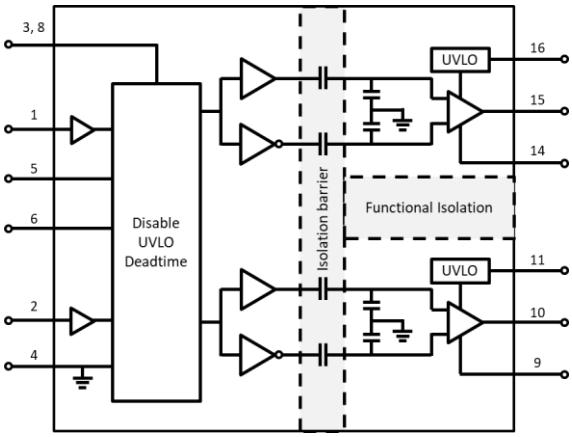
DATASHEET

Dual-Channel Isolated Gate Driver
CE21550X-G Series



Features:

- Compliance Halogens Free
  (Br < 900 ppm, Cl < 900 ppm, Br+Cl < 1500 ppm)
- 3V to 5.5V Input VCCI Range to Interface with Both Digital and Analog Controllers
- Up to 25V VDD Output Drive Supply
- Programmable Overlap and Dead Time
- Wide temperature range: -40°C to 125°C

Description

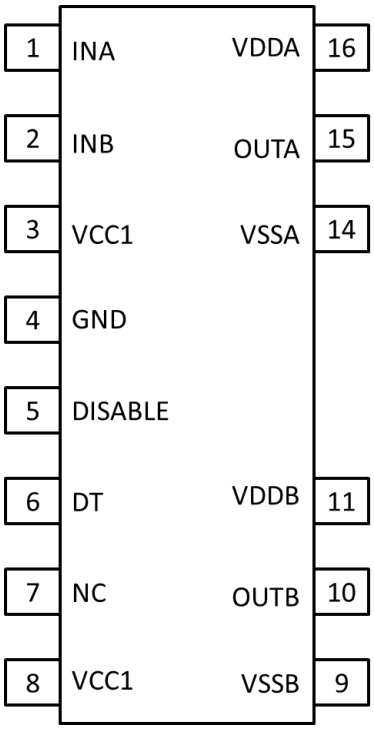
The CE21550X has a source peak current of 4A and a sink peak current of 8A. The maximum switching frequency can reach 5MHz. It is suitable for gate driver of MOSFET, IGBT and SiC MOSFET.

Every driver can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver with programmable dead time (DT). A DISABLE pin shuts down both outputs simultaneously when it is set high and allows normal operation when left open or grounded. As a fail-safe measure, primary-side logic failures force both outputs low.

Applications

- HEV and BEV Battery Chargers
- Isolated Converters in DC-DC and AC-DC Power Supplies
- Server, Telecom, IT, and Industrial Infrastructures
- Motor Drive and DC-AC Solar Inverters
- LED Lighting
- Inductive Heating
- Uninterruptible Power Supply (UPS)

Pin Description



0.1μF capacitor from VCC1 and GND.
1μF capacitor from VDDA and VDDB to VSSA and VSSB.

Pin	Symbol	Description
1	INA	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
2	INB	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
3,8	VCC1	Primary-side supply voltage.
4	GND	Primary-side ground reference.
5	DISABLE	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. If this pin is not used, it is recommended to ground this pin to obtain better noise immunity. When connecting to a microcontroller, use a low ESR/ESL capacitor of approximately 1nF to bypass the DIS pin.
6	DT	Programmable dead time function. Tying DT to VCCI allows the outputs to overlap. Leaving DT open sets, the dead time to <15 ns. Placing a 500Ω to 500kΩ resistor (RDT) between DT and GND adjusts dead time according to: DT(ns) ≈ 10 x RDT(kΩ).
7	NC	No connection.
9	VSSB	Ground for secondary-side driver B.
10	OUTB	Output of driver B.
11	VDDB	Secondary-side power for driver B.
14	VSSA	Ground for secondary-side driver A.
15	OUTA	Output of driver A.
16	VDDA	Secondary-side power for driver A.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC1}	7	V
Input signal voltage	V_{IN}	V_{CC1}+0.5	V
Driver bias supply	V_{DD}	30	V
Maximum Output Voltage	V_{OUT}	V_{DD}+0.5	V
Isolation Voltage *1	V_{ISO}	5000	V rms
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C
Soldering Temperature *2	T_{SOL}	260	°C

Notes:
*1 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1 to 8 are shorted together, and pins 9 to 16 are shorted together.
*2 For 10 seconds.
*3 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter		Symbol	Min	Max	Unit
Input Supply Voltage		V_{CC1}	3	5.5	V
Output Supply Voltage	CE21550A	V_{DD}	6.5	25	V
	CE21550B		9.2	25	V
Input voltage		V_{IN}	0	V_{CC1}	V
Output voltage		V_O	0	V_{DD}	V

Electro-Optical Characteristics

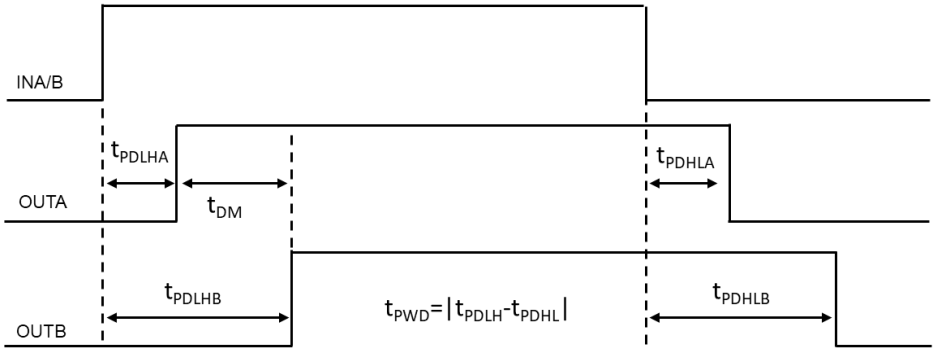
V_{CC1} = 3.3V or 5V, T_A=25°C, V_{DDA} = V_{DDB} = 12 V, unless otherwise noted.

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Quiescent Current	I_{VCCI}		0.5	1.1	mA	V_{INX} = 0V
	I_{VDDX}		0.9	1.5	mA	V_{INX} = 0V
Operating Current	I_{VCCI}		0.9		mA	V_{INX} f=500kHz, 50% duty cycle
	I_{VDDX}		2.2		mA	
UVLO Rising Threshold	V_{VCCI_ON}	2.55	2.7	2.85	V	
UVLO Falling threshold	V_{VCCI_OFF}	2.35	2.5	2.65	V	
Threshold hysteresis	V_{VCCI_HYS}		0.2		V	
UVLO Rising threshold	V_{VDDX_ON}	5.7	6.1	6.5	V	CE21550A
UVLO Falling threshold	V_{VDDX_OFF}	5.4	5.8	6.2	V	
UVLO Threshold hysteresis	V_{VDDX_HYS}		0.3		V	
UVLO Rising threshold	V_{VDDX_ON}	8.3	8.7	9.2	V	CE21550B
UVLO Falling threshold	V_{VDDX_OFF}	7.8	8.2	8.7	V	
UVLO Threshold hysteresis	V_{VDDX_HYS}		0.5		V	
Input high threshold voltage	V_{INX_H} V_{DIS_H}	1.6	1.8	2	V	
Input low threshold voltage	V_{INX_L} V_{DIS_L}	0.8	1	1.2	V	
Input threshold hysteresis	V_{INX_HYS} V_{DIS_HYS}		0.8		V	
Peak output source current	I_{O+}		4		A	C_{VDD} = 10µF, C_{LOAD} = 0.68µF, f = 100Hz, bench measurement
Peak output sink current	I_{O-}		8		A	
Output resistance at high state	R_{OH}		1		Ω	I_{OUT} = -10 mA
Output resistance at low state	R_{OL}		0.4		Ω	I_{OUT} = 10 mA
Output voltage at high state	V_{OH}		11.99		V	V_{DDX} = 12 V, I_{OUT} = -10 mA
Output voltage at low state	V_{OL}		4		mV	V_{DDX} = 12 V, I_{OUT} = 10 mA
Dead time	DT	Overlap determined by INA INB			ns	Pull DT pin to VCCI
		0	8	15	ns	DT pin is left open
		150	200	250	ns	R_{DT} = 20 KΩ

V_{CC1} = 3.3V or 5V, T_A=25°C, V_{DDA} = V_{DDB} = 12 V, unless otherwise noted.

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Output rise time	t_r		7	18	ns	C_{OUT} = 1.8nF
Output fall time	t_f		8	12	ns	C_{OUT} = 1.8nF
Minimum pulse width	t_{PWmin}		10	20	ns	Output off for less than minimum, C_{OUT} = 0pF
Propagation delay Low to High	t_{PDHL}	14	19	30	ns	
Propagation delay High to Low	t_{PDLH}	14	19	30	ns	
Pulse width distortion	t_{PWD}			5	ns	
Propagation delays matching between V_{OUTA}, V_{OUTB}	t_{DM}			5	ns	f = 100kHz
High-level common-mode transient immunity	$\|CM_H\|$		100		kV/us	V_{CM}=1000V;
Low-level common-mode transient immunity	$\|CM_L\|$		100		kV/us	V_{CM}=1000V;

Fig. 1 Overlapping inputs, Dead Time Disable



shows how to calculate pulse width distortion(t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase and disabling the dead time function by shorting the DT Pin to V_{CC1}.

Fig.2 Rising and Falling Time

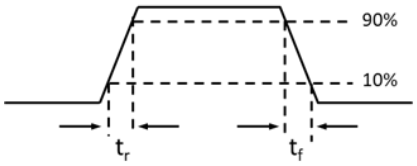
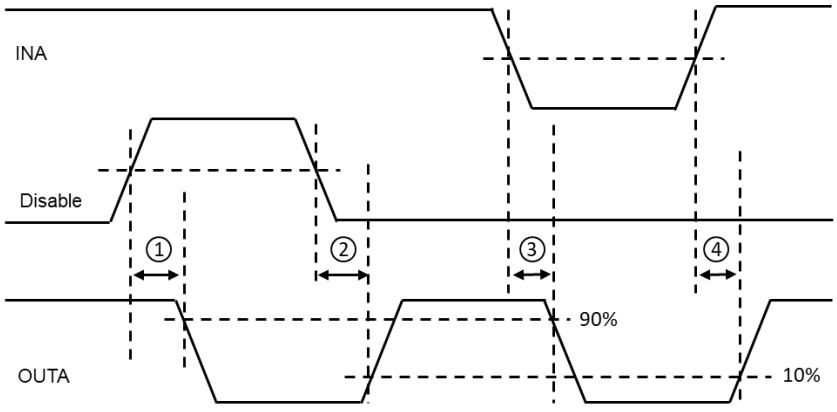
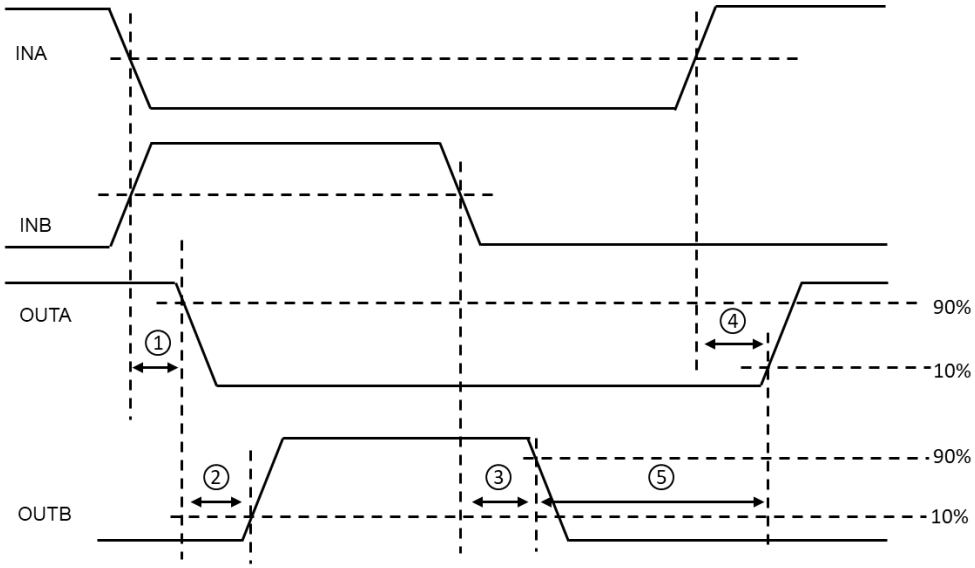


Fig.3 Input and Disable Response Time



① Disable High Response Time ③ t_{PDHL}
② Disable Low Response Time ④ t_{PDLH}

Fig.4 Programmable Dead Time



① t_{PDHL} ② Dead Time (set by R_{DT})
③ t_{PDHL} ④ t_{PDLH}
⑤ Dead Time(Determined by Input signals if longer than DT set by R_{DT})

Leaving the DT pin open or tying it to GND through an appropriate resistor (RDT) sets a dead-time interval.

Order Information

Part Number

CE21550X(TA)-G

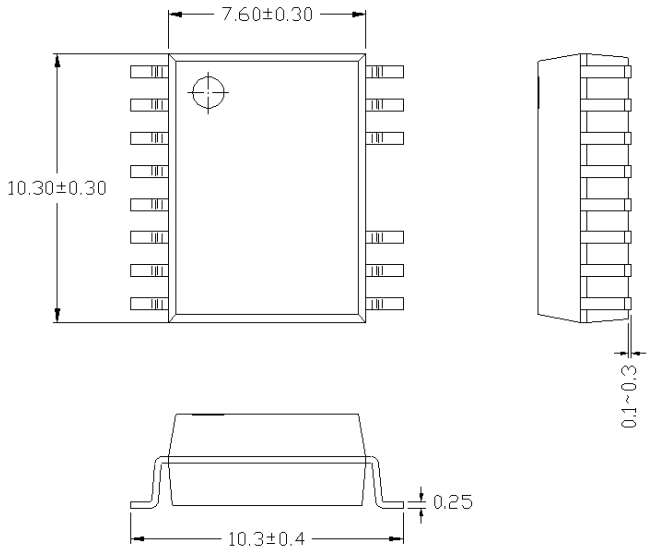
Note

CE	=	denotes EVERLIGHT
21550	=	part no.
X	=	VDD Supply Min. A: 6.5V B: 9.2V
G	=	Halogens free

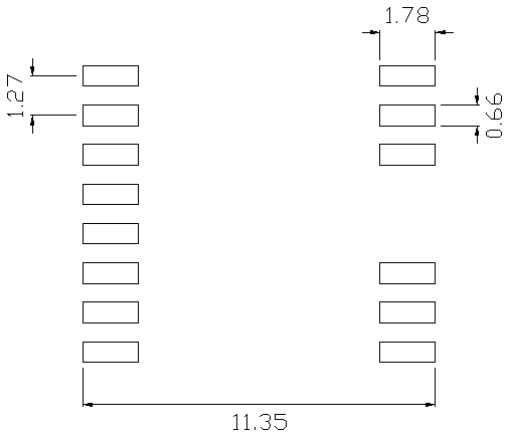
Option	Description	Packing quantity
(TA)	Surface mount lead form + TA tape & reel option	1500 units per reel

Package Dimension

(Dimensions in mm)

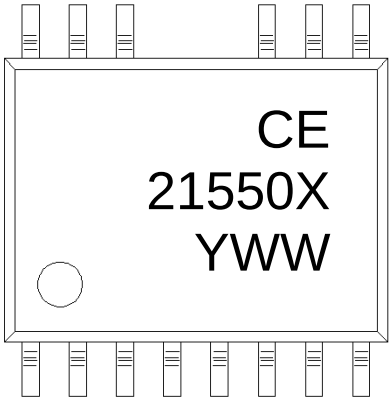


Recommended pad layout for surface mount leadform



Notes.
Suggested pad dimension is just for reference only.
Please modify the pad dimension based on individual need.

Device Marking



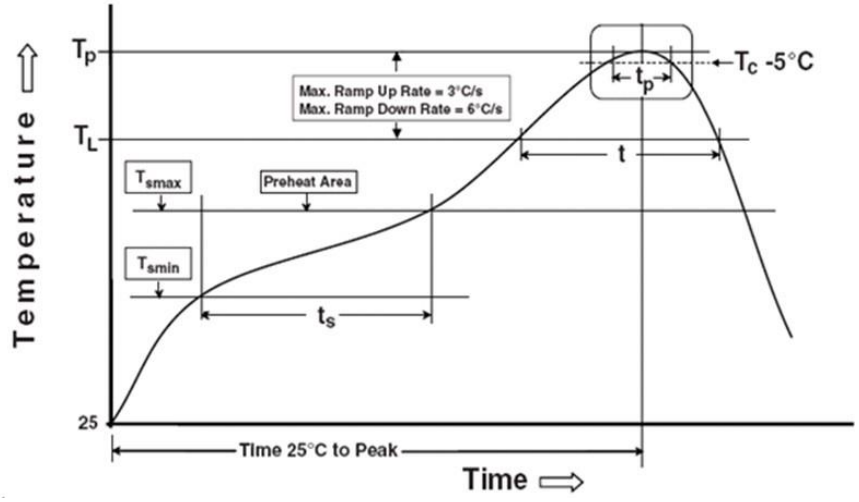
Notes

CE	denotes EVERLIGHT
21550X	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note: Reference: IPC/JEDEC J-STD-020D

Preheat	
Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max
Other	
Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_P)	260°C
Time within 5 °C of Actual Peak Temperature: T_P -5°C	30 s
Ramp- Down Rate from Peak Temperature	6°C /second max.
Time 25°C to peak temperature	8 minutes max.
Reflow times	3 times

DISCLAIMER

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
2. The graphs shown in this datasheet are representing typical data only and do not show guaranteed values.
3. When using this product, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
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