



# HT32F67593 Datasheet

**32-Bit Arm® Cortex®-M0+ Bluetooth® LE Microcontroller,  
1024 KB Flash, 128 KB SRAM and 192 KB ROM with BLEC,  
DMAC, STIM, GPTM, WDT, RTC, SPI, UART, I<sup>2</sup>C,  
SCI, IrDA, I<sup>2</sup>S, PCM, AES128, TRNG, QEI, ADC, TSEN**

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# 1 General Description

The Holtek HT32F67593 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core which runs the Bluetooth® LE (BLE) protocol stack and applications. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 64 MHz with a Flash accelerator to obtain maximum efficiency. It provides 1024 KB encryptable in-system Flash memory with 16 KB cache controller for code/data storage, 128 KB of embedded SRAM memory for system operation and application program usage and 192 KB of embedded ROM memory for preprogrammed embedded RTX-RTOS kernel, driver library, and BLE lower layer protocol stack software. A variety of peripherals, such as BLEC, DMAC, STIM, GPTM, WDT, RTC, SPI, UART, I<sup>2</sup>C, SCI, IrDA, I<sup>2</sup>S, PCM, AES128, TRNG, QEI, ADC, TSEN and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wake-up latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of BLE products such as handheld products, health care products, home appliances, smart device information beacons, data loggers, human interface device service, etc.

**arm** CORTEX

# 2 Features

## Processor

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 64 MHz operating frequency
- 0.93 DMIPS/MHz
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 40-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O port, hardware multiplier and low latency interrupt respond time.

## On-Chip Memory

- 1024 KB in-system Flash memory with 16 KB cache controller for code/data and options storage
- 128 KB of embedded SRAM memory for system operation and application program usage
- 192 KB of embedded ROM memory for preprogrammed embedded RTX-RTOS kernel, driver library, and BLEC lower layer protocol stack software

The in-system Flash memory provides non-volatile storage for code and data.

The ROM provides preprogrammed embedded RTX-RTOS kernel, driver library, and BLEC lower layer protocol stack software. It also contains a boot loader that can be used to reprogram the device using SPI or UART. Since ROM contains BLE host and controller software libraries, leaving more of the Flash memory available for the customer applications.

A 128K Bytes SRAM used for both store the Cortex®-M0+ code. It is split into 4 × 32K Bytes blocks, each block should be enabled or disabled individually by software to minimize power consumption when system in low power mode. In additional it contains a 16K bytes Flash cache. When it is not used, the cache can be used as a general-purpose SRAM.

## Debug Support

- Serial Wire Debug Port -SW-DP
- Supports over-the-air (OTA) upgrade

## Bluetooth Low Energy Controller – BLEC

- 2.4 GHz RF transceiver compatible with Bluetooth Low Energy (BLE) 5.3 specification
- Operating clock 16 MHz
- Low power modes supporting 32.768 kHz
- Four operating modes: Active, Sleep, Deep-Sleep and Hibernation
- GFSK modulation

- Supports LE 1 Mbps, 2 Mbps and coded 500 Kbps, 125 Kbps for long-range
- Receiver supports programmable gain control of over 70 dB
- Excellent receiver sensitivity of -94 dBm @ 1 Mbps
- Programmable transmitter output power up to +10 dBm
- All device classes support: Broadcaster, Central, Observer, Peripheral
- Simultaneous Master and Slave operation
- All packet types: Advertising, Data, Control
- Encryption: AES, CCM
- Bit stream processing: CRC, Whitening

The BLE core is a qualified Bluetooth baseband controller compatible with the Bluetooth Smart specification and it is in charge of packet encoding/decoding and frame scheduling. It performs Link Layer Control management supporting the main BLE states, including advertising and connection.

## Reset Control Unit – RSTCU

- System Resets
  - Power On Reset – POR
  - Brown Out Detector – BOD
  - Low Voltage Detector – LVD
- Watchdog Time-out reset
- Software-initiate reset of digital peripherals

There are several sources of reset, some are triggered due to errors or unexpected behavior, while others are user initiated.

## Clock Control Unit – CKCU

- External 16 MHz crystal ( $\pm 20$  ppm)
- External 32.768 kHz crystal ( $\pm 50$  ppm)
- Internal 16 MHz RC oscillator
- Internal 48 MHz RC oscillator
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The CKCU support two external and three internal clock sources. A 16 MHz crystal is required as the frequency for the radio. This signal is doubled internally to create a 64 MHz clock by PLL. Bluetooth low energy requires a slow-speed clock with better than  $\pm 50$  ppm accuracy if the device is to enter any low power mode while maintaining a connection. The internal 32 kHz RC oscillator can in some use cases be compensated to meet the requirement. The low-speed crystal oscillator is designed for use with a 32.768 kHz crystal. The internal high speed PLL (64 MHz) can be used as a clock source for the processor, Arm® Cortex®-M0+ system. The 32 kHz clock source can be used as external clocking referenced through GPIO.

## Power Management Control Unit – PMU

- Single  $V_{CC}$  power supply: 1.8 V to 3.6 V
- On-Chip internal SISO DC/DC
- To minimize power consumption, PMU supports a number of software configurable power mode and power management features.

Power Mode Function Block	Active (ACT)	Sleep (SLP)	Deep-Sleep (DSLDP)	Hibernation (HIB)
CPU	Active	Off	Off	Off
Flash	On	Available	Off	Off
SRAM	On	On	Off	Off
RADIO	On	On	Off	Off
SRAM Retention	Full	Partial	No	No
16M RC / Crystal	On	Off	Off	Off
32K RC / Crystal	On	On	On	Off
Peripheral	Available	Available	Off	Off
Wake up on RTC	Available	Available	Available	Off
Wake up on GPIO	Available	Available	Available	Available

In the Active mode, the application Cortex®-M0+ CPU is actively executing code. The Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source.

In the Sleep mode, all active peripherals can be clocked. But the application CPU core and memory are not clocked, and no code is executed. Any interrupt event will bring the processor back into active mode.

In the Deep-Sleep mode, only the always-on domain is active. An external wake-up event RTC event is required to bring the device back to active mode.

In the Hibernation mode, the device is turned off entirely, including the always-on domain. The I/O are latched with the value they had before entering hibernation mode. A change of state on any I/O pin defined as a wake-up from hibernation pin wakes up the device and functions as a reset trigger.

## DMA Controller – DMAC

- Supports memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral transmission
- Supports UART, SPI, I<sup>2</sup>C, SCI, I<sup>2</sup>S, ADC, GPTM
- 8 independent DMA channels
- Configurable 2 level priority
- Independent source and destination transfer size (8-bit, 16-bit, 32-bit)
- Supports circular mode
- Up to 65535 programmable number of data to be transferred
- Source and destination address increment or no increment

The DMA controller provides a way to offload data transfer tasks from the CPU, allowing for more efficient use of the processor and the available bus bandwidth. The DMA controller can perform transfers between memory and peripherals. The controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

## I/O Ports – GPIO

- Up to 16 GPIOs
- Programmable driver strength up to 13 mA
- Fully flexible digital pin multiplexing allows use as GPIO or any of several peripherals functions
- Pin state can be retained during all sleep modes
- Pins configured as digital inputs are Schmitt-triggered
- Programmable control for GPIO pad configuration
  - Weak pull-up or pull-down resistors
  - Digital input enables
- Programmable control for interrupts
  - POR Interrupt generation masking per pin
  - Edge-triggered on rising or falling

There are up to 16 general purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports can be multiplexed to any digital peripheral through the I/O controller which has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

## System Tick Timer – STT

- 40-bit compare match count-up counter – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restarts counter after a match condition

There is a system tick timer (STT), which provides a 40-bit incrementing wrap-on-zero counter with a flexible control mechanism. The system tick timer can be used in several different ways.

## System Timer – STIM

- Supports a low-speed 32 kHz clock as its clock source
- Supports a 32-bit counter and a 12-bit prescaler
- Supports 3 types of interrupt and wake-up: overflow, compare and tick
- Supports 4-channel compare interrupt and sleep wake-up
- Supports CPU interrupts and PMU wake-up interrupts independently
- Supports configuration success flag checking

The device has a 32-bit System Timers (STIM). This timer has a 4-channel compare register. The STIM operates in the low speed clock domain and can remain operating in the Sleep Mode. The STIM introduces a flexible clock scheme that delivers the required functionality and performance while minimizing power consumption.

Note: The STIM peripherals rely on a low-frequency clock source to provide its clock. Using a clock source with a stable frequency can achieve better clock accuracy.

## General-Purpose Timer – GPTM

- 16-bit or 32-bit operating modes
  - 16-bit or 32-bit programmable one-shot timer
  - 16-bit or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with a 4-bit prescaler
  - 16-bit input-edge count or time-capture mode with 4-bit prescaler
  - 16-bit PWM mode with 4-bit prescaler and software configurable output inversion
- Count Mode
  - Count Up Mode
  - Continue Count Up Mode
  - Count Up-Down Mode
  - Continue Up-Down Mode
- Three 32-bit counter or up to Six 16-bit counters
- Up to six PWM pins
- Efficient transfers using the DMA controller
- One 32-bit Timer supports IR output to specific pin
- Capture Mode
- IR decode function with capture mode

The general-purpose timers can be used to count or time external events that drive the timer-input pins. Each 16 or 32-bit GPTM block provides two 16-bit timers or counters that can be configured to operate independently as timers or event counters or configured to operate as on 32-bit timer.

## Watchdog Timer – WDT

- 32-bit counter up with 30.52  $\mu$ s step for a maximum 36.41 hr time-out
- Non-Maskable Interrupt (NMI) or WDT reset
- NMI interrupt can be selected masked 16  $\times$  30.52  $\mu$ s ahead before WDT reset

The watchdog timer is used to regain control when system fails because of a software error, or an external device failed to respond properly.

There is a dependent watchdog timer, which can generate a reset when a predefined timer-out value is reached. The internal 32K RC oscillator provides the clock source for this watchdog timer.

## Real Time Clock – RTC

- 40-bit incrementing counter with support for programmable increment to support ppm-adjustment
- Four match registers supporting the generation of events
- Software and hardware reset of events

The Real Time Clock implements a second and sub-second counter with support for soft-compensation for ppm-offsets, with four match registers.

## Serial Peripheral Interface – SPI

- SPI clock frequency up to 16 MHz and programmable output frequencies in master mode
- 8 bytes transmit and receive FIFO
- SPI mode 0, 1, 2, 3 support (clock edge and phase)
- Supports both master and slave modes
- Supports Multi-master and multi-slave operation
- Supports RX timeout interrupt
- Programmable TX only / RX only / TRX mode
- Programmable SPI\_DO idle byte

This interface supports a subset of the Serial Peripheral Interface SPI. The serial interface can transmit and receive 8, 16, 32 bits or as long as data in master/slave mode. Data is written from a master (CPU/DMA) over the APB bus to the SPI.

## Universal Asynchronous Receiver Transmitter – UART

- Programmable serial data baud rate
- Hardware flow control support (CTS/RTS)
- Functionality based on the 16550 industry standard
- Programmable character properties, such as number of data bits per character (5~8), optional
- Parity bit (with odd/even/stick/no select) and number of stop bits (1, 1.5 or 2)
- 8 bytes transmit and receive FIFOs
- Supports line break generation and detection
- Supports RX timeout interrupt

The UART is compliant to the industry-standard 16550 and is used for serial communication with a peripheral data set. Data is written from a master (CPU/DMA) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU/DMA) to read back. Both UARTs support hardware flow control signals (RTS, CTS).

## Inter-Integrated Circuit – I<sup>2</sup>C

- Two-wire I<sup>2</sup>C serial interface consists of a serial data line (SDA) and a serial clock (SCL)
- Supports two speed modes:
  - Standard mode: 0 ~ 100K bit/s
  - Fast mode: ≤ 400K bit/s
- Supports 8 bytes transmit/receive FIFOs
- Configurable master or slave, transmit/receive operation
- Supports 7-bit or 10-bit addressing mode
- Supports configurable slave address and target address
- Interrupt operation

The I<sup>2</sup>C interface is a programmable control bus that provides support for the communications link between Integrated Circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D and D/A converters.

## Smart Card Interface – SCI

- Supports the asynchronous protocols T=0 in accordance with ISO7816-3
- Flexible output clock 1/2/4 MHz
- Error management at character level for T=0 that parity error counter in reception mode and in transmission mode with auto-repetition
- 32-bit counting by ETU clock for time-out counter
- Power-down mode for reducing current consumption when no activity

The smart card interface is compatible with the ISO7816-3 and EMV 4.2 related standards. As a master device, it can transmit data controlled by CPU/DMA to destination card, and also it can receive data stored in SRAM.

## Inter-IC Sound – I<sup>2</sup>S

- Master and Slave modes
- I<sup>2</sup>S-justified, Left-justified and DSP (PCM A&B) formats
- 16-bit, 20-bit, 24-bit operation
- Programmable MCLK output: 16/8/4/2 MHz
- Programmable sample rate  $f_s$ : 8/16/32 kHz

The I<sup>2</sup>S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADC or DACs.

## Cryptography

### Advanced Encryption Standard – AES128

- Supports AES Encrypt / Decrypt functions
- Supports AES ECB/CBC/CTR modes
- Supports Key Size of 128 bits
- Supports 4 words Initial Vector for CBC and CTR modes
- 4 × 32-bit AES data buffer
- DMA support
- Supports Word Data Swap function

The AES core supports both encryption and decryption functions and supports 128-bit input data. It should be noted that hardware does not pad out any input data bits, therefore users need to do pad action by software at first.

## True Random Number Generator – TRNG

- TRNG used to provide the seed for encryption processes, its output can be used as entropy input for a Crypto engine

The crypto engine could work in bypass mode and aims to accelerate the algorithm calculations that are needed in order to implement the AES and CBC crypto.

## Security

- Supports 32-bit Unique ID for each chip
- Supports automatic hardware decoding

The security module used to protect the code saved in the Flash memory, it supports encrypted storage of code for each chip. A 32-bit unique ID is used as the encryption key and each chip can perform the same function but store different code. The user can also use the security module to encrypt the BOOT program.

## Quadrature Encoder Interface – QEI

- Supports 2-channel incremental encode

A quadrature encoder, also known as a 2-channel incremental encoder, converts linear displacement into a pulse signal. By monitoring both the number of pulses and the relative phase of the two signals, you can track the position, direction of rotation, and speed. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface (QEI) interprets the code produced by a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture a running estimate of the velocity of the encoder wheel.

## Analog to Digital Converter – ADC

- 12-bit dynamic SAR ADC engine
- Conversion time and dynamic range can be changed
  - 12-bit dynamic with 1 Msps for audio application
  - 10-bit dynamic with 16 Msps for general application
- Up to 5 single-ended channels
- One channel for  $V_{CC}$  monitoring
- DMA support

The low power general purpose 12-bit ADC has up to 5 channels and operates in the single ended mode.

## Temperature Sensor – TSEN

- Detection range:  $-40\text{ }^{\circ}\text{C} \sim 125\text{ }^{\circ}\text{C}$
- Accuracy:  $\pm 8\text{ }^{\circ}\text{C}$
- Resolution:  $0.3\text{ }^{\circ}\text{C}$

A BJT based temperature sensor is integrated, which can be used for performance tuning over temperatures. The sensed voltage is converted to 12-bit digital code by general purpose ADC. Accuracy compensation could be implemented by customer if required.

## Package and Operation Temperature

- 28-pin LGA package
- Operation temperature range: -40 °C to 85 °C

# 3 Overview

## Device Information

**Table 1. Features and Peripheral List**

Peripherals		HT32F67593
In-System Flash (KB)		1024
ROM (KB)		192
SRAM (KB)		128
Timers	STIM	1
	GPTM	3
	WDT	1
	RTC	1
Communication	SPI	1
	UART	2
	I <sup>2</sup> C	2
	SCI (ISO7816-3)	1
	IrDA	1
	I <sup>2</sup> S/LJF/PCM	1
AES-128		1
TRNG		1
QEI (Quadrature Encoder I/F)		1
12-bit ADC	Number of ADC	1
	Number of channels	5
TSEN (Temperature sensor)		1
GPIO		Up to 16
CPU frequency		Up to 64 MHz
Operating voltage		1.8 V ~ 3.6 V
Operating temperature		-40 °C ~ 85 °C
Package		28-pin LGA

## Block Diagram

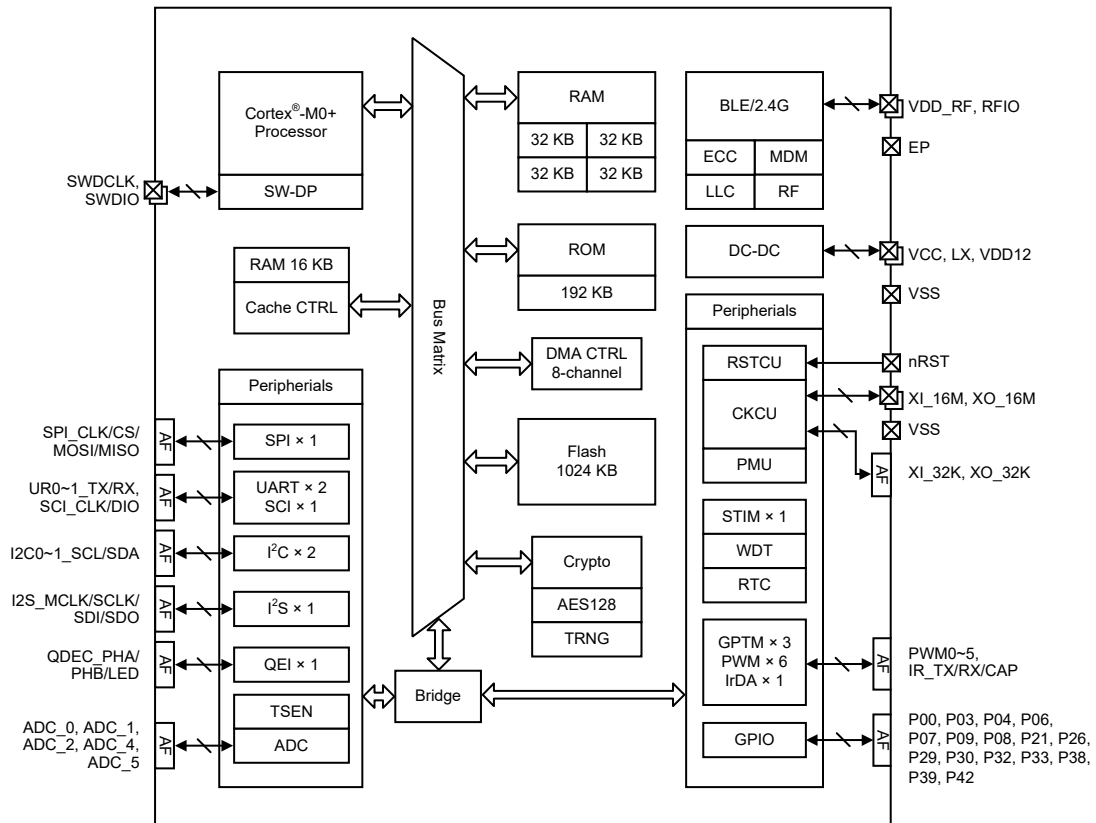


Figure 1. Block Diagram

# 4 Pin Assignment

**HT32F67593**  
**28 LGA-A**

Default		P00	VCC	LX	VDD12	VDD_RET	VDD_RF	VSS	Default		
Default		21	20	19	18	17	16	15	Default		
		33V <sub>A</sub>	AP	33V <sub>A</sub>	P12	P12	P12	AP			
XO_16M	22	33V <sub>A</sub>	AP	3.3 V Analog Power Pad					RF	14	RFIO
XI_16M	23	33V <sub>A</sub>	P12	1.2 V Power Pad					33V	13	P29
nRST	24	33V <sub>PU</sub>	33V <sub>A</sub>	3.3 V Digital & Analog I/O Pad					33V	12	P07
XO_32K	25	33V <sub>A</sub>	33V	3.3 V Digital I/O Pad					33V	11	P42
XI_32K	26	33V <sub>A</sub>	RF	RF Pad					33V	10	P26
P33	27	33V <sub>A</sub>	33V <sub>PU</sub>	3.3V Pad with default Pull-up					33V	9	P39
P21	28	33V <sub>A</sub>	EP: VSS					33V <sub>PU</sub>	8	SWDIO	
○		33V <sub>A</sub>	33V <sub>A</sub>	33V <sub>A</sub>	33V <sub>A</sub>	33V	33V	33V <sub>PU</sub>			
Default		1	2	3	4	5	6	7	Default		
		P38	P03	P32	P09	P08	P30	SWCLK			

Figure 2. 28-pin LGA Pin Assignment

**Table 2. Pin Assignment**

Package	Alternate Function Mapping											
	28LGA	Default	GPIO	ADC×1	IrDA×1	CLKOUT	SPI	I <sup>2</sup> C×2	UART×2	PWM×6	QEI×1	I <sup>2</sup> S/PCM×1
28	P21		ADC_2				V	V	V	V	V	V
1	P38				16MOUT		V	V	V	V	V	V
2	P03		ADC_0				V	V	V	V	V	V
3	P32		ADC_4				V	V	V	V	V	V
4	P09		ADC_1				V	V	V	V	V	V
5	P08						V	V	V	V	V	V
6	P30						V	V	V	V	V	V
7	SWCLK											
8	SWDIO											
9	P39						V	V	V	V	V	V
10	P26						V	V	V	V	V	V
11	P42						V	V	V	V	V	V
12	P07						V	V	V	V	V	V
13	P29				32KOUT		V	V	V	V	V	V
14	RFIO											
15	VSS											
16	VDD_RF											
17	VDD_RET											
18	VDD12											
19	LX											
20	VCC											
21	P00			IR_TX			V	V	V	V	V	V
22	XO_16M											
23	XI_16M											
24	nRST											
25	XO_32K	P04										
26	XI_32K	P06										
27	P33		ADC_5				V	V	V	V	V	V

Note: Alternate Function “V”: Programmable

**Table 3. Alternate Function Mapping**

PID	Function	PID	Function	PID	Function	PID	Function	PID	Function
0	GPIO	20	SPI_CLK	34	I2S_WCLK	46	GPTM1_IR_OUT	58	GPTM2_B_DECODE
1	UART0_CTS	21	SPI_MISO	35	I2S_SDATA	47	GPTM1_CAP0	71	PDM_CLK_OUT
2	UART0_RXD	22	SPI_CS	36	I2S_MCLK	48	GPTM1_CAP1	72	PDM_SDATA_INPUT
3	UART0_RTS	23	SPI_MOSI	37	QDEC_PHA	49	GPTM1_A_PWM	106	TRXS_RF_SWITCH0
4	UART0_TXD	24	TEST_CLK_OUTPUT (Only for P29)	38	QDEC_PHB	50	GPTM1_B_PWM	107	TRXS_RF_SWITCH1
5	UART1_CTS	25	CLOCK_OUTPUT (Only for P38)	39	QDEC_LED	51	GPTM1_A_DECODE	108	TRXS_RF_SWITCH2
6	UART1_RXD	26	I2C0_SCL	40	GPTM0_CAP0	52	GPTM1_B_DECODE	109	CLKOUT
7	UART1_RTS	27	I2C0_SDA	41	GPTM0_CAP1	53	GPTM2_CAP0	111	PA_EXT_EN
8	UART1_TXD	28	I2C1_SCL	42	GPTM0_A_PWM	54	GPTM2_CAP1	112	LNA_EXT_EN
13	7816_UAM_CLK	29	I2C1_SDA	43	GPTM0_B_PWM	55	GPTM2_A_PWM	113	ADC_TRIG
14	7816_UAM_DAT	32	I2S_ODATA	44	GPTM0_A_DECODE	56	GPTM2_B_PWM		
15	7816_UAM_RST_N	33	I2S_BCLK	45	GPTM0_B_DECODE	57	GPTM2_A_DECODE		

**Table 4. Pin Description**

Pin Number 28 LGA	Pin Name	Type <sup>(1)</sup>	I/O Structure <sup>(2)</sup>	Description	
				Default Function	Common Function
28	P21	AI/O	33V	P21	ADC_2
1	P38	AI/O	33V	P38	16MOUT
2	P03	AI/O	33V	P03	ADC_0
3	P32	AI/O	33V	P32	ADC_4
4	P09	AI/O	33V	P09	ADC_1
5	P08	I/O	33V	P08	—
6	P30	I/O	33V	P30	—
7	SWCLK	I	33V_PU	SWCLK	—
8	SWDIO	I/O	33V_PU	SWDIO	—
9	P39	I/O	33V	P39	—
10	P26	I/O	33V	P26	—
11	P42	I/O	33V	P42	—
12	P07	I/O	33V	P07	—
13	P29	I/O	33V	P29	32KOUT
14	RFIO	AI/O	12V	RF I/O	—
15	VSS	P	—	RF power ground	—
17	VDD_RF	P	12V	VDD for RF Block	—
16	VDD_RET	P	12V	VDD for Retention	—
18	VDD12	P	12V	DC-DC Output (1.2 V)	—
19	LX	AO	33V	DC-DC switching output	—
20	VCC	P	33V	Power Supply (1.8~3.6 V)	—
21	P00	AI/O	33V	P00	IR_TX
22	XO_16M	AO	33V	External 16 MHz DCXO XO	—
23	XI_16M	AI	33V	External 16 MHz DCXO XI	—
24	nRST	I	33V_PU	External reset pin	—
25	XO_32K	AO	33V	XO_32K	P04
26	XI_32K	AI	33V	XI_32K	P06
27	P09	AI/O	33V	P09	ADC_5

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply

2. 33V = 3.3 V tolerant, PU = Pull-up, 12V = 1.2 V

3. The EP means the exposed pad on the packages. It must be connected to ground.

# 5 Electrical Characteristics

## Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5. Absolute Maximum Ratings**

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	External Main Supply Voltage	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 3.6	V
V <sub>IN</sub>	Input Voltage on I/O	V <sub>SS</sub> - 0.3	V <sub>CC</sub> + 0.3	V
T <sub>A</sub>	Ambient Operating Temperature Range	-40	85	°C
T <sub>STG</sub>	Storage Temperature Range	-60	150	°C
T <sub>J</sub>	Maximum Junction Temperature	—	125	°C
V <sub>ESD</sub>	Electrostatic Discharge Voltage – Human Body Mode	-2000	2000	V
	Electrostatic Discharge Voltage – Charged Device Mode	-500	500	V

## Recommended DC Operating Conditions

**Table 6. Recommended DC Operating Conditions**

T<sub>A</sub> = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Main Operating Voltage	—	1.8 <sup>(1)</sup>	3.3	3.6	V
V <sub>ADC</sub>	ADC Input Voltage <sup>(2)</sup>	—	0.0	—	1.1	V
V <sub>OSC</sub>	Crystal Oscillator Input Voltage	—	0.5	—	1.2	V

Note: 1. After reset is released, device functionality is guaranteed even when the V<sub>CC</sub> drops to the V<sub>BOR</sub> minimum (1.62 V).

2. The ADC pin option voltage range is 0 V to 1.1 V, with a pin tolerance of 3.6 V.

3. All voltage values are with respect to ground, unless otherwise noted.

## Power Consumption

**Table 7. Power Consumption Characteristics**

T<sub>A</sub> = 25 °C, V<sub>CC</sub> = 3.0 V and V<sub>DD\_RET</sub> = 1.1 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>LDO Mode</b>						
I <sub>ACT</sub>	16 MHz Active	Internal RC	—	1.2	—	mA
		External 16 MHz Crystal	—	1.65	—	mA
	Radio RX	@ 1 Mbps PHY	—	9.4	—	mA
		@ 2 Mbps PHY	—	9.4	—	mA
	Radio TX	@ 0 dBm	—	10	—	mA
@ 10 dBm		—	40.5	—	mA	
I <sub>SLP</sub>	Sleep	128K SRAM Retention	—	7.5	—	µA
		64K SRAM Retention	—	5.2	—	µA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>DSL</sub> P	Deep-Sleep	RTC On, External 32K Crystal	—	3.1	—	μA
I <sub>HIB</sub>	Hibernation	RTC Off	—	1.6	—	μA
<b>DC/DC Mode</b> <sup>(Note)</sup>						
I <sub>ACT</sub>	16 MHz Active	Internal RC	—	0.77	—	mA
		External 16 MHz Crystal	—	1.2	—	mA
	Radio RX	@ 1 Mbps PHY	—	4.1	—	mA
		@ 2 Mbps PHY	—	4.2	—	mA
Radio TX	@ 0 dBm	—	4.5	—	mA	
	@ 10 dBm	—	12	—	mA	
I <sub>S</sub> LP	Sleep	128K SRAM Retention	—	2.9	—	μA
		64K SRAM Retention	—	2.5	—	μA
I <sub>DSL</sub> P	Deep-Sleep	RTC On, External 32K Crystal	—	2	—	μA
I <sub>HIB</sub>	Hibernation	RTC Off	—	1.6	—	μA

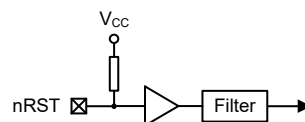
Note: The real current in the DC/DC mode depends on the inductor component selection. The DC/DC minimum operating voltage is 2.2V. When the V<sub>CC</sub> supply voltage drops below 2.2V, the Power mode must be configured to LDO Mode.

## Reset Characteristics

**Table 8. V<sub>CC</sub> Power Reset Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R <sub>PU</sub>	Weak Internal Pull-up Equivalent Resistor	V <sub>CC</sub> = 3.3 V	100	110	120	kΩ
		V <sub>CC</sub> = 3.0 V	110	125	140	
		V <sub>CC</sub> = 2.5 V	130	160	190	
		V <sub>CC</sub> = 1.8 V	260	290	320	
t <sub>PUS</sub>	Reset Input Pulse	1.8 V < V <sub>CC</sub> < 3.6 V	—	—	100	ns



**Figure 3. nRST Pin Block Diagram**

## External Clock Characteristics

**Table 9. 16 MHz External Crystal Oscillator Characteristics**

T<sub>A</sub> = 25 °C & V<sub>CC</sub> = 3.0 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ESR	Equivalent Series Resistance	6 pF < C <sub>L</sub> < 9 pF	—	20	120	Ω
C <sub>L</sub>	Crystal Load Capacitance	—	3	—	27	pF
f <sub>HSE</sub>	Crystal Frequency	—	—	16	—	MHz
FT <sub>HSE</sub>	Crystal Frequency Tolerance	—	-20	—	20	ppm
t <sub>HSE</sub> SU	Start-up Time	—	1.3	1.5	2.3	ms
TOL <sub>HSE</sub>	Crystal Tolerance	T <sub>A</sub> = 25 ± 3 °C	—	—	±10	ppm
		T <sub>A</sub> = -20 ~ 75 °C	—	—	±10	ppm

**Table 10. 32.768 kHz External Crystal Oscillator Characteristics**

$T_A = 25\text{ }^\circ\text{C}$  &  $V_{CC} = 3.0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ESR	Equivalent Series Resistance	$6\text{ pF} < C_L < 9\text{ pF}$	—	30	100	$\Omega$
$C_L$	Crystal Load Capacitance	—	3	—	27	pF
$f_{LSE}$	Crystal Frequency	—	—	32.768	—	kHz
$FT_{LSE}$	Crystal Frequency Tolerance	—	-50	—	50	ppm
$t_{LSESU}$	Start-up Time	—	—	3	—	ms

## Internal Clock Characteristics

**Table 11. 32 kHz Internal RC Oscillator Characteristics**

$T_A = 25\text{ }^\circ\text{C}$  &  $V_{CC} = 3.0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$f_{IRC32K}$	Internal 32 kHz RC Oscillation Frequency	Calibrate frequency	31.9	32	32.1	kHz
$TC_{IRC32K}$	Temperature Coefficient	—	—	100	—	ppm/ $^\circ\text{C}$

**Table 12. 16 MHz Internal RC Oscillator Characteristics**

$T_A = 25\text{ }^\circ\text{C}$  &  $V_{CC} = 3.0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$f_{IRC16M}$	Internal 16 MHz RC Oscillation Frequency	Calibrate frequency	15.68	16.0	16.32	MHz
$TC_{IRC16M}$	Temperature Coefficient	—	—	100	—	ppm/ $^\circ\text{C}$

**Table 13. 48 MHz Internal RC Oscillator Characteristics**

$T_A = 25\text{ }^\circ\text{C}$  &  $V_{CC} = 3.0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$f_{IRC48M}$	Internal 48 MHz RC Oscillation Frequency	Calibration frequency	45.68	48.0	48.3	MHz
$TC_{IRC48M}$	Temperature Coefficient	—	—	100	—	ppm/ $^\circ\text{C}$
$FAC_{IRC48M\_NOCAL}$	Frequency Accuracy	No calibration	$\pm 2$	$\pm 3$	$\pm 5$	%
$T_{IRC48\_START-UP}$	Start-up Time	—	—	8	10	$\mu\text{s}$

## RF Characteristics

**Table 14. Radio RX Characteristics**

$T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.0\text{ V}$  & LDO Mode, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$P_{MIN}$	Sensitivity @ 1 Mbps	—	-94	—	dBm
	Sensitivity @ 2 Mbps	—	-92	—	
	Sensitivity @ Long Range 500 Kbps	—	-100	—	
	Sensitivity @ Long Range 125 Kbps	—	-102	—	
$P_{MAX}$	Max Input Power	—	-10	—	dBm
<b>In-Band Blocking</b>					
$C_{IO}$	Co-channel Interference, Wanted Signal -67 dBm	—	13	—	dB
$C_{I1}$	30.8% PER, Interferer at $f_{OFFS} = +1\text{ MHz}$	—	0	—	dB
	30.8% PER, Interferer at $f_{OFFS} = -1\text{ MHz}$	—	3	—	
$C_{I2}$	30.8% PER, Interferer at $f_{OFFS} = +2\text{ MHz}$	—	-34	—	dB
	30.8% PER, Interferer at $f_{OFFS} = -2\text{ MHz}$	—	-33	—	

Symbol	Parameter	Min.	Typ.	Max.	Unit
C <sub>I3</sub>	30.8% PER, Interferer at f <sub>OFFS</sub> = +3 MHz	—	-40	—	dB
	30.8% PER, Interferer at f <sub>OFFS</sub> = -3 MHz	—	-34	—	
C <sub>I4</sub>	30.8% PER, Interferer at Image Channel (f <sub>IMAGE</sub> )	—	-18	—	dB
C <sub>I5</sub>	30.8% PER, Interferer at Image Channel (f <sub>IMAGE</sub> + 1 MHz)	—	-34	—	dB
	30.8% PER, Interferer at Image Channel (f <sub>IMAGE</sub> - 1 MHz)	—	-45	—	
<b>Out-of-Band Blocking</b>					
	f = 30 ~ 2,000 MHz	—	-40	—	dBm
	f = 2,000 ~ 2,399 MHz	—	-19	—	
	f = 2,484 ~ 3,000 MHz	—	-22	—	
	f = 3,000 ~ 12,750 MHz	—	-42	—	
	Intermodulation Performance for Wanted Signal at -64 dBm and 1 Mbps BLE, 3 <sup>rd</sup> , 4 <sup>th</sup> and 5 <sup>th</sup> Offset Channel	—	-35	—	dBm
P <sub>ISSI</sub>	Upper Limit of Monotonous Range	-94	—	-20	dBm

**Table 15. Radio TX Characteristics**

T<sub>A</sub> = 25 °C, V<sub>CC</sub> = 3.0 V & LDO Mode, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
P <sub>TX</sub>	Output Power	-40	0	10	dBm
	TX RF Output Step	—	3	—	dB
ΔF2AVG	Average Frequency Deviation for 10101010 Pattern @ 1 Mbps	240	248	250	kHz
ΔF1AVG	Average Frequency Deviation for 11110000 Pattern @ 1 Mbps	240	248	270	kHz
	ΔF2AVG/ΔF1AVG @ 1M	0.8	1	1.08	
Carrier	Frequency Accuracy	-150	-68	150	kHz
	Maximum Frequency Drift	-50	-5	50	
	Initial Frequency Drift	-23	-3	23	
	Maximum Drift Rate (per 50 μs)	-20	0	20	
<b>In-Band Emissions</b>					
	< f ± 2 MHz( f = 2400 ~ 2483.5 MHz, P <sub>TX</sub> = 0 dBm)	—	-44	—	dBm
<b>Harmonics</b>					
	2 <sup>nd</sup> , Output Power 0 dBm( f = 2440 MHz)	—	-48	—	dBm
	3 <sup>rd</sup> , Output Power 0 dBm( f = 2440 MHz)	—	-48	—	
	4 <sup>th</sup> , Output Power 0 dBm( f = 2440 MHz)	—	-48	—	
	5 <sup>th</sup> , Output Power 0 dBm( f = 2440 MHz)	—	-48	—	

## I/O Port Characteristics

**Table 16. I/O Port Characteristics**

T<sub>A</sub> = 25 °C & V<sub>CC</sub> = 3.0 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	I/O Input Low Level	1.8 < V <sub>CC</sub> < 3.6V	—	—	0.3V <sub>CC</sub>	V
V <sub>IH</sub>	I/O Input High Level	1.8 < V <sub>CC</sub> < 3.6V	0.7V <sub>CC</sub>	—	—	V
C <sub>IO</sub>	I/O Pin Capacitance	—	—	5	—	pF
R <sub>PU</sub>	Pull-up Equivalent Resistor	V <sub>CC</sub> = 3.3 V	—	40	50	kΩ
		V <sub>CC</sub> = 3.0 V	—	42	52	kΩ
		V <sub>CC</sub> = 2.5 V	—	51	60	kΩ
		V <sub>CC</sub> = 1.8 V	—	85	100	kΩ

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R <sub>PD</sub>	Pull-down Equivalent Resistor	V <sub>CC</sub> = 3.3 V	40	45	55	kΩ
		V <sub>CC</sub> = 3.0 V	45	50	60	kΩ
		V <sub>CC</sub> = 2.5 V	55	60	70	kΩ
		V <sub>CC</sub> = 1.8 V	85	100	115	kΩ
I <sub>DRV0</sub>	Level-0	V <sub>CC</sub> = 3.3 V	5.43	5.45	5.46	mA
		V <sub>CC</sub> = 3.0 V	4.42	4.62	4.71	mA
		V <sub>CC</sub> = 2.5 V	3.72	3.74	3.75	mA
		V <sub>CC</sub> = 1.8 V	1.72	1.78	1.83	mA
I <sub>DRV1</sub>	Level-1	V <sub>CC</sub> = 3.3 V	9.68	9.71	9.75	mA
		V <sub>CC</sub> = 3.0 V	8.49	8.54	8.62	mA
		V <sub>CC</sub> = 2.5 V	6.32	6.38	6.43	mA
		V <sub>CC</sub> = 1.8 V	3.67	3.76	3.78	mA
I <sub>DRV2</sub>	Level-2	V <sub>CC</sub> = 3.3 V	12.30	12.80	13.00	mA
		V <sub>CC</sub> = 3.0 V	10.7	11.32	11.36	mA
		V <sub>CC</sub> = 2.5 V	8.52	8.56	8.58	mA
		V <sub>CC</sub> = 1.8 V	5.10	5.40	5.42	mA
I <sub>DRV3</sub>	Level-3	V <sub>CC</sub> = 3.3 V	13.62	14.76	15.67	mA
		V <sub>CC</sub> = 3.0 V	12.35	13.20	13.60	mA
		V <sub>CC</sub> = 2.5 V	9.76	10.60	11.30	mA
		V <sub>CC</sub> = 1.8 V	6.17	6.24	6.38	mA

## ADC Characteristics

Table 17. ADC Characteristics

T<sub>A</sub> = 25 °C & V<sub>CC</sub> = 3.0 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>REF</sub>	Reference Voltage <sup>(1)</sup>	—	—	1.1	—	V
f <sub>ADC</sub>	Clock Frequency	—	—	16	—	MHz
f <sub>S</sub>	Sampling Rate <sup>(3)</sup>	12-bit (Down sample = 16)	—	1	—	MspS
		10-bit (Down sample = 1)	—	16	—	MspS
t <sub>TRIG</sub>	External Trigger Period	—	—	—	10	1/f <sub>ADC</sub>
V <sub>AIN</sub>	Conversion Voltage Range	—	0	—	V <sub>REF+</sub>	V
R <sub>AIN</sub>	External Input Impedance	—	—	—	10	MΩ
C <sub>ADC</sub>	Internal S/H Capacitor Impedance	—	—	5	—	pF
t <sub>PU</sub>	Power-up Time	—	—	1	—	CC <sup>(2)</sup>
t <sub>S</sub>	Sampling Time	—	—	0.5	—	1/f <sub>ADC</sub>
ACC	Accuracy	V <sub>AIN</sub> < 50 mV	—	±10	—	LSB
		50 mV < V <sub>AIN</sub> < 1.1 V	—	±2	±3	LSB
ENOB	Effective Number of Bits	12-bit	—	11.5	—	Bits

Note: 1. When V<sub>AIN</sub> > V<sub>REF+</sub>, the ADC convert result is 0xFFFF.

2. CC: Conversion Cycle.

3. Sampling Rate = f<sub>ADC</sub> / Down sample.

## I<sup>2</sup>C Characteristics

Table 18. I<sup>2</sup>C Characteristics

T<sub>A</sub> = 25 °C, V<sub>CC</sub> = 3.0 V, unless otherwise specified.

Symbol	Parameter	Min	Typ.	Max	Unit
f <sub>SCL</sub>	SCL Clock Frequency	—	400	—	kHz
t <sub>SCL(L)</sub>	SCL Clock Low Time	1.5	—	—	μs
t <sub>SCL(H)</sub>	SCL Clock High Time	1	—	—	μs
t <sub>BUF</sub>	Bus Free Time before A New Transmission	2.5	—	—	μs
t <sub>H(STA)</sub>	START Condition Hold Time	0.6	—	—	μs
t <sub>SU(STA)</sub>	START Condition Setup Time	1.2	—	—	μs
t <sub>H(SDA)</sub>	SDA Data Hold Time	10	—	—	μs
t <sub>SU(SDA)</sub>	SDA Data Setup Time	10	—	—	μs
t <sub>SU(STO)</sub>	STOP Condition Setup Time	1.2	—	—	μs
t <sub>RISE</sub>	SCL and SDA Rise Time	—	0.5	—	μs
t <sub>FALL</sub>	SCL and SDA Fall Time	—	0.5	—	μs
t <sub>AA</sub>	Clock Low to Data Out Valid	0.9	—	1.1	μs
t <sub>DH</sub>	Data Out Hold Time	0.9	—	—	μs

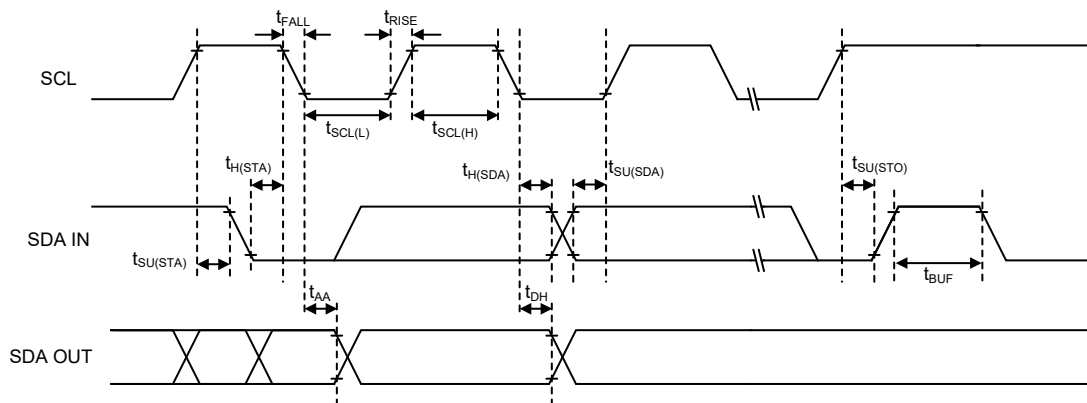


Figure 4. I<sup>2</sup>C Timing Diagram

## SPI Characteristics

Table 19. SPI Characteristics

$T_A = 25\text{ }^\circ\text{C}$  &  $V_{CC} = 3.0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/t_{CK}$	Clock Frequency	$1.8\text{ V} < V_{CC} < 3.6\text{ V}$	—	—	16	MHz
$t_{W(CKH)}$	Clock High Time	—	$t_{CK}/2-0.5$	—	$t_{CK}/2$	ns
$t_{W(CKL)}$	Clock Low Time	—	$t_{CK}/2$	—	$t_{CK}/2+0.5$	ns
$t_{S(IN)}$	Data Input Setup Time	—	8	—	—	ns
$t_{H(IN)}$	Data Input Hold Time	—	3.5	—	—	ns
$t_{V(OUT)}$	Data Output Valid Time	—	—	1	2	ns
$t_{H(OUT)}$	Data Output Hold Time	—	0	—	—	ns

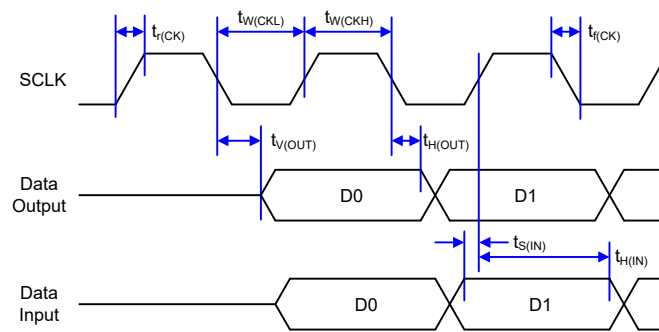


Figure 5. SPI Timing Diagram

## TSEN Characteristics

Table 20. TSEN Characteristics

$T_A = 25\text{ }^\circ\text{C}$  &  $V_{CC} = 3.0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TC	Sensor Temperature Coefficient	—	—	2	—	mV/°C
$T_{RNG}$	Temperature Sensor Range	—	-40	—	125	°C
$T_{ACC}$	Temperature Sensor Accuracy	—	-8	—	8	°C
$T_{RES}$	Temperature Sensor Resolution	—	—	0.3	—	°C
$t_{V(OUT)}$	Data Output Valid Time	—	—	0.3	—	ns
$I_{TSEN}$	Temperature Sensor Current	—	—	20	—	μA

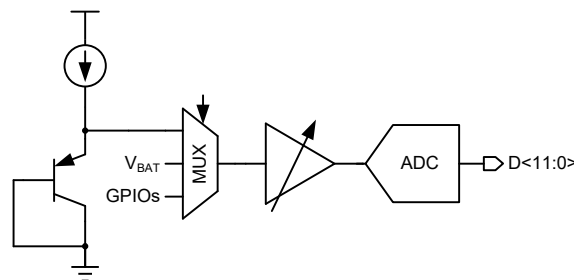


Figure 6. TSEN Operation Diagram

## 6 Package Information

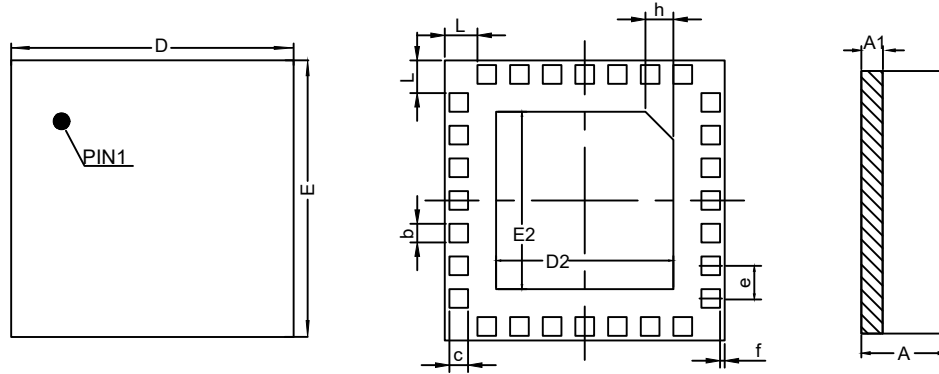
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Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package/Carton Information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

## 28-pin LGA (3mm × 3mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.024	0.026	0.028
A1	0.006	0.007	0.008
b	0.007	0.008	0.009
c	0.007	0.008	0.009
D	0.114	0.118	0.122
D2	0.071	0.075	0.079
e	0.013	0.014	0.015
E	0.114	0.118	0.122
E2	0.071	0.075	0.079
L	0.013	0.014	0.015
f	0.002	0.002	0.002
h	0.011	0.012	0.013

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.62	0.67	0.72
A1	0.14	0.17	0.20
b	0.17	0.20	0.23
c	0.17	0.20	0.23
D	2.90	3.00	3.10
D2	1.80	1.90	2.00
e	0.33	0.35	0.37
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
L	0.33	0.35	0.37
f	0.045	0.05	0.055
h	0.28	0.30	0.32

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