6V, 3A, Synchronous Step-Down Module with Small Package

1 Features

- 2.5V to 6V Wide Input Range
- Up to 3A Output Current
- 20μA Low Quiescent Current
- 2.4MHz Fixed Switching Frequency
- Forced PWM Operation Mode
- Output Voltage adjustable from 0.6V
- 100% Maximum Duty Cycle
- Constant On Time control for fast response
- Power Good Indicator
- Output Auto Discharge
- EN UVLO Adjustable
- Full Protection, OCP and Hiccup, FB Open/Short Protection, OTP
- Support Pre-Biased Output Startup
- Available in a EMLGA2X2.5-10 Package

2 Applications

- Optical Module
- Networking/Servers
- Power for Portable Products
- Storage (SSD/HDD)
- Space-Limited Application

3 Description

The GD30DM1113 is an easy-to-use synchronous step-down power module that integrates low on-resistance power MOSFETs and an inductor.

The GD30DM1113 offers a compact solution that requires only 5 external components to achieve a 3A of output current efficiently with constant on time (COT) control for fast loop response.

The GD30DM1113 has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open short protection and thermal shutdown in case of excessive power dissipation.

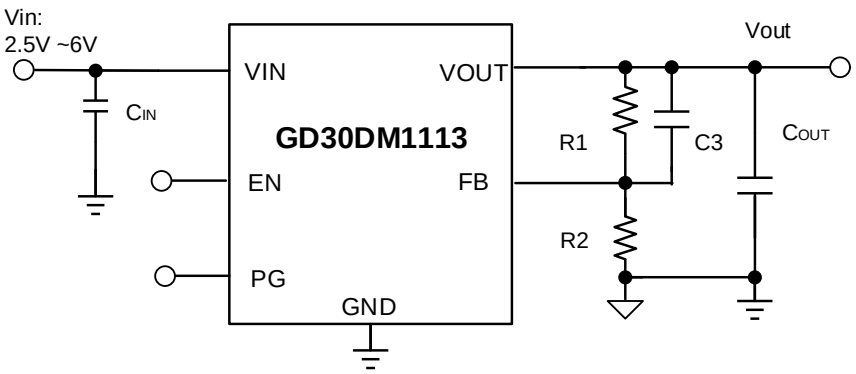
The GD30DM1113 is available in a space-saving EMLGA2.0X2.5-10 package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DM1113	EMLGA2X2.5-10	2.00mm x 2.50mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



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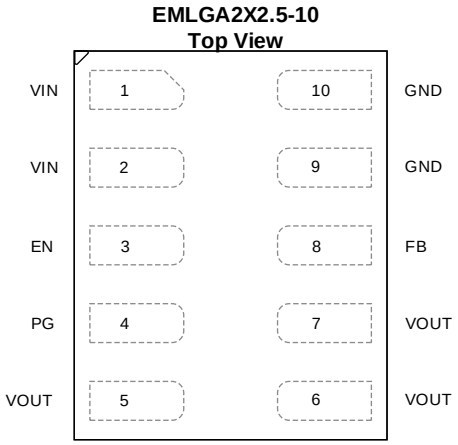
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	EMLGA2X2.5-10		
VIN	1，2	I	**Supply voltage.** The GD30DM1113 operates from a 2.5V to 6V unregulated input. A decoupling capacitor is needed to prevent large voltage spikes from appearing at the input. Place the decoupling capacitor as close to VIN as possible.
EN	3	I	**Enable.** Internal pull up current source. Pull down below 0.85V to disable. Float to enable. See the Enable (EN) Control on page 9 for more details.
PG	4	O	**Power good output.** This is an open-drain signal. A pull-up resistor (connect to VIN or external VCC) is required to indicate high if the output voltage is within regulation. Floating it if not used.
VOUT	5,6,7	O	**Output Voltage Power Rail.** Connect load to VOUT. Output capacitor is needed.
FB	8	I	**Feedback input to the convertor.** Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
GND	9，10	G	**IC ground.** Connect the GND pins to larger copper areas to the negative terminals of the input and output capacitors.

1. I = Input, O = Output, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
VIN	VIN to GND	-0.3	6.5	V
All Other Pins		-0.3	6.5	°C
T_{STG}	Storage temperature	-55	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
VIN	VIN to GND	2.5		6	V
I_{OUT}	Max Continuous Output Current		3		A
T_J	Operating junction temperature	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	EMLGA2X2.5-10	UNIT
Θ_{JA}	Junction to ambient thermal resistance	64	°C/W
Θ_{JC_TOP}	Junction to case(TOP) thermal resistance	22	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-

5.5 Electrical Characteristics

V_{IN} = 5V, V_{EN} = 2V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
VIN_{UVR}	VIN UVLO rising threshold			2.3	2.45	V
VIN_{UV_hys}	VIN UVLO hysteresis			0.2		V
I_Q	Quiescent supply current	V_{EN}=2V, VFB=0.69V, VIN=5V		20		μA
I_{SD}	Shutdown supply current	V_{EN}=0V		2	3	μA
ENABLE						
V_{EN_RISE}	Enable rising threshold			1		V
V_{EN_FALL}	Enable falling threshold			0.85		V
t_{EN_DELAY}				240		μs
I_{EN}	Input current	Enable threshold +50mV		-2.7		μA
	Input current	Enable threshold - 50mV		-0.7		
PEAK CURRENT LIMIT						
I_{LIM_PMOS}	Pmos Peak Current Limit			5		A
I_{LIM_NMOS}	Nmos Peak Current Limit			3.5		A
N_{COP_DIS}	Low-side negative current limit	EN discharge		-2		A
N_{COP_OVP}	Low-side negative current limit	VOUT OVP		-2		A
N_{OCP_CCM}	Low-side negative current limit			-3.5		A
Feedback Voltage and SS						
V_{FB}	Feedback voltage	T_J = 25°C	594	600	606	mV
I_{FB}	Feedback leakage				0.1	μA
I_{LKG}	Switch leakage current	V_{EN}=0V		1		μA
Tss	Soft-Start time	SS float, V_{OUT} from 0% to 100%		1		ms
Output Discharge Resistor						
$R_{DISCHARGE}$	Passive Output discharge resistor	V_{EN}=0V, VOUT=1.2V		130		Ω
Power Good						
$PG_{OVP\_rising\_th}$	Output OVP rising threshold			110%		V_{FB}
$PG_{OVP\_falling\_th}$	Output OVP falling threshold			105%		V_{FB}
$PG_{UVP\_falling\_th}$	UVP threshold falling threshold			90%		V_{FB}
$PG_{UVP\_rising\_th}$	UVP threshold rising threshold			93%		V_{FB}
t_{PG_Dealy}	Power good delay			120		μs
SWITCHING REGULATOR						
FSW	Oscillator frequency			2.4		MHz
t_{ON_MIN}	Minimum switch on time			30		ns
T_{OFF_MIN}	Minimum switch off time			80		ns

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OVP						
V_{OVP}	Output Over-voltage threshold			115%		VFB
V_{OVP_HYS}	Output Over-voltage hysteresis			10%		VFB
t_{OV_DELAY}	OVP delay			4.5		μs
THERMAL SHUTDOWM						
T_{OTP}	Thermal shutdown			160		°C
T_{HYS}	Thermal shutdown hysteresis[1]			30		°C

1. Guaranteed by design and engineering sample characterization.

5.6 Typical Characteristics

VIN = 3.3V, VOUT = 1.2V, CIN = 22μF, COUT = 3*10μF, T_A = 25°C, unless otherwise noted.

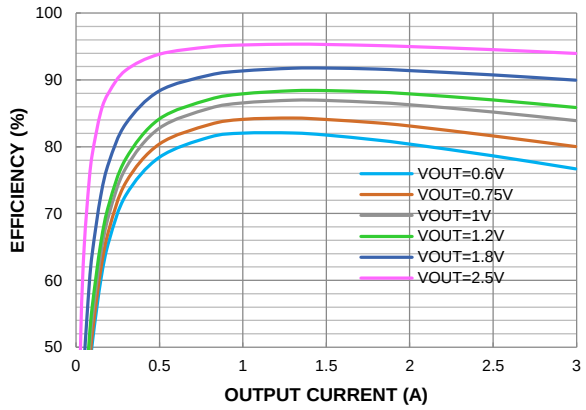


Figure 1. Efficiency vs. Output Current

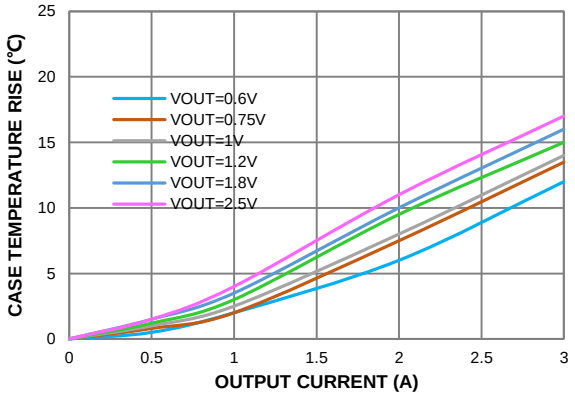


Figure 2. Case Thermal Rise

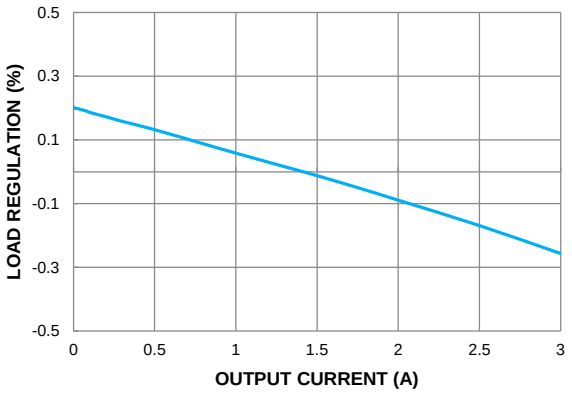


Figure 3. Load Regulation & Vout = 1.2V

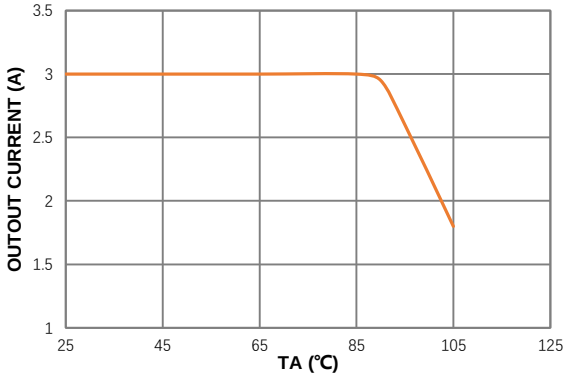


Figure 4. Thermal Derating Curve

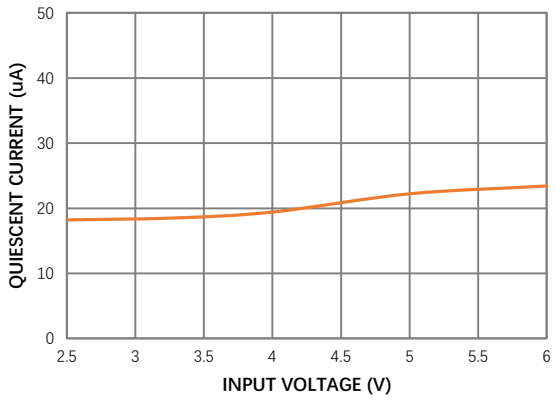


Figure 5. Quiescent Current & VIN=2.5~6V, VEN=2V, V_{FB}=0.63V

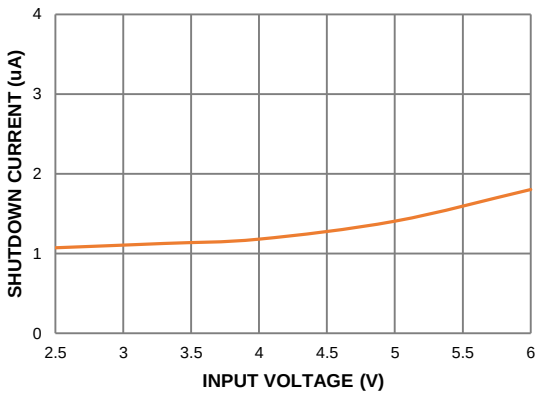


Figure 6. Shutdown Current & VIN=2.5~6V, V_{EN}=0V

5.7 Block Diagram

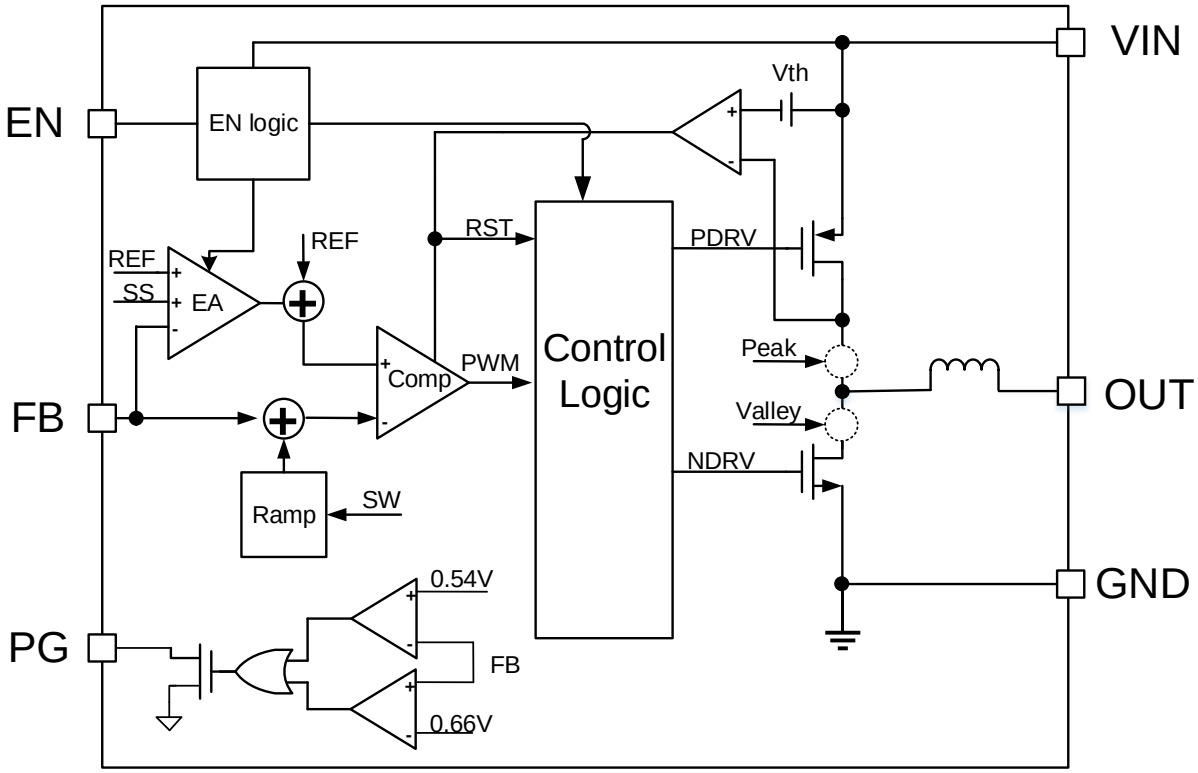


Figure 7. GD30DM1113 Functional Block Diagram

5.8 Operation

The GD30DM1113 is fully integrated synchronous rectified step-down Power Module. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization.

5.8.1 Pulse-Width Modulation (PWM) Control

At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (VFB) is below the reference voltage (VREF), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when VFB drops below VREF. By repeating operation this way, the Power Module regulates the output voltage. The integrated low- side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. To avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

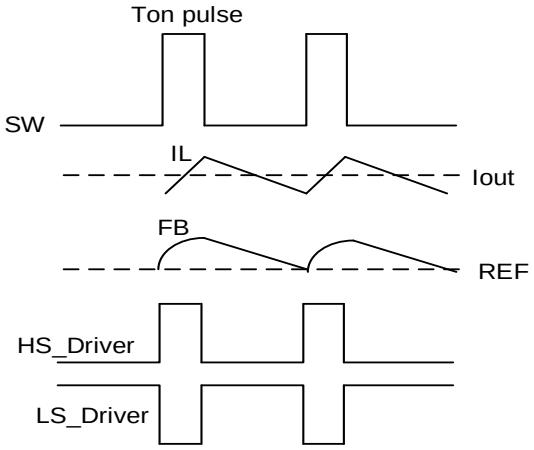


Figure 8. FPWM Operation

An internal compensation mechanism is adopted in the COT control to achieve more stable operation even when ceramic capacitors are used as output capacitors. This internal compensation also improves jitter performance without affecting line or load regulation characteristics.

5.8.2 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is about 2.3V, while its falling threshold is consistently 2.1V.

5.8.3 Enable

The EN pin provides electrical on and off control for the device. Float EN pin or drive EN pin a voltage higher than the rising threshold (1V typically) can enable GD30DM1113, pull the EN pin voltage lower than 0.85V can disable the GD30DM1113.

For adjustable input under voltage, use the EN in as shown in Figure 9 to setup the UVLO by using the two external resistors. Once the EN pin voltage is over 1V, an additional 2.7μA of hysteresis is added. This additional current facilitates input voltage hysteresis. Use the Equation(1) and Equation(2) to set the input startup voltage and stop voltage.

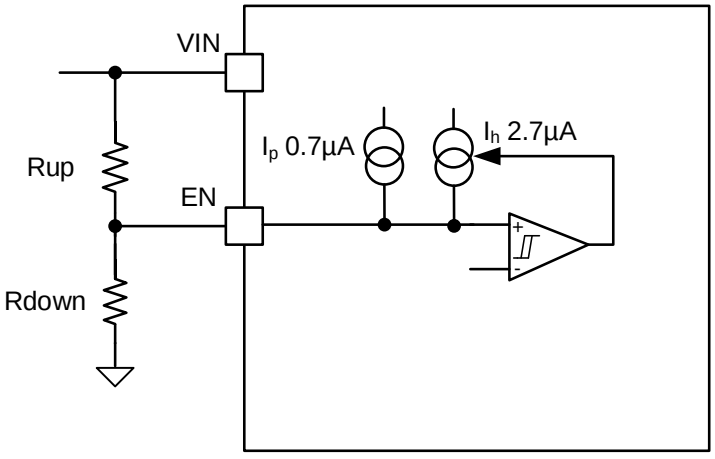


Figure 9. Setup the Input Under Voltage Lockout

$$R_{UP} = \frac{V_{START} * \frac{0.85V}{1V} - V_{STOP}}{0.7\mu A * (1 - \frac{0.85V}{1V}) + 2.7\mu A} \quad (1)$$

$$R_{DOWN} = \frac{R_{UP} * 0.85V}{V_{STOP} - 0.85V + R_{UP} * (2.7\mu A + 0.7\mu A)} \quad (2)$$

5.8.4 Power Good Indicator

The GD30DM1113 has a power good (PG) output. PG is the open drain output and requires an external pull-up resistor (10 ~ 500 kΩ) for power good indication. When the FB voltage is above 93% and less than 110% of the reference voltage, the PG will be pulled up to high, otherwise if FB voltage is out of this window, the PG will be pulled to GND. The MOSFET has a maximum RDS(ON) of less than 10Ω.

PG also has self-bias function, if VIN is absent, even PG pulled up by external power source, PG will be pulled down internally, PG voltage vs. Sink current curve as figure 10 shown.

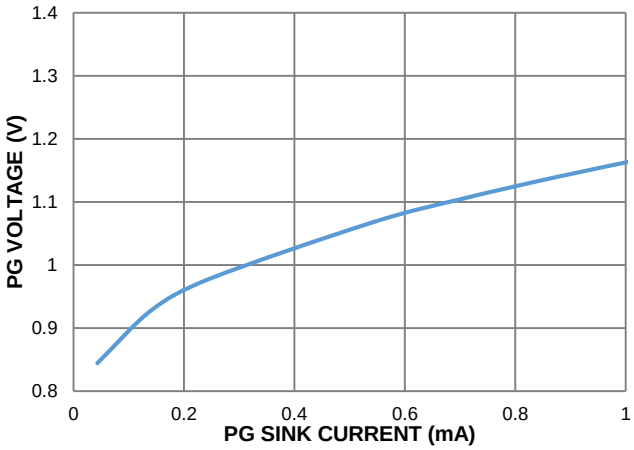


Figure 10. PG Self-bias Voltage Vs Sink Current

5.8.5 Soft-Start

The GD30DM1113 employs a soft-start(SS) mechanism to ensure a smooth output during power-up. When EN&VIN is above the rising threshold, the internal reference voltage ramps up gradually, and the output voltage ramps up smoothly as well. The GD30DM1113 has an internal 22nF SS capacitor. When SS pin is float, SS time is 2ms (Vout from 0% to 100%).

5.8.6 Pre-bias Start-up

The GD30DM1113 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the voltage on the soft start is charged as well, IC will not switch. Once the soft-voltage is above the biased voltage, GD30DM1113 will switch normally.

5.8.7 Output Discharge

During EN shutdown, IC will discharge the output capacitor. After the EN low, there will be two stage output

discharge behavior. The first stage is active discharge, in this condition, IC will turn on the low-side MOSFET to discharge the output capacitor. The low-side MOSFET will be off when -2A negative current limit is triggered. Both high-side and low-side MOSFET will be remains off for 2us then low-side MOSFET will be turned on again. IC will repeat this behavior when the FB voltage discharged to 25% of the reference voltage. The active discharge behavior will be stopped and IC will enable the passive discharge. In passive discharge stage IC will gradually discharge the output to GND via the internal 130ohm discharge FET.

5.8.8 100% Duty Operation

When GD30DM1113 will automatically extend the frequency to support the application when VIN is close to VOUT. The frequency extend circuit will be triggered when minimum off time is reached. The GD30DM1113 can support up to 100% maximum duty cycle once FB is lower than internal Reference.

5.8.9 Over Current Protection and Short Circuits Protection

The GD30DM1113 has a cycle-by-cycle over-current limiting control (OCL). The current-limit circuit employs a valley current-sensing algorithm. The part uses the RDS(ON) of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold (6.5A typically), the device will enter over-current protection mode, High Side FET will not be allowed to turn on until the inductor current falls to valley current limit threshold. Meanwhile the GD30DM1113 will start 31 cycles current limit mode. After the 31 cycle ends, IC will enter hiccup mode.

The GD30DM1113 enters short-circuit protection (SCP) mode when it reaches the current limit and attempts to recover with hiccup mode. In this process, the GD30DM1113 disables the output power stage, discharges the soft-start capacitor, and then attempts to soft start automatically. If the short-circuit condition remains after the soft start ends, the GD30DM1113 repeats this cycle until the short circuit disappears and the output rises back to regulation levels.

When the feedback voltage(VFB) is less than 50% of reference if dead short condition happened, the GD30DM1113 will enter hiccup mode immediately, IC will auto retry once dead short is disappeared.

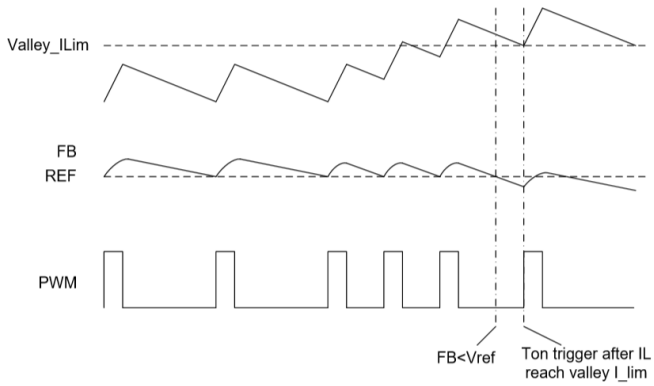


Figure 11. Valley Current limit control

5.8.10 Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the junction temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

6 Application Information

6.1 Typical Application Circuit

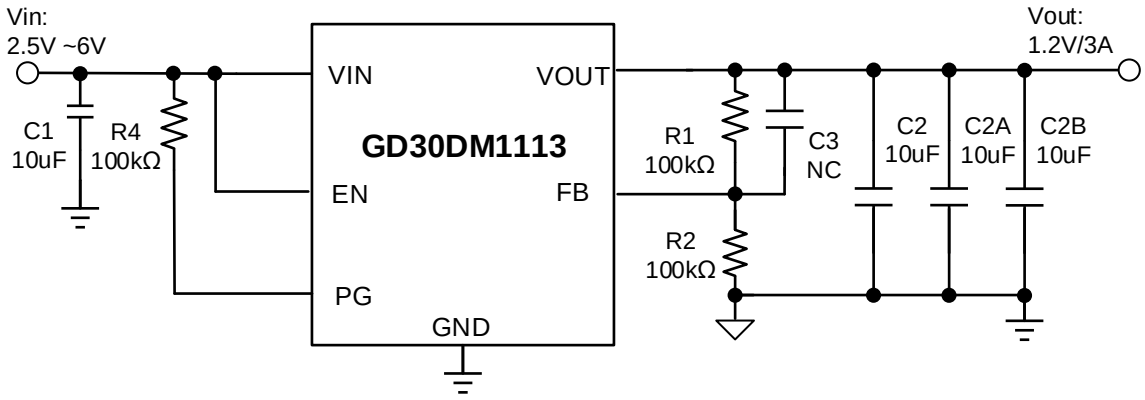


Figure 12. Typical VOUT=1.2V/3A application

6.2 Setting the Output Voltage

The GD30DM1113 output voltage can be set by the external resistor dividers. First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It I recommended to choose a value 20k for R1. The reference voltage is fixed at 0.6V. The feedback network is shown below Figure.

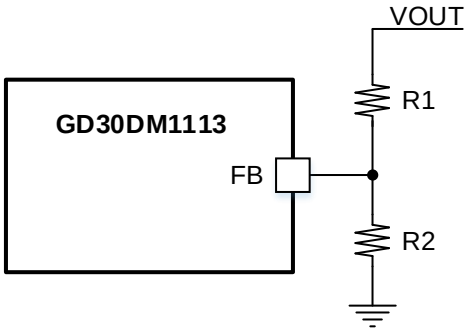


Figure 13. Feedback Network

Choose R1 and R2 using Equation(3):

$$V_{OUT} = \frac{V_{FB}(R_1 + R_2)}{R_2} \quad (3)$$

6.3 Setting Input capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the stepdown converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the

converter. The input ripple current can be estimated as follows:

$$C_{IN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimated as follows:

$$\triangle V_{IN} = \frac{I_{OUT}}{F_{OSC} * C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Worse-case condition is VIN = 2VOUT:

$$\triangle V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} * C_{IN}} \quad (7)$$

6.3.1 Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation(8):

$$\triangle V_{OUT} = \frac{V_{OUT}}{F_{OSC} * L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8F_{OSC} * C_{OUT}}) \quad (8)$$

Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor, FOSC is the switching frequency. Note that, in real application, should consider that the ceramic capacitor capacitance has derating.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple caused by ESR is very small. For simplification, the output voltage ripple can be estimated as:

$$\triangle V_{OUT} = \frac{V_{OUT}}{F_{OSC} * L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (\frac{1}{8F_{OSC} * C_{OUT}}) \quad (9)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\triangle V_{OUT} = \frac{V_{OUT}}{F_{OSC} * L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The GD30DM1113 can be optimized for a wide range of capacitance and ESR values.

Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{OUT_max} can be limited approximately by:

$$C_{OUTMAX} = (I_{LIMITAVE} - I_{OUT}) \times \frac{T_{SS}}{V_{OUT}} \quad (11)$$

Where, ILIM_AVG is the average start-up current during soft-start period, Tss is the soft-start time (2ms typically). The recommended parameters for typical output application as Table 1 shown.

Table 1. Design Example Resistor Selection for Common Output Voltages

VOUT (V)	R1 (kΩ)	R2 (kΩ)	C1 (μF)	C2 (μF)
2.5	100	31.6	22	3*10
1.8	100	50	22	3*10
1.2	100	100	22	3*10
1	66.5	100	22	3*10
0.75	25	100	22	3*10
0.6	0	NC	22	3*10

NOTE 4: 2*10uF Output capacitor also can work normally, but the performance of Output Voltage Ripple maybe not as good. 3*10uF Output capacitor is recommended to improve the performance of Output Voltage Ripple.

6.4 Typical Application Curves

VIN = 3.3V, VOUT = 1.2V, CIN = 22μF, COUT = 3*10μF, TA = 25°C, unless otherwise noted.

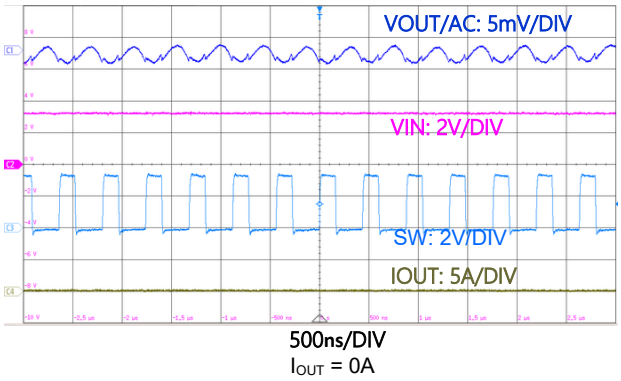


Figure 14. Output Voltage Ripple

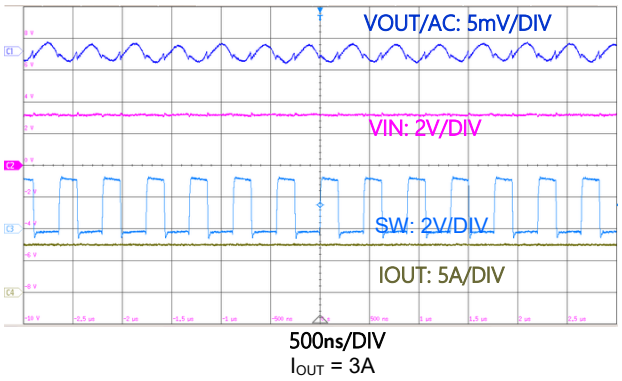


Figure 15. Output Voltage Ripple

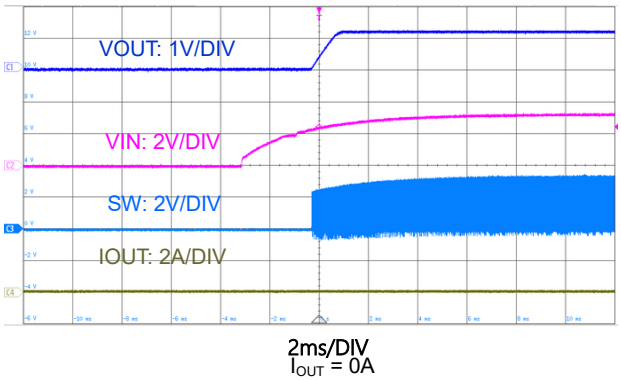


Figure 16. Start-Up through VIN

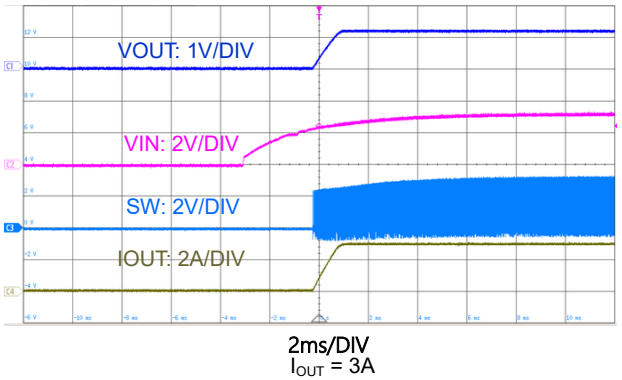


Figure 17. Start-Up through VIN

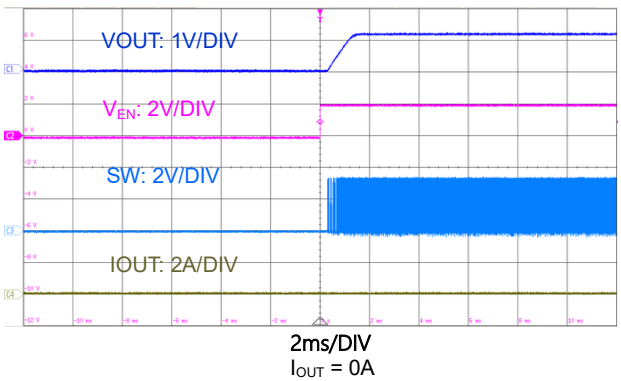


Figure 18. Start-Up through EN

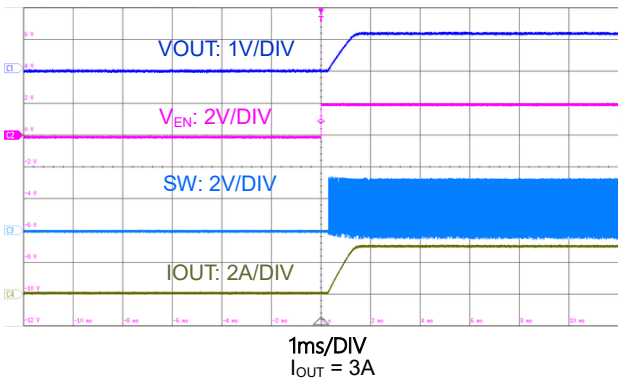
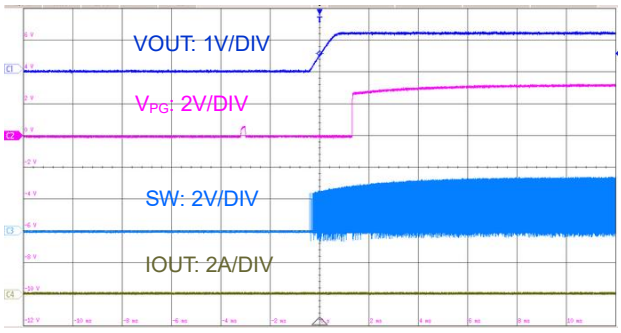
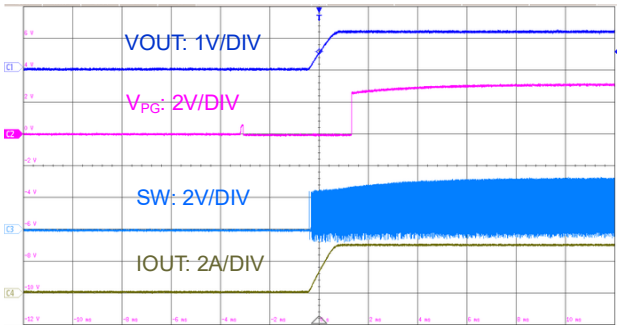


Figure 19. Start-Up through EN



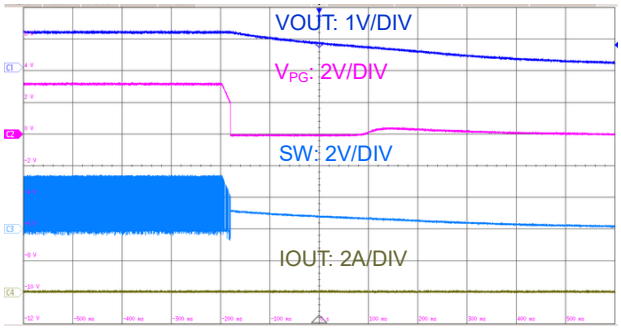
2ms/DIV
I_{OUT} = 0A

Figure 20. PG ON



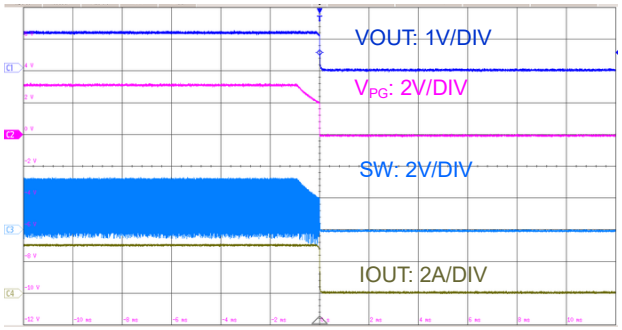
2ms/DIV
I_{OUT} = 3A

Figure 21. PG ON



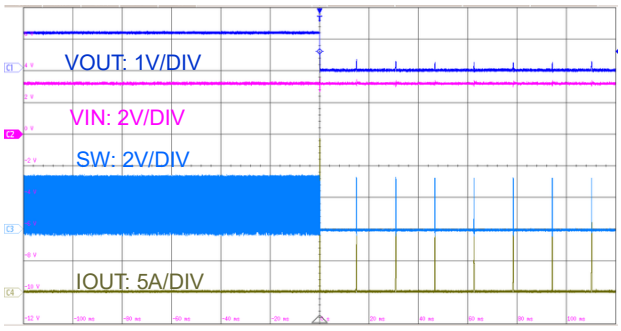
100ms/DIV
I_{OUT} = 0A

Figure 22. PG OFF



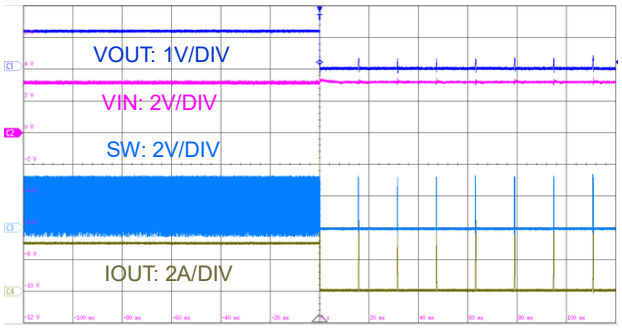
2ms/DIV
I_{OUT} = 3A

Figure 23. PG OFF



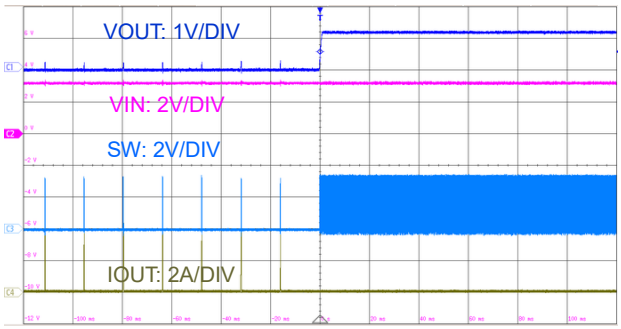
20ms/DIV
I_{OUT} = 0A

Figure 24. Short Entry



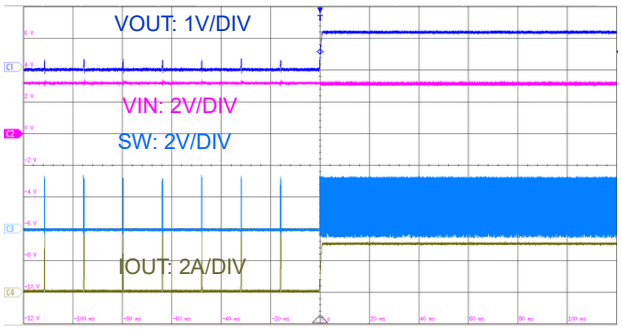
20ms/DIV
I_{OUT} = 3A

Figure 25. Short Entry



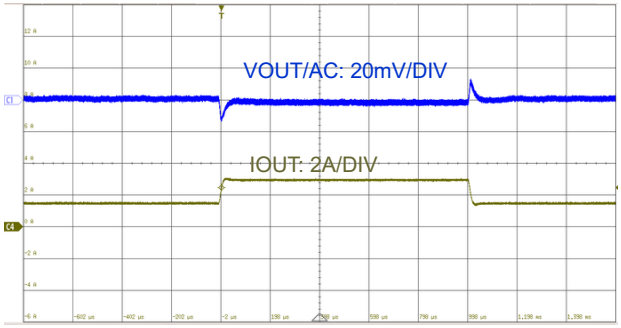
20ms/DIV
I_{OUT} = 0A

Figure 26. Short Recovery



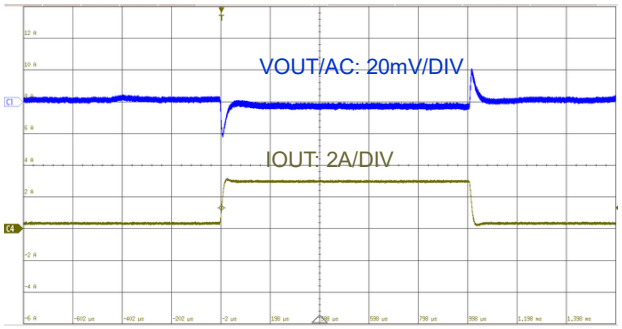
20ms/DIV
I_{OUT} = 3A

Figure 27. Short Recovery



200us/DIV
I_{OUT} = 1.5A to 3A, 1.2A/μs Slew Rate

Figure 28. Load Transient

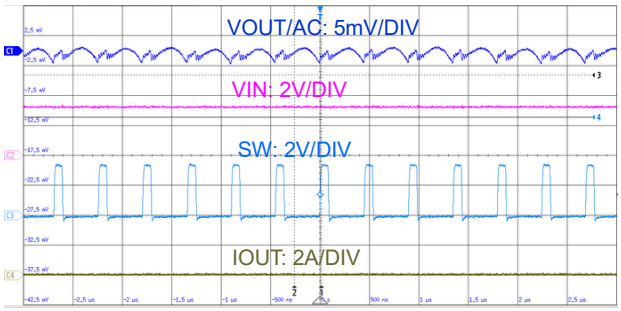


200us/DIV
I_{OUT} = 0.3A to 3A, 1.2A/μs Slew Rate

Figure 29. Load Transient

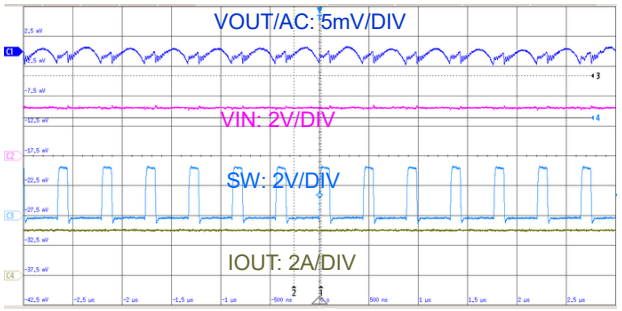
Typical Application Curves (continued)

VIN = 3.3V, VOUT = 0.6V, CIN = 22μF, COUT = 3*10μF, TA = 25°C, unless otherwise noted.



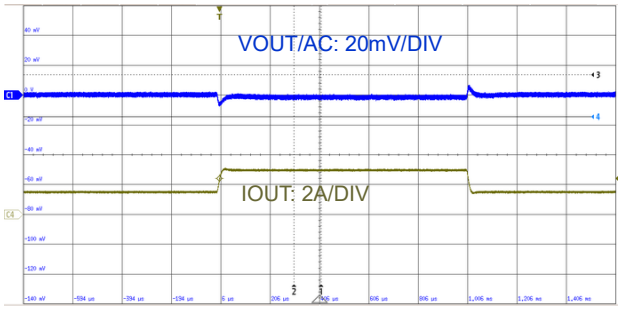
500ns/DIV
I_{OUT} = 0A

Figure 30. Output Voltage Ripple



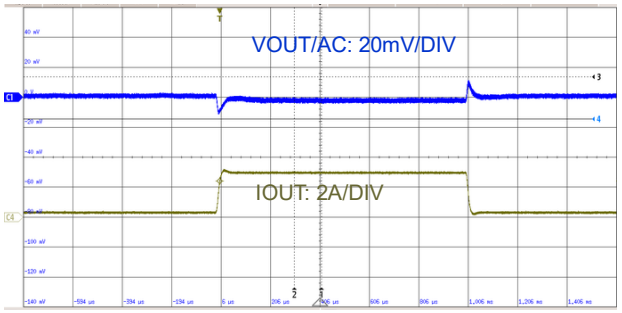
500ns/DIV
I_{OUT} = 6A

Figure 31. Output Voltage Ripple



200us/DIV
I_{OUT} = 1.5A to 3A, 1.2A/μs Slew Rate

Figure 32. Load Transient

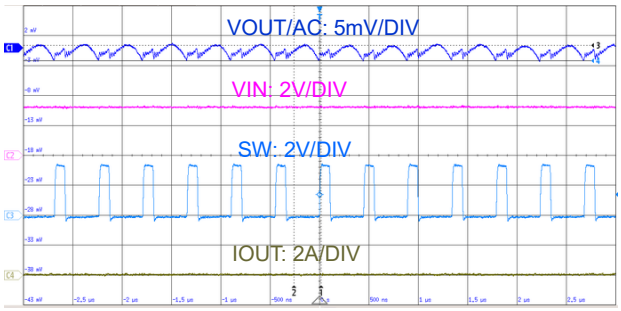


200us/DIV
I_{OUT} = 0.3A to 3A, 1.2A/μs Slew Rate

Figure 33. Load Transient

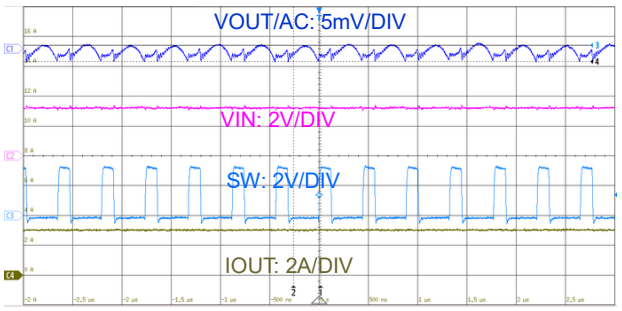
Typical Application Curves (continued)

VIN = 3.3V, VOUT = 0.75V, CIN = 22μF, COUT = 3*10μF, TA = 25°C, unless otherwise noted.



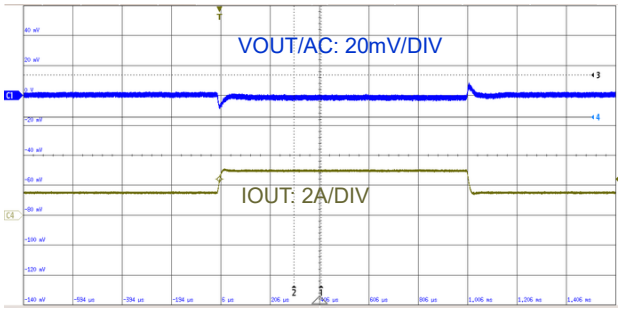
500ns/DIV
I_{OUT} = 0A

Figure 34. Output Voltage Ripple



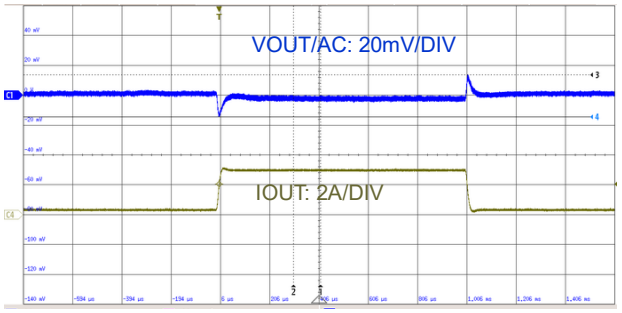
500ns/DIV
I_{OUT} = 3A

Figure 35. Output Voltage Ripple



200us/DIV
I_{OUT} = 1.5A to 3A, 1.2A/μs Slew Rate

Figure 36. Load Transient

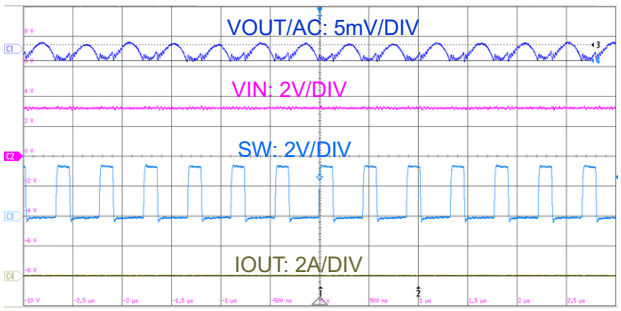


200us/DIV
I_{OUT} = 0.3A to 3A, 1.2A/μs Slew Rate

Figure 37. Load Transient

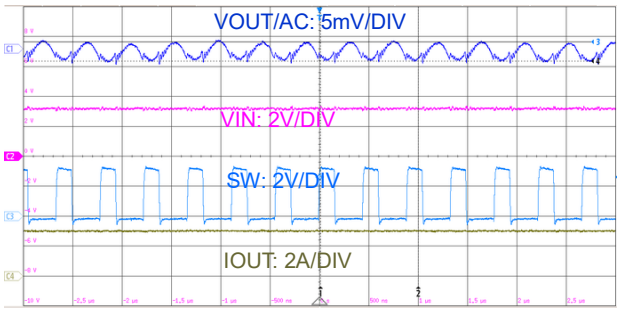
Typical Application Curves (continued)

VIN = 3.3V, VOUT = 1V, CIN = 22μF, COUT = 3*10μF, TA = 25°C, unless otherwise noted.



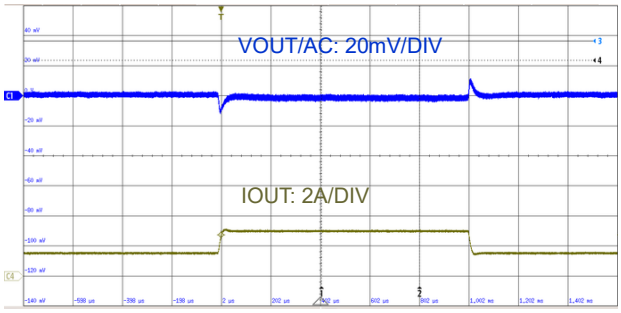
500ns/DIV
I_{OUT} = 0A

Figure 38. Output Voltage Ripple



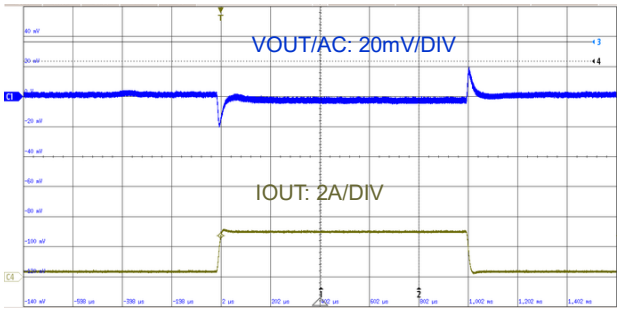
500ns/DIV
I_{OUT} = 3A

Figure 39. Output Voltage Ripple



200us/DIV
I_{OUT} = 1.5A to 3A, 1.2A/μs Slew Rate

Figure 40. Load Transient

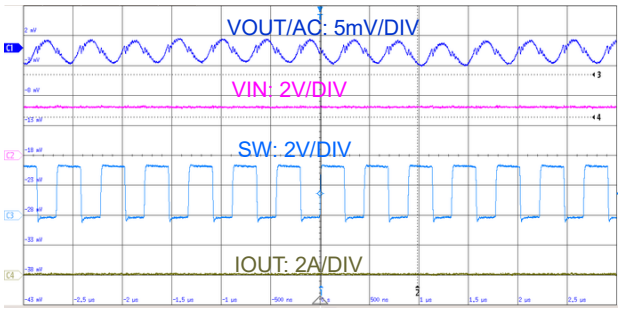


200us/DIV
I_{OUT} = 0.3A to 3A, 1.2A/μs Slew Rate

Figure 41. Load Transient

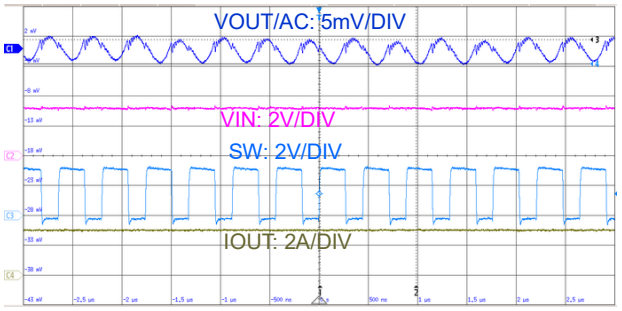
Typical Application Curves (continued)

VIN = 3.3V, VOUT = 1.8V, CIN = 22μF, COUT = 3*10μF, TA = 25°C, unless otherwise noted.



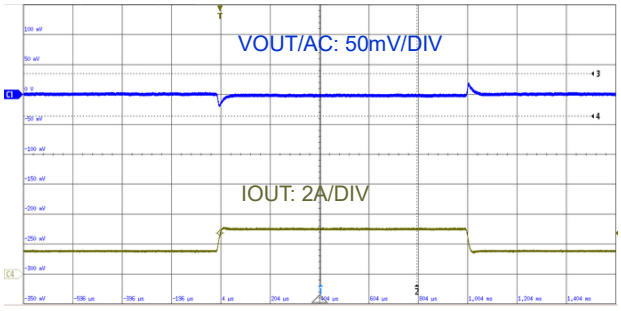
500ns/DIV
I_{OUT} = 0A

Figure 42. Output Voltage Ripple



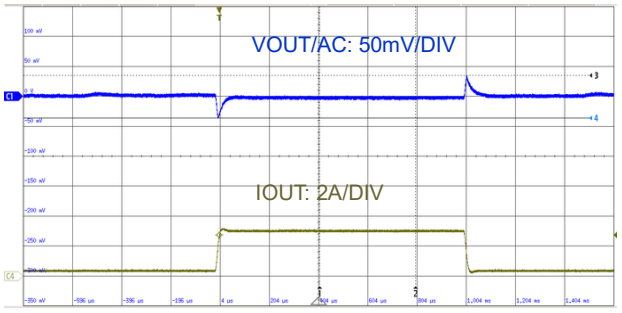
500ns/DIV
I_{OUT} = 3A

Figure 43. Output Voltage Ripple



200us/DIV
I_{OUT} = 1.5A to 3A, 1.2A/μs Slew Rate

Figure 44. Load Transient

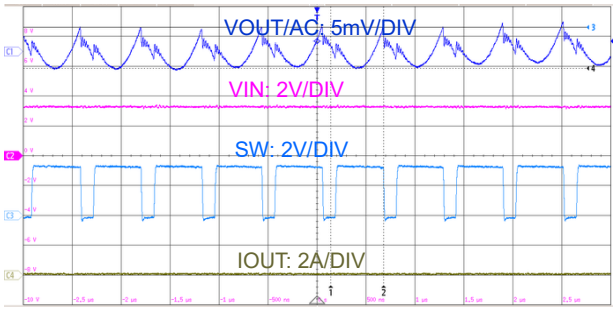


200us/DIV
I_{OUT} = 0.3A to 3A, 1.2A/μs Slew Rate

Figure 45. Load Transient

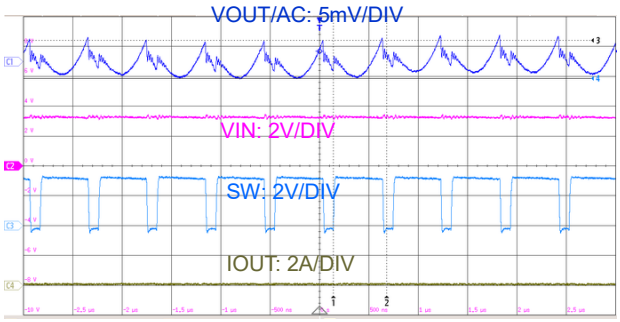
Typical Application Curves (continued)

VIN = 3.3V, VOUT = 2.5V, CIN = 2*22μF, COUT = 4*22μF, TA = 25°C, unless otherwise noted.



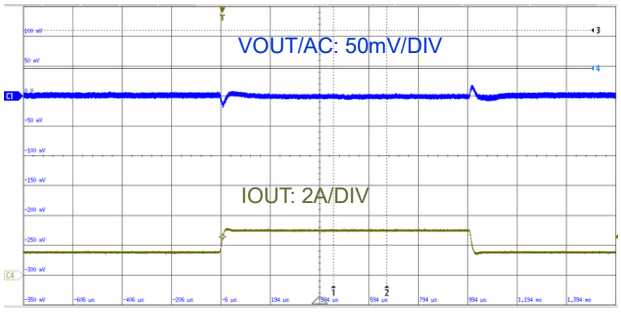
500ns/DIV
I_{OUT} = 0A

Figure 46. Output Voltage Ripple



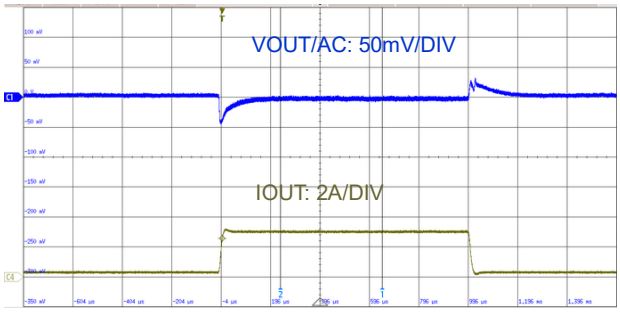
500ns/DIV
I_{OUT} = 3A

Figure 47. Output Voltage Ripple



200us/DIV
I_{OUT} = 1.5A to 3A, 1.2A/μs Slew Rate

Figure 48. Load Transient



200us/DIV
I_{OUT} = 0.3A to 3A, 1.2A/μs Slew Rate

Figure 49. Load Transient

7 Layout Guidelines and Example

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching Power Module, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below and take figures as the reference.

1) The high current paths (GND, VIN and SW) should be placed very close to the device with short, direct and wide traces.
2) Place the input capacitor as close to VIN and GND as possible.
3) Place the external feedback resistors as close to FB as possible.
4) Keep the switching node (such as SW, BST) far away from the feedback network.
5) Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

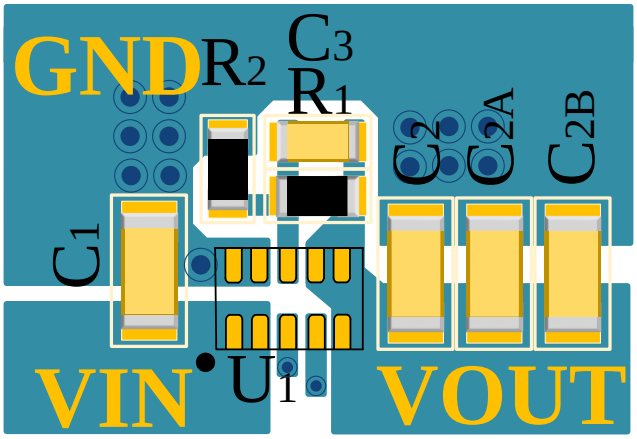
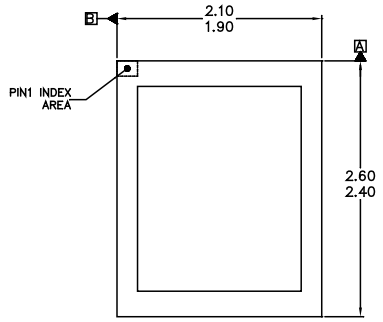


Figure 50. Recommend PCB Layout

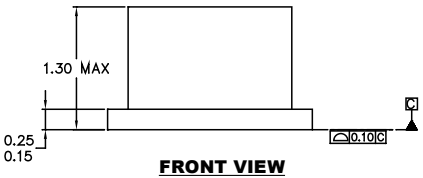
8 Package Information

8.1 Outline Dimensions

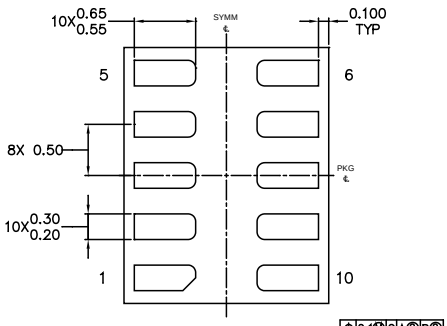
EMLGA2.0X2.5-10 Package Outline



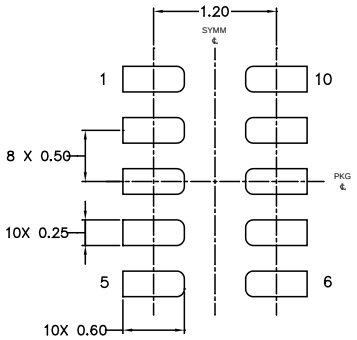
TOP VIEW



FRONT VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

LE020025010A-B-24/06

9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MPQ	OP Temp(°C)
GD30DM1113SVTR-I	EMLGA2X2.5-10	Green	Tape & Reel	4000	−40°C to +125°C

10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2025

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